Passively Probing an InfiniBand System with an Agilent 16700 Series Logic Analysis System

Product Note

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InfiniBand Logic Analysis Support

Description

This product note describes the techniques required for passively probing a parallel InfiniBand channel with an Agilent 16700 Series logic analysis system.

Glossary of Terms

Terminology	Description
SerDes	Serializer / De-serializer ASIC (Typically pronounced "Sir-Deez")
IBA	InfiniBand Architecture
SUT	Signal Under Test
SMT	Surface Mount
PCB	Printed Circuit Board
LVTTL	Low Voltage TTL Logic
SSTL-2	Stub Series Terminated Logic (2.5 Volt)
Mictor	Amp Matched Impedance Connector (Used with high-density logic analyzer cables)
10b/8b	InfiniBand data coding scheme

Agilent Technologies

Generic Block Diagram

Due to loading restrictions and logic analyzer performance, probing raw differential InfiniBand data with a logic analyzer is nearly impossible. The logic analyzer must probe the de-serialized data to passively measure traffic on InfiniBand channels. For systems utilizing discrete SerDes chips, the parallel data is available to route to logic analyzer connectors. Mictor connectors, along with optional isolation circuitry to minimize logic analyzer loading on the parallel data, are connected to the 10b bus running between the SerDes and the InfiniBand controller ASIC. A simplified block diagram of this connection scheme is shown in Figure 1.

Systems that contain the SerDes built into a custom ASIC will require an auxiliary bus to output the parallel data to the ASIC pins to be compatible with a logic analyzer. Without an external SerDes or auxiliary bus the 10b traffic is not observable and cannot be probed by the logic analyzer.

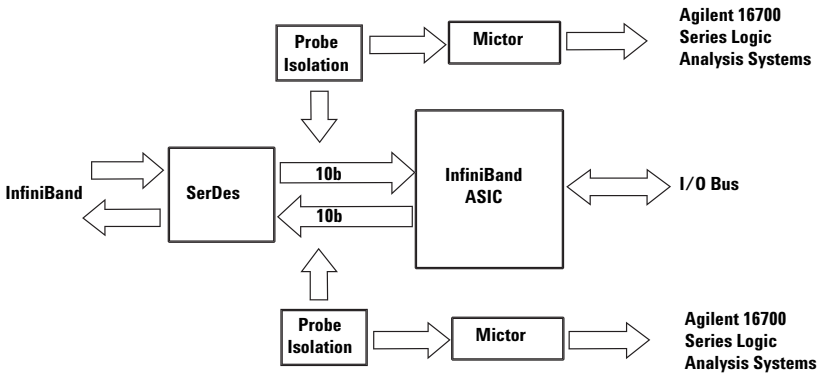


Figure 1. Block diagram of Mictor connectors connected to the 10b bus running between the SerDes and the InfiniBand controller ASIC

Agilent HDMP-2634 SerDes ASIC's

This product note supports probing and analysis of the Agilent HDMP-2634 SerDes. The Agilent SerDes drives 10b encoded data at 10 bits x 125 MHz (DDR) at an SSTL-2 logic level. The data is sampled by the logic analyzer on both the rising and falling edge of the clock for an effective data rate of 250 MHz. Data is displayed on the logic analyzer in raw 10b encoded format, unless a post-processing tool is used to convert and decode the data.

Logic Analysis Features

Triggering

The Agilent 16700 Series logic analysis systems typically contain 4 sequence levels for triggering on data streams. Since the data is effectively double data rate, the 16700 Series system must run in "Turbo" mode, which reduces the number of available sequence levels to six.

Generic Data Display

The 16700 Series system contains a waveform viewer and linear listing window to view sampled data. Both of these tools display the data in the raw format that is sampled by the logic analyzer.

Post Processing and Custom Displays

A tool development kit for the 16700 Series system can be used to create powerful post-processing tools that perform 8b data and packet decoding. This capability is currently available to InfiniBand developers who design Mictor connectors into their InfiniBand host channel adapter (HCA) and target channel adapter (TCA) systems. Figure 2 shows an example of the kind of packet decoding that can be performed. Full real-time acquisition of InfiniBand traffic along with concurrent transactions on other system buses such as PCI-X, CPU buses, PC266 DDR and Rambus® are supported. Events on one bus can trigger measurements on all buses with time-correlated views of all bus events.

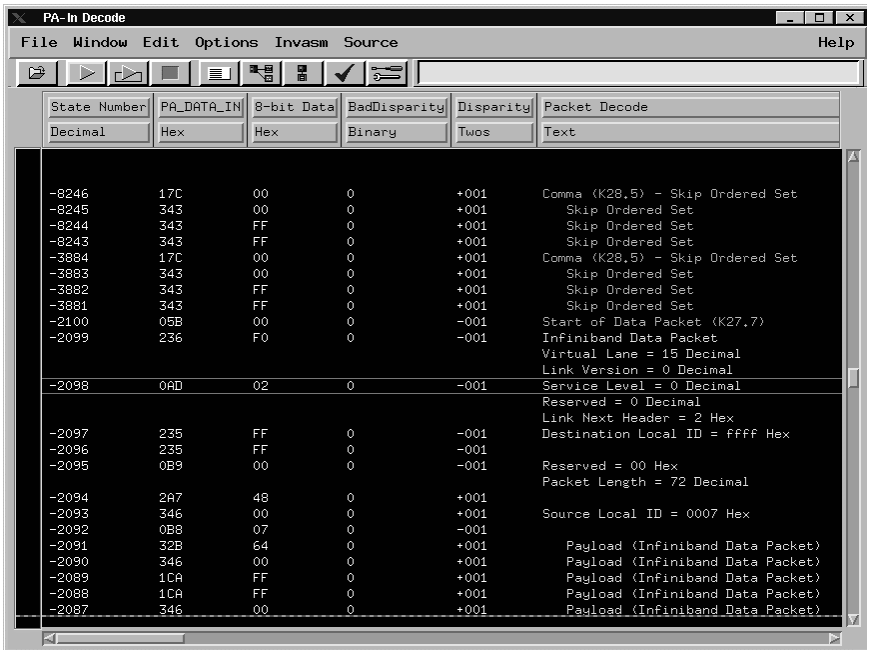


Figure 2. Example of 10b ≥ 8b and InfiniBand protocol decode

Termination Networks

Termination networks are required for probing a digital signal. The termination network isolates the logic analyzer cabling and sensing circuitry from the signal under test and provides a high impedance, low capacitance load at the probe point.

Built-in Termination Networks

The first and simplest technique for probing the output of the SerDes ASIC is to use cabling from Agilent with the termination networks built into the cable tip (Agilent E5346A high-density cable).

Signals are simply routed on the printed circuit board (PCB) to Mictor connectors and terminated internally on the connection cable. Connector placement is critical to minimize the stub length and reflections on signals with fast rise times. However, even the best routing cannot eliminate the stubs completely since the path to the connector and the cable tip is a stub.

The general rule of thumb is to keep the stub length less than 1/5 the rise time of the signal under test (SUT). Whenever it is possible to route the signals within the previous constraints, use the built-in termination networks. They are designed for the Agilent logic analysis systems and are compensated to provide flat frequency response between the signal under test and the logic analyzer input comparators.Refer to the following equations for deciding whether to use built-in termination networks.

$l_{stub} \leq 1/5 \times t_{rise\ time} / V_{prop\ speed}$

$l_{stub} \leq 1/5 \times t_{rise\ time} / V_{prop\ speed} \leq 1/5 \times 1000\ ps / (150\ ps / in) \leq 1.3''$
($1ns_{\ rise\ time}$)

$l_{stub} \leq 1/5 \times t_{rise\ time} / V_{prop\ speed} \leq 1/5 \times 500\ ps / (150\ ps / in) \leq 0.65''$
($500\ ps_{\ rise\ time}$)

The Agilent SerDes has a 1-1.5 ns rise time, which requires traces to be kept between 1.3 – 2 inches in length.

Discrete Termination Networks

When routing constraints prohibit using the built-in termination networks, external components can be designed into the circuit to increase the length between the logic analyzer connector and the signal under test. However, this is only recommended under rare cases when routing issues prohibit the use of standard cabling. Discrete termination networks are complex to design and beyond the scope of this document. Two solutions are provided for signals with 500 ps and 1 ns rise times.

The following sections describe the recommended termination network and how to select components for a target system.

Designing a Discrete RCR Termination Network

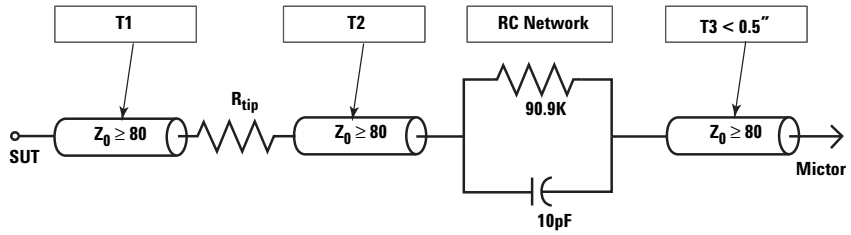


Figure 3. Schematic diagram for designing a discrete termination network

SUT Rise Time	T1 Length	T2 Length	T3 Length	T1/T2/T3 Impedance	R_{tip}
≥ 1ns	≤ 1.4″	≤ 1.4″	≤ 0.5″	$Z_0 \geq 80\ \Omega$	196 Ω
≥ 500ps	≤ 0.7″	≤ 0.7″	≤ 0.5″	$Z_0 \geq 80\ \Omega$	215 Ω

Table 1. Key parameters for designing a discrete probing network

The key parameter to consider when designing a discrete probing network is the rise time of the signal under test. Maximum trace lengths and tip resistor values are dependent upon the rise time.

Note:
The Table 1 values are derived from complex equations that are a function of the logic analyzer connector and cabling electrical characteristics, input network, standard component values, trace impedance and length, and parasitic capacitance and inductance. It is beyond the scope of this document to provide these equations for general discussion. If the maximum trace lengths specified here are not sufficient to probe the signal under test, please consult an Agilent technical specialist.

T1, T2, and T3 are all 80W or higher PCB traces on the target system that connect the various components in the probing network. It is important to keep the trace impedance as high as possible. It is recommended that outer layers be used, which minimize the capacitance and maximize the impedance and propagation speeds.

In general, design the trace on an outer layer with as high impedance as possible without implementing out-of-the-ordinary design techniques such as ground plane cutouts. Keep the trace lengths within the tolerances specified in the table.

The tip resistor R_{tip} must be placed within the T1 length of the SUT. The trace length and tip resistor have been selected to provide maximum frequency response into the logic analyzer input network.

The RC network is connected to Rtip via a PCB trace T2, which should not exceed the T2 length. Use precision 0402 or 0603 SMT components for this network (1% R, 5% C).

The Mictor connector should be placed as close to the RC network as possible, not to exceed T3 length = 0.5 inches PCB trace length. The input impedance of the connector and logic analyzer cable is 120W. In practice it is very difficult to achieve a matched impedance PCB trace, resulting in an inevitable mismatch. To keep the reflections from degrading the setup and hold margins, the maximum length of T3 has been specified in Table 1.

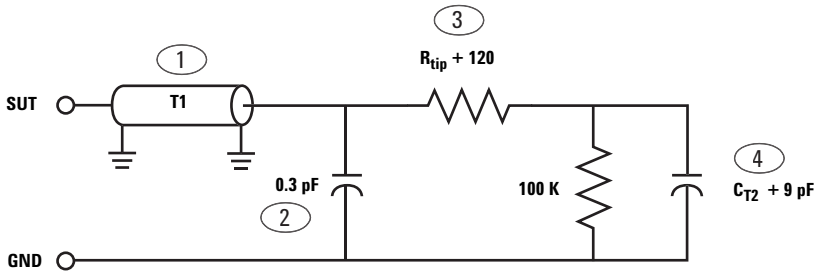


Figure 4. Equivalent load

The discrete probing network and the logic analyzer input can be modeled as shown in Figure 4.

1. T1 is a PCB trace transmission line specified in Table 1. R_{tip} is the sum of the tip resistor and the logic analyzer cable impedance.
2. The 0.3 pF capacitance is the parasitic capacitance of the tip resistor pads.
3. The equivalent series resistance is the sum of the tip resistor R_{tip} and the 120Ω (dc component) logic analyzer cable impedance.
4. The capacitive load is the sum of the logic analyzer capacitance plus the T2 PCB transmission line lumped capacitance. Assuming T2 has a length of 1.4 inches and a 2 pF per inch capacitance, the equivalent capacitive load can be calculated by the following equation:

$$C_{equiv} = 9\ pF + T2_{pF/in} \times T2_{length} = 9\ pF + 2\ pF/in \times 1.4'' = 11.8\ pF$$

Extrapolating T1 and T2 Trace Lengths

It is fairly straightforward to extrapolate the previous values for faster, slower, and intermediate rise times. For signals with rise times faster than 300 ps, a more detailed analysis must be performed. Refer to the following equations for calculating the optimal maximum trace length for the T1 and T2 PCB traces. Note that the following lengths are only approximations since the resistor values are selected to be compatible with industry standard components.

$$l_{max} \approx t_{rise\ time} \times (0.7'' / 500\ ps),\ 300\ ps < t_{rise\ time} \leq 750\ ps,\ R_{tip} = 215\Omega$$

$$t_{rise\ time} > 750\ ps,\ R_{tip} = 196\Omega$$

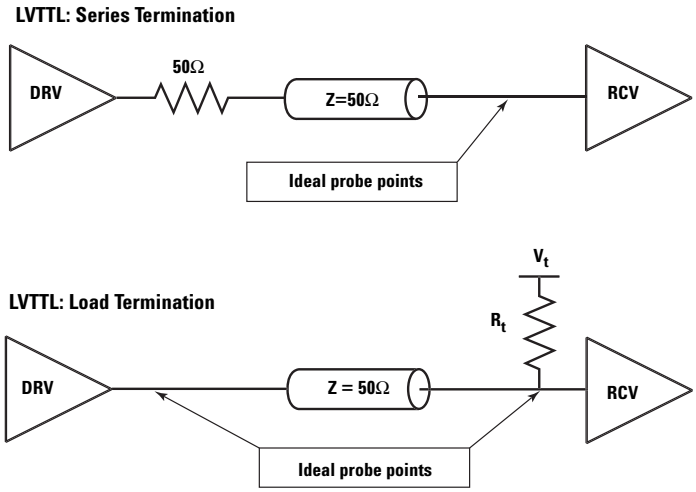


Figure 5. LVTTL Series termination

Routing Techniques

Regardless of whether discrete networks are used or not, the following describes some general guidelines for probing high-speed signals and buses. LVTTL and SSTL logic buses are described here.

Note:
The following schematics are meant to be a basic guide for probing placement, not a description of how to terminate transmission lines. Please refer to the vendors documentation for exact termination techniques.

Series Terminated LVTTL

Series termination resistors can be used to dampen reflections on traces that exceed the length equals 1/5 rise time rule. Signals propagating along a source series transmission line resolve at the load. Midpoints along the transmission line will contain a partial signal rise until the reflection returns and completes the transition. If the intermediate step function voltage happens to be near the threshold voltage of the logic analyzer, metastability may occur and ultimately degrade setup and hold margins into the logic analyzer. Series terminated transmission lines should be probed at the load.

Load Terminated LVTTL

Uni-directional and bi-directional load terminated transmission lines can generally be probed at the driver, load, or anywhere in between as long as all signals are probed at the same position. It is important to keep the stub lengths less than 1/5 the rise time. Ideally, one endpoint should be selected for probing.

SSTL-2

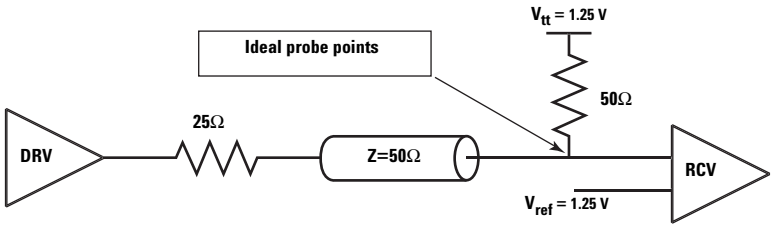
The Agilent SerDes drives/receives signals in an SSTL-2 format. While SSTL-2 provides excellent high-speed signal fidelity during transmission across a PCB board, issues arise that do not normally occur with single-ended LVTTL logic.

An SSTL-2 transmission line is shown in Figure 6. Class-I termination specifies a 50Ω resistor to Vtt at the receiver. Class-II termination requires a 50Ω resistor to Vtt at both the source and receiver. A 25Ω series resistor is typically designed into the driver. In general, it is safe to probe the signal at or very near the load termination resistors, which may be either end for Class-II buses.

SSTL-3

The technique for termination and probing 3.3V SSTL logic is the same except the bias voltage is higher and the logic analyzer threshold must be set to 1.5V instead of 1.25V.

SSTL-2: Class-1 Termination



SSTL-2: Class-II Termination

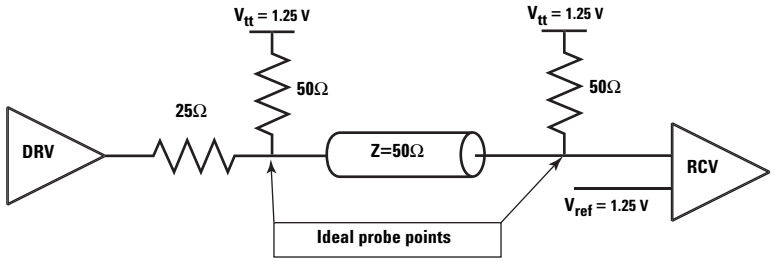


Figure 6. SSTL-2 Class-I termination

Logic Analyzer Connectors

Mictor Connectors

Mictor connectors are used to connect the SUT to the logic analyzer. The connectors each provide for 32 signals plus two clocks. The Mictor connectors each have 38 SMT pins plus five through-hole ground returns. Mechanical documentation and layout information can be found at www.agilent.com.

Connector Placement Techniques

In general, connectors should be placed as close to the probe point as possible to minimize stubs. Refer to the section “Built-in termination Networks” page 3. for maximum recommended stub lengths. If discrete termination networks are used because of real estate concerns, connector placement typically becomes less critical since the maximum distance is effectively doubled. Traces from the termination networks should be matched in length so that all signals have equal propagation delays and setup and hold margins are preserved.

Mictor Connector Pinout

Table 2 describes an example pinout for the Mictor-38 connector. Note that Agilent uses a staggered pin numbering (1 / 2 alternating sides) while other vendors may recommend numbering in order on one side. Either way, as long as the signals are routed to the correct physical location, the numbering scheme does not matter.

Agilent requires pins 1-4 to be left unconnected. In addition, the state analyzer clocks MUST be connected to pins 5 and 6. The 5 center plated mounting holes MUST be connected to ground. All other signals are user definable. Bused signals should place the MSB on pin 7/8, descending downward to the LSB.

Refer to the SerDes documentation for pin numbers.

Odd Pin Side	Signal	Signal	Even Pin Side
1	NC	NC	2
3	NC	NC	4
5	CLKA	CLKB	6
7	DA[9]	DB[9]	8
9	DA[8]	DB[8]	10
11	DA[7]	DB[7]	12
13	DA[6]	DB[6]	14
15	DA[5]	DB[5]	16
17	DA[4]	DB[4]	18
19	DA[3]	DB[3]	20
21	DA[2]	DB[2]	22
23	DA[1]	DB[1]	24
25	DA[0]	DB[0]	26
27			28
29			30
31			32
33			34
35			36
37			38

Table 2. Mictor-38 connectors for the Agilent SerDes

Appendix

Supported Logic Analyzer Modules for InfiniBand

InfiniBand applications should use model 16715A logic analyzer modules and higher. While the frequency of older logic analyzer modules may be sufficient, the eye-finder feature and better setup and hold window makes the 16715A and higher necessary.

Agilent Part Number	State Speed	Channels	Memory Depth
16715/16A	167 MHz	68	2M State
16717A	333 MHz	68	2M State
16750/51/52A	400 MHz	68	4M / 16M / 32M State

Agilent Part Number	Description
16702B	Mainframe with display and touch-screen
16700B	Mainframe with no display
16701B	Expansion Frame

Probing Part Numbers and Ordering Information

Agilent Part Number	Description
E5346-60001	Set of 5 Mictor connectors for use with high-density cable
E5346A	High-density logic analyzer cable with built-in termination networks
E5351A	High-density logic analyzer cable with NO termination. Requires discrete termination.

Related Literature

Publication Number	Title	Description
5968-4632E	*Probing Solutions for Agilent Technologies Logic Analysis Systems*	Product Overview
5968-9661E	*Agilent Technologies 16700 Series Logic Analysis System*	Product Overview
5988-2424EN	*Test Tools for InfiniBand*	Color Brochure

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