The Agilent Technologies
E2920 PCI/PCI-XSeries

Application Note 2

Verify if a device can stand all kinds of protocol variations

Validating servers and workstations that contain various I/O systems, various peripherals and high and low-speed devices, has become a sophisticated task. If you are a validation engineer, you have to ensure that server products can stand all possible protocol variations, that corner cases are covered and that the testing stays within reasonable limits.

Agilent Techologies' solution is a combination of testcards and software running on the system under test, the System Validation Package (SVP).

Aims of this Application Note
- To show how to set up and control several Agilent testcards to simulate PCI or PCI-X application-realistic system traffic.

- To show how to analyze occurred protocol rule violations or data-compare errors.

Questions that can be answered with the help of the SVP

- How can protocol variations be set?

- Can my system stand the protocol variations I set?

- Can my system transfer data in a correct way?

- How can I analyze occurred protocol violation or data-compare errors?

Benefits of the Agilent Product

- Provides the easiest way of defining corner cases when designing systems, bridges and add-on cards.

- Uses the Protocol Permutator and Randomizer (PPR) technology, which ensures permutation of PCI or PCI-X protocol parameters and data traffic in a pseudo-random way.

- Provides measurable test coverage and test repeatability.

- Provides short testing time.
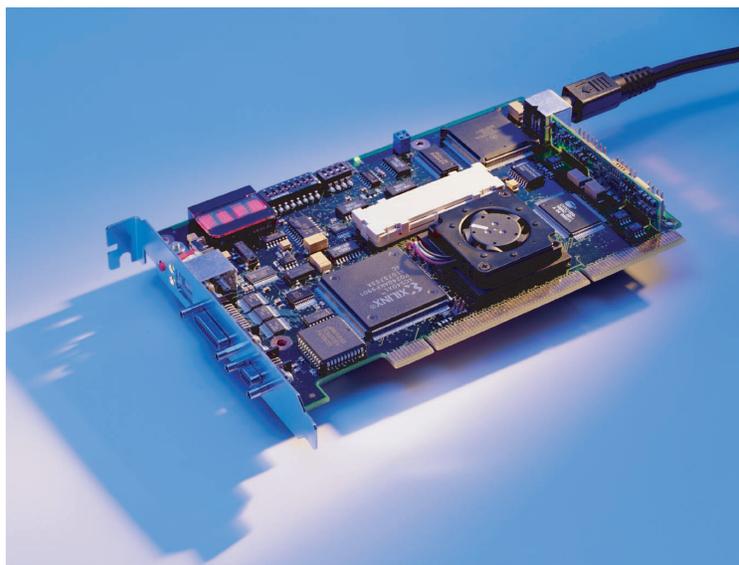
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Setting Up the Test

Introduction

To make the test setup easier, the SVP provides several ready-to-run tests to put particular data paths in I/O systems under stress in a controlled and predictable way.

In this application note, the operating principles of the SVP are introduced by checking the availability/readability of the system memory.

To perform this, the ready-to-run System Memory Read test is used. The System Memory Read test requires one PCI/PCI-X testcard plugged into the PCI/PCI-X bus connected to the host bridge.

Task

A host bridge is to be tested by reading from the system memory. The memory read should be performed with different burstlengths (2, 3, 8 and 11). Errors (protocol violations and data compare errors) that occur during the test should be by using the Analyzer functionality of the testcards.

Steps required to fulfill this Task

The test for stressing a bridge is performed as follows:

1. Set up the test configuration with the help of the SVP GUI. That means, select the ready-to-run test, select the testcards for this test and set the test parameters (for example, address space and test duration).

2. Set protocol variations (different burstlengths).

3. Run the test.

4. Analyze the test results with the help of the Analyzer functionality of the testcard.

These steps are described in the following sections.

Set Up the Test Configuration

To set up the test configuration:
1. Plug the testcard in the bus that is connected to the host

2. Run the SVP software. The software automatically scans all connected PCI and PCI-X busses and other control interfaces (RS-232, USB, Fast Host Interface) for Agilent test cards and initializes them. The main window of the SVP GUI now looks as follows:
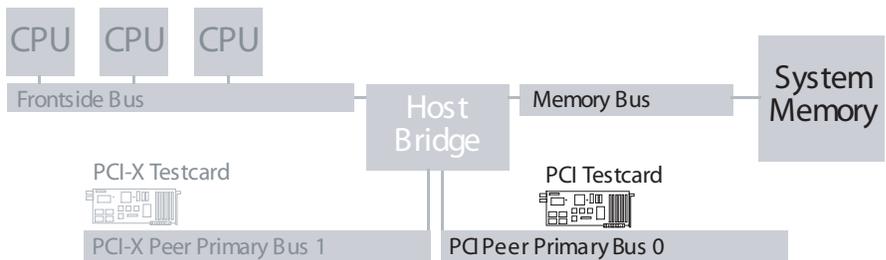
Figure 1.
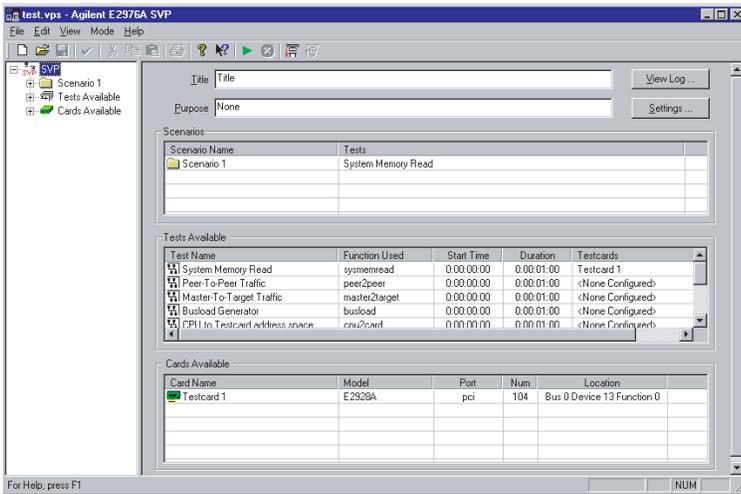
Figure 2.

The SVP software provides three set-up levels; scenarios, tests and testcards:

• One scenario can combine several ready-to-run tests to run in parallel. Several scenarios are executed successively.

• The ready-to-run tests are specified by the testcards they use (must be selected by the user), the address space, test duration, bytes to transfer and the bandwidth with which the test tries to occupy the bus.

• The testcards are specified by their location in the bus system, their features that can be enabled or disabled and their protocol variation settings.

How to set up the scenario, the test and the testcards necessary for this task is described in the following:

To select the System Memory Read test:

3. Select Scenario 1 in the SVP navigator and click the Select Test(s) button in the Scenario Details window.
   This opens the Select from Available Items dialog box.

4. Move the System Memory Read test from the Available list to the Selected list and click OK.
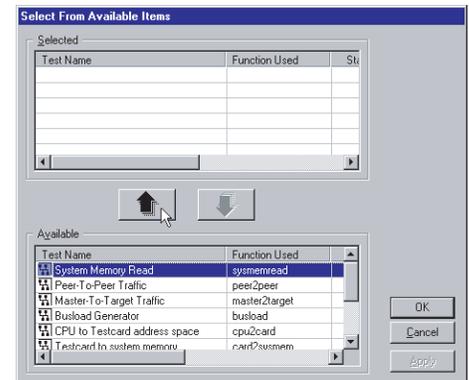
Figure 3.

To select the testcard for the System Memory Read test:

5. Select the System Memory Read item in the navigator and click the Select Card(s) button in the Test Setup window.
   This opens the Select from Available Items dialog box.

6. Move the respective testcard into the Selected list.

In the Test Setup window, the default values for the test parameters are used.

3

Setting Testcard Properties

The Agilent SVP software specifies testcard properties for all available testcards by default. The settings are displayed in the Testcard Set Up window.

To carry out the task mentioned above, the testcards must be set up as follows:

• The Analyzer feature of each testcard must be enabled to allow analyzing of errors occurred.

• The master of each testcard transfers data with burst lengths of 2, 3, 8 and 11.

To enable the Analyzer feature:
1. Open the Testcard Set Up window by clicking the respective testcard in the SVP navigator.

2. Check the Use Analyzer option for each testcard.
   Now, the Analyzer triggers as soon as an error (data-compare error or protocol violation) occurs.

The captured data is stored in the testcard's trace memory and can later be uploaded for analyzing.
See section *Analyzing the Results.*

The testcard properties shown in the Testcard Set Up window include the master and target settings for the testcard.
These settings (displayed when you click the Details buttons next to the Use Master and Use Target options) are the properties permutated by the PPR technology.

By default, all memory accesses are varied through all possible combinations of their attributes. This applies for varying block sizes and the use of the different memory commands, such as write, read, write invalidate, read line, and read multiple. Furthermore, permutations are made in terms of the alignments and byte enables. This means that all variations of byte, word, and dword accesses are used.

In this test example, you have to modify these settings to ensure the use of various burst lengths.

To set burst length variations:

1. In the Testcard Set Up window for each testcard, click the Details button next to the Use Master option.
   This opens the Card Settings dialog box.

2. Enter the values 2, 3, 8 and 11 for the property Burst Length List (Master PPR attribute) and click OK
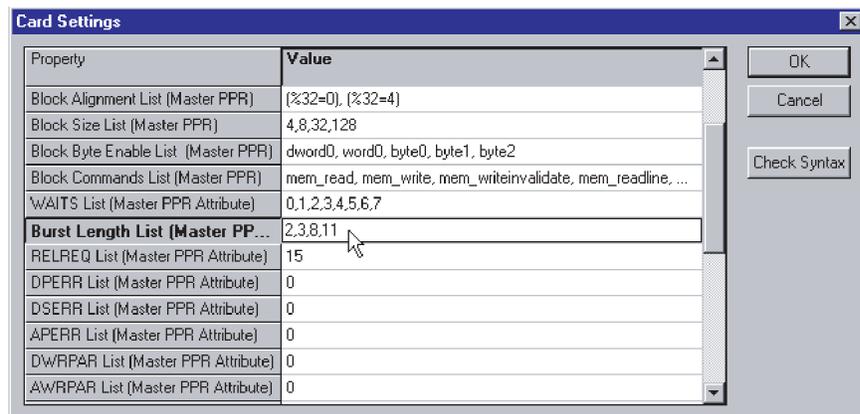
Figure 4.

Note:
The Check Syntax button is used to check if the testcard is able to store the defined variations.

Now the test is ready to run.

Running the Test

To run the test:

1. Ensure that you are in online mode. If not, click Go Online in the Mode menu.

2. Click the run icon ▶ in the tool bar.

The software runs the test and the results are shown in the SVP Reporting dialog box, which is opened automatically.

The test report informs, among other things, about the testcard status. That means, it shows all errors occurred.

In this test example, the report is interrupted as soon as an error (data-compare error or protocol violation) occurs.
To define this:

1. Click the SVP item in the navigator and select the Settings... button.
This opens the SVP Test Settings dialog box.

2. In the SVP Test Settings dialog box, select Stop On Error.

The error is displayed in the SVP test report and can now be analyzed with the Analyzer software of the testcard.
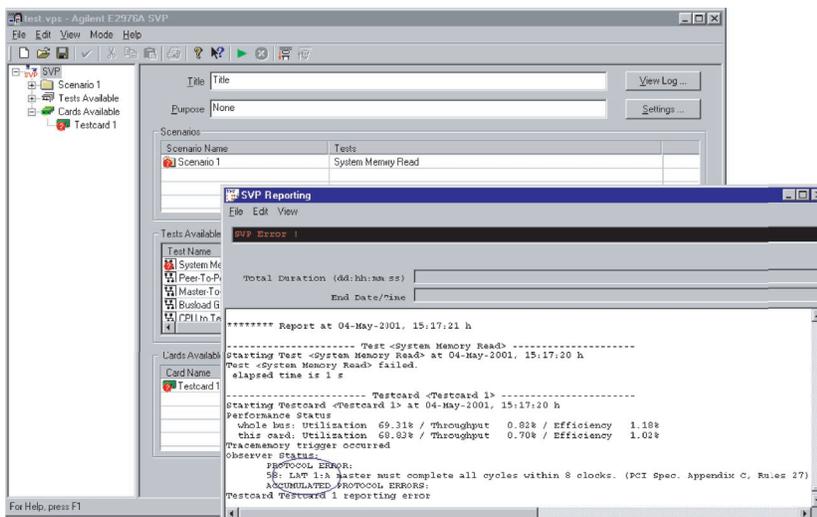
Figure 5.

Analyzing the Results

As previously defined, the test-card's Analyzer triggers as soon as an error occurs.
The captured data stored in the testcard's trace memory can now be uploaded to the Analyzer GUI for analysis.
To help you analyze the captured data, the Analyzer GUI provides several display modes. In this test example, the Waveform Viewer is used to analyze the data.

To analyze the errors with the Analyzer software, some preparations are necessary:

1. Switch the SVP software to offline mode by selecting Go Offline in the Mode menu.

2. Start the E2920 PCI Analyzer software or PCI-X Analyzer software respectively.

3. Open the Waveform Viewer by clicking the in the Analyzer toolbar.

Click the Trigger button to display data around the trigger point. You can now analyze the transaction that causes the protocol error.

You can also use the Bus Cycle Lister, which provides a more compact view of the captured PCI transactions.

Figure 6.

Glossary

PCI Analyzer   The testcard's Analyzer queries for information on the PCI bus, the state of the Exerciser, or the external trigger inputs, so that it can check timing and protocol rules, capture traffic and measure performance.

PCI-X Analyzer   The testcard's Analyzer queries for information on the PCI-X bus, the state of the Exerciser, or the external trigger inputs, so that it can check capture traffic.

PPR Technology   PPR permutates the PCI or PCI-X protocol parameters and data traffic in a pseudo-random way.

Protocol Checker   The testcard's protocol checker continuously monitors the bus and checks for violations of predefined protocol rules, which are partly defined by the PCI and the PCI-X specification and partly by Agilent.
Each individual rule can be masked out and will then neither trigger the trace memory nor appear in any report. To mask rules, click the details button next to the *Use Protocol Checker (Rule Masking)* check box.

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Related Agilent Literature

· Agilent E2925B 32bit, 33 MHz, Agilent E2926B 32/64bit, 33 MHz PCI Exerciser & Analyzer, technical
  specifications, p/n 5968-3501E
· Agilent E2928A 32/64bit, 66 MHz, PCI Exerciser & Analyzer, technical specifications, p/n 5968-3506E
· Agilent E2929A PCI Exerciser & Analyzer, technical specifications, P/n 5968-8984E
· Agilent E2922A PCI-X Master Target Card, technical overview, p/n 5968-9577E
· Agilent E2940A CompactPCI Exerciser & Analyzer, technical overview, P/n 5968-1915E
· Agilent E2976A System Validation Pack, Agilent E2977A System Test Library, technical overview,
  p/n 5968-3500E
· Agilent E2920 Computer Verification Tools, PCI Series, brochure, p/n 5968-9694E
· Intel discusses basic concepts of PCI performance and efficient use of PCI with the Agilent E2920 series,
  case study, p/n 5988-0448ENDE
· HP NSD stabilizes server designs quickly and completely with the Agilent E2920 PCI Series, case study,
  p/n 5968-6948E
· HP HSTC speeds high-end server testing and reduces engineering costs with the Agilent E2920 PCI
  Series, case study, p/n 5968-6949E
· Agilent E2920 Verification Tools, PCI Series gives Altera Corporation competitive Advantage, case study,
  p/n 5968-4191E
-5 Measurements of Agilent E2920 PCI/PCI-X Series p/n 5968-4191E

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