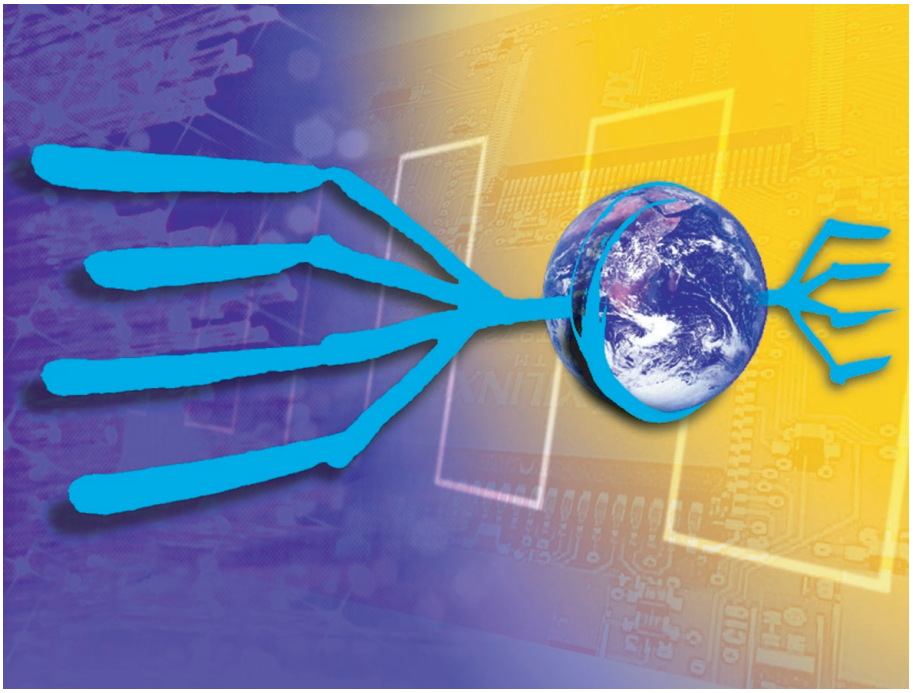
Agilent Technologies ParBERT 81250 Automatic Phase Margin Measurements at 43.2 Gb/s

Product Note



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Introduction

The Agilent 81250 ParBERT 43G (Parallel Bit Error Ratio Tester) is a solution for generating and analyzing electrical data streams of 38 Gb/s up to 43.2 Gb/s. It allows you to stimulate and analyze 16:1 multiplexers and 1:16 demultiplexers at data rates of 2.7 Gb/s and 43.2 Gb/s, according to the OC-768 and SFI-5 (SERDES Framer Interface 5) data range. A measure for signal quality is the phase margin, the timing interval with a bit error ratio (BER) below a certain threshold (e.g. 10^{-9}).

This product note describes a method for measuring phase margins and BER vs. delay (bath tub) plots utilizing a ParBERT 81250 43.2 Gb/s setup in connection with a 10.8 Gb/s generator system. The described setup can be fully automated using the ParBERT application programming interface.

Idea

A ParBERT 81250 43.2 Gb/s setup has two operation modes, clock data recovery (CDR) and external clock mode. Both modes do not allow a direct sampling point delay variation.
In CDR mode, the E4869A 43.2 Gb/s analyzer (DEMUX module) samples the incoming bit stream at the optimum sampling point, i.e. in the middle of each bit. Since the sampling point is fixed, no BER vs. delay measurements are possible in this mode.

For a setup in external clock mode, where E4868A 43G[1] generator (MUX module), device under test (DUT) and E4869A DEMUX are locked on the split clock signal of an external signal source, a variation of the sampling point delay is possible using an external adjustable delay line in the clock path to the DEMUX, see Figure 1a. An analogous setup for E4869A DEMUX performance testing is displayed in Figure 1b. Both setups from Figure 1 are shown in more detail in Figure 2 and Figure 3, respectively.

The drawback of this method is the mechanical delay variation used in such adjustable delay lines, which must be done either manually or by step motor control.

The idea is now to substitute the mechanically adjustable delay line in the DEMUX clock path with a ParBERT 10.8 Gb/s system, where the clock signal delay can be modified very simple by using the ParBERT user software graphical user interface (GUI) or the ParBERT application programming interface (API).

This method for automatic sampling point variation, with a basic setup as outlined in Figure 1b and Figure 4, is used for performance testing in the final production process step for E4869A DEMUX modules.

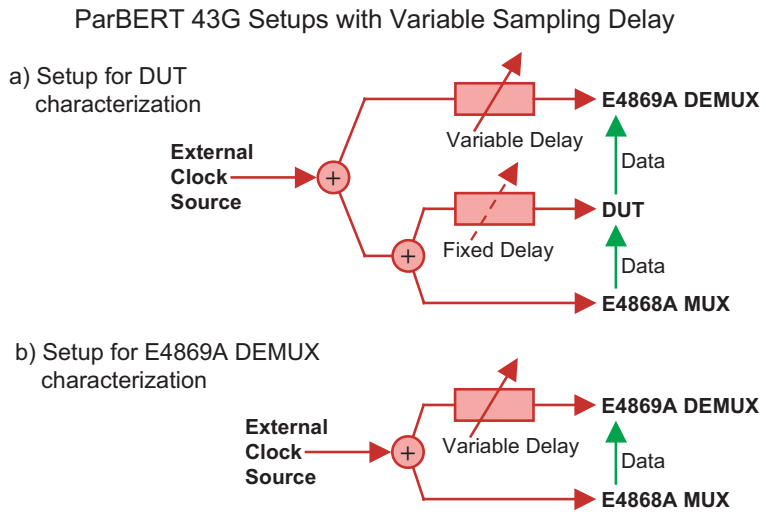

Figure 1: Data and external clock signal path setups with variable sampling delay for (a) device under test (DUT) characterization and (b) ParBERT 81250 43.2 Gb/s DEMUX performance testing. The delay to the DUT (fixed delay) in a) has to be adjusted once to avoid setup-and-hold time violations.

[1] Whenever in this product note the term 43G appears, the data rate range from 38 Gb/s to 43.2 Gb/s should be substituted. This applies also for 10.8G and 10.8 GHz, where 9.5 Gb/s to 10.8 Gb/s and 9.5 GHz to 10.8 GHz should be substituted, analogous for 2.7G and 2.7 GHz

Clock Delay Generation

The ParBERT 10.8 Gb/s system used for clock delay generation consists of an E4808A central module and an E4866A 10.8G generator module. The 10.8G generator module provides additionally to the 10.8 Gb/s data normal and complement output a 10.8 GHz clock signal. A delay change of the 10.8G generator applies simultaneously to data out and clock out.

switched off during delay variation), so that the 43G DEMUX module stays locked on the external clock.

This behavior is necessary to keep up the data synchronization in the whole 43G setup.

This method of clock delay generation has some influence on the quality of the delayed clock signal, since random jitter is inserted into the 10.8 GHz external clock source for the 43G DEMUX.

The additional random jitter leads to phase margin results which deviate slightly from results obtained with a mechanical delay line as shown in Figure 2 and Figure 3. This effect will be addressed in detail later on.

In order to vary the delay in small fractions of one bit length (approx. 25 ps), the delay generation unit of the 10.8G generator must be operated below its 1 ps resolution specification. The resolution limit is not enforced by the user software, so that smaller delay steps (e.g 0.5 ps) can be requested from the 10.8G hardware.

Nevertheless, adjacent delay steps of e.g. 0.5 ps lead to unpredictable deviations from the expected delay shift at the 10.8 GHz clock output, only the mean value after several steps approximates 0.5 ps.

The overall delay accuracy of a 10.8G E4866A generator is specified to be better than 20 ps ± 50 ppm relative to the zero delay placement. As a consequence of the unpredictable delay step size and the overall delay accuracy in the order of magnitude one 43G bit length the actual delay steps have to be determined. Since the 10.8 Gb/s data output shifts simultaneously to the 10.8 GHz clock output, the actual delay step can be measured using a high-speed sampling oscilloscope with averaging turned on (see blue lines in Figure 4). A suitable trigger source for the oscilloscope is the 675 MHz clock output of the 43G MUX module.

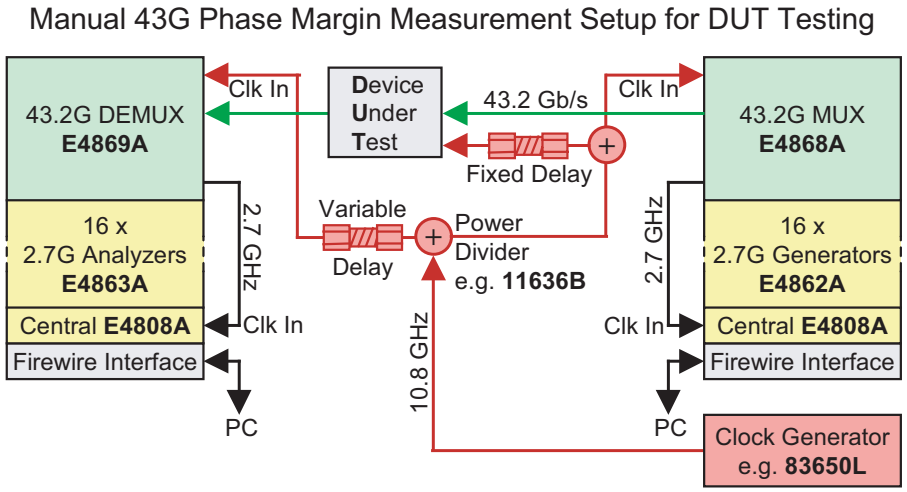

Figure 2: ParBERT 81250 43.2 Gb/s setup for device under test (DUT) characterization. Bit error ratio (BER) measurements with variable sampling delay are realized by a mechanical variable delay line. The fixed delay must be adjusted only once to avoid DUT setup-and-hold time violations.

The principle for clock delay variation is to lock the central module on one end of the split 10.8 GHz external clock source and utilize the delay capabilities of the 10.8G generator. The 10.8 GHz clock out of the 10.8G generator provides then the external clock signal for the 43G MUX module. The whole setup is shown exemplarily for E4869A DEMUX performance testing in Figure 4. The according setup for DUT characterization from Figure 1a can be realized analogous to Figure 2 by inserting a fixed delay line from the DUT to the additional splitter in the clock path to the MUX module.

A delay change at the 10.8G generator occurs continuously at its 10.8 GHz clock out (in other words the clock output signal is never

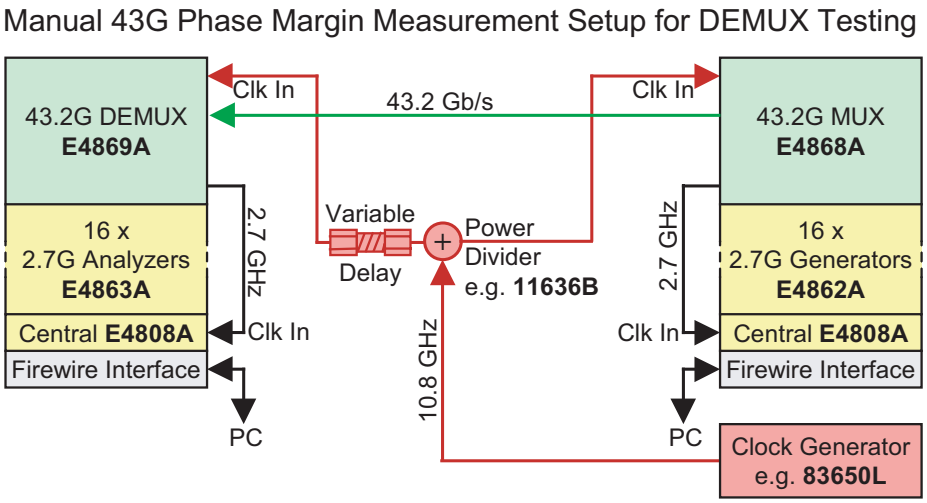

Figure 3: ParBERT 81250 43.2 Gb/s setup for E4869A DEMUX performance testing. Bit error ratio (BER) measurements with variable sampling delay are realized by a mechanical variable delay line.

Measurement Algorithm

Before the described measurement algorithm can be applied, the following precondition must be met:[2] Using internal clock mode for the 43G generator system and clock data recovery for the 43G analyzer system, all 16 43G analyzer system channels must be able to synchronize on a pseudo random word sequence (PRWS) pattern. An overall port BER of 0 is not required.

The measurement algorithm is split in a common section and two application sections. The common section (A) describes the basic steps until the whole setup is prepared for the application sections. The first application section (B) describes phase margin measurements, whereas the second application section (C) explains how to measure bath tub plots.

A) Basic Steps

1. Connect setup as displayed in Figure 4

2. Turn on external clock source with an output power of 6 dBm, use a frequency which equals the desired data rate divided by four (e.g. 40 Gb/s: Use 10 GHz)

3. Switch 10.8G system E4808A central module to external clock-mode

4. Lock 10.8G system E4808A central module on the external 10.8 GHz clock source (GUI: Press *Measure* button)

5. Start 10.8G system, use a clock pattern (101010...) at the data in port of the E4866A generator module. This leads to a 5.4 GHz signal at the 10.8 Gb/s data output, which shifts simultaneously to the 10.8 GHz clock output and can therefore be used for delay step measurements at the oscilloscope

6. Set the delay of the E4866A generator module to an arbitrary positive value (e.g. 1 ns) in order to allow negative delay variations after synchronization

7. Switch 43G generator system E4868A MUX module to external 10.8 GHz clock mode. The MUX module locks on the 10.8 GHz clock from the external clock source

8. Switch 43G generator system E4808A central module to external clock mode

9. Lock 43G generator system E4808A central module on the 2.7 GHz clock provided from the E4868A MUX module. The 16 E4862A generator channels are now clockwise in phase with the MUX module

10. Start 43G generator system, use a PRWS pattern

11. Switch 43G analyzer system E4869A DEMUX module to external 10.8 GHz clock mode. The DEMUX module locks on the 10.8 GHz clock signal from the 10.8G E4866A generator

12. Switch 43G analyzer system E4808A central module to external clock mode

13. Lock 43G analyzer system E4808A central module on the 2.7 GHz clock provided from the E4869A DEMUX module. The 16 E4863A analyzer channels are now clockwise in phase with the DEMUX module

14. Start 43G analyzer system, use the same PRWS pattern as in the 43G generator system

15. Check if all 2.7G E4863A analyzer channels are measuring the BER. Otherwise they could not synchronize due to setup/hold constrains. In this case, stop the 43G analyzer system, increase the delay of the E4866A generator in the 10.8G system by 1 ps. Repeat previous and current step until all channels are synchronized, i.e. as long as there are channels which do not measure the BER (a port BER of 0 is not necessary)

The setup is now prepared for phase margin and bath tub plot measurements.

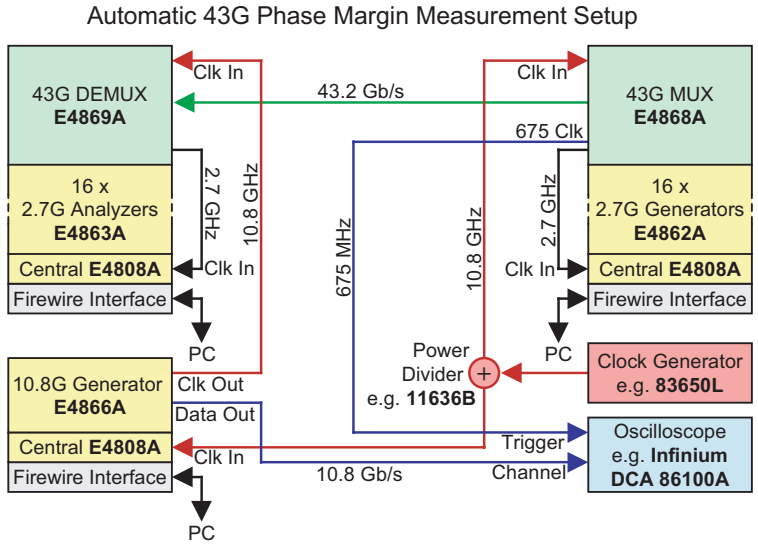

Figure 4: ParBERT 81250 43.2 Gb/s setup for automatic E4869A DEMUX performance testing. Bit error ratio (BER) measurements with variable sampling delay are realized by a ParBERT 10.8G system, actual delay steps can be measured with the sampling oscilloscope.

[2] For further information on the ParBERT user interface and for details on how to perform the described steps, please refer to the Agilent 81250 ParBERT System User Guide

B) Phase Margin Measurements

1. Prepare setup as described in A)

2. Increase the delay (step size not larger than 1 ps) of the 10.8G system E4866A generator until the 43G analyzer system port BER is as close as possible to (but still below) a certain BER limit (e.g. 10^{-9})

3. Measure the position of an arbitrary rising edge from the E4866A generator data out normal on the oscilloscope with highest feasible accuracy (= t_{right})

4. Decrease the delay of the E4866A generator in steps of max. 1 ps until the port BER is as close as possible to (but again still below) the BER limit

5. Measure the current position of the previously measured rising edge (= t_{left})

6. Calculate the phase margin using the formula

$$\text{phase margin} = t_{right} - t_{left}$$

C) Bath Tub Plots

1. Prepare setup as described in A)

2. Decrease the delay of the E4866A generator by at least one 43G bit length (i.e. > 25 ps). The port BER of the 43G analyzer system reads now 0.5

3. Measure the position of an arbitrary rising edge from the E4866A generator data out normal on the oscilloscope with highest feasible accuracy (= $t_{reference}$). This edge position will be the zero reference for all further delay measurements on the oscilloscope

4. Increase the delay of the E4866A generator in steps of 1 ps or less

5. Measure 43G analyzer system port BER and new position of reference edge at oscilloscope (= $t_{current}$). The actual delay on the time axis of the bath tub plot (= $t_{bath\ tub}$) can be calculated using the formula

$$t_{bath\ tub} = t_{current} - t_{reference}$$

Repeat previous and current step until at least a delay shift of two 43G bit lengths (> 50 ps) is reached

6. Shift time axis of bath tub plot so that the starting point 0 ps designates the optimum sampling point, i.e. the center point of the BER bath tub plot

Examples for bath tub plots measured with this algorithm are displayed in Figure 5.

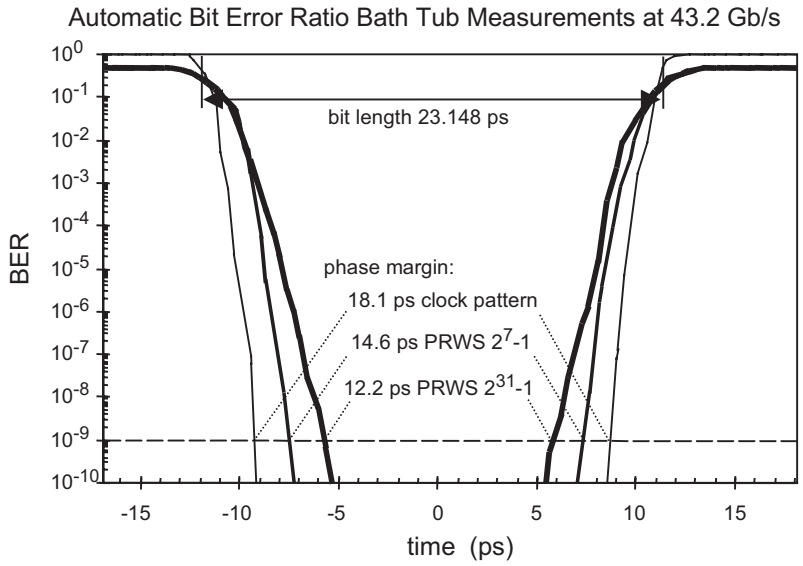

Figure 5: Performance of a ParBERT 43G MUX/DEMUX setup evaluated from bit error ratio (BER) vs. delay (bath tub) plots at 43.2 Gb/s, automatically measured with a setup as shown in Figure 4. The phase margin values, which are evaluated exemplarily at a BER threshold of 10^{-9}, are not corrected by the additionally inserted random jitter from the 10.8G system.

Performance Considerations

The performance of the presented automatic bath tub measurement method depends strongly on two factors.

The first is the accuracy of the delay step measurements, and the second is the amount of jitter injected by the 10.8G system used as variable clock delay generator.

Delay Step Accuracy

The impact of the sampling oscilloscope edge position measurement accuracy can be reduced

- by turning averages on (at least 16),
- by minimizing the time intervals between adjacent delay step meas urements to avoid temperature drifts, and
- by applying as much amplitude as feasible to the oscilloscope trigger and channel in order to reduce the impact of amplitude noise.

Inserted Random Jitter

In contrast to the delay step measurements, the influence of the additional random jitter cannot be minimized. Its impact is shown in Figure 6. The BER plot denominated 'manual' is the result of a bath tub measurement with a setup as displayed in Figure 3. It represents the actual performance of the 43G ParBERT MUX/DEMUX system for a 43.2 Gb/s clock pattern. Before this reference measurement, the mechanic delay line has been calibrated with the sampling oscilloscope.

For a 43.2 Gb/s clock pattern (101010...), the phase margin at threshold 10^{-9} is reduced from 20.9 ps to 18.1 ps, which means that the time interval with a BER below this threshold is reduced by 2.8 ps.

Assuming purely random jitter with gaussian distribution in the clock pattern, the gaussian error function (integral of gaussian distribution) can be used to describe the bath tub plots. The amount of random jitter in a clock signal is normally expressed as one standard deviation σ of the clock edge position. An estimation for this root mean square (RMS) value can be derived from jitter values obtained at threshold 10^{-9} from the BER curves in Figure 6 using the formula:

$$\sigma = \frac{\text{bit length} - \text{phase margin at } 10^{-9}}{6.1}$$

Thus, from the curve with phase margin 20.9 ps at 10^{-9} a RMS jitter value of 0.37 ps can be derived. The curve with phase margin 18.1 ps shows a RMS jitter of 0.83 ps.

Therefore, the RMS random jitter of the whole 43G system is increased from 0.37 ps with mechanical delay variation to 0.83 ps with automatic delay generation.

The sigma value σ_{1+2} (= random jitter of automatic setup) of a gaussian distribution resulting from a convolution of two gaussian distributions with sigma values σ_1 (= random jitter of mechanical setup) and σ_2 (= random jitter inserted by 10.8G system) is given by

$$\sigma_{1+2} = \sqrt{\sigma_1^2 + \sigma_2^2},$$

thus the amount of inserted random jitter (σ_2) can be calculated to 0.75 ps by rewriting the equation. This random jitter value correlates very good with oscilloscope measurements.

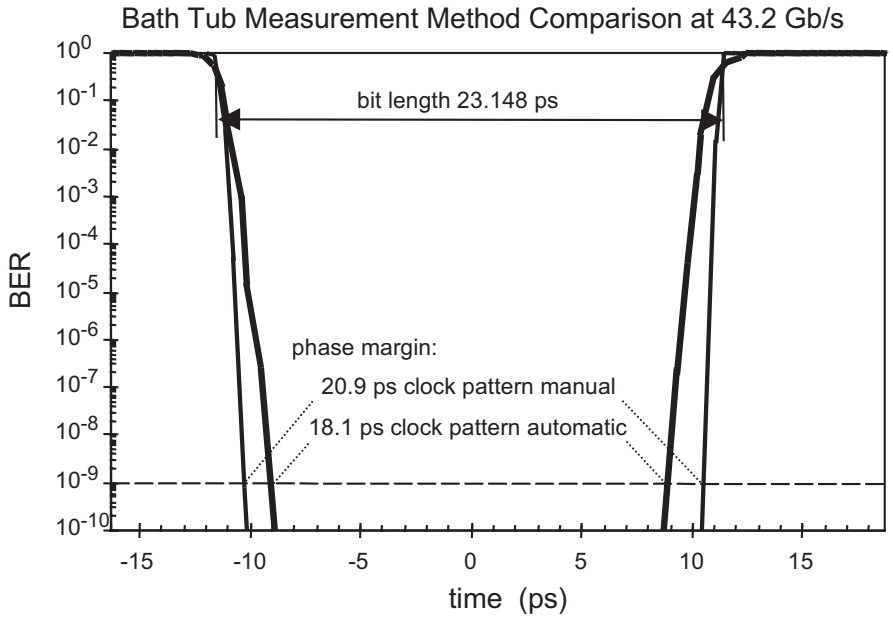

Figure 6: Comparison of bath tub plots at 43.2 Gb/s measured with a manual (see Figure 3) and an automatic (see Figure 4) ParBERT 81250 setup. Phase margin values are evaluated exemplarily at a BER threshold of 10^{-9}. The deviation in the phase margins results from inserted random jitter from the 10.8G system

Correction of Phase Margins

Phase margins measured with an automatic ParBERT setup as described previously (see Figure 4) are decreased by the amount of random jitter inserted by the 10.8G system.

A mathematical correction of measured phase margins at a certain threshold to compensate effects from the clock delay generation is in general for data patterns (e.g. PRWS) not feasible, since the total jitter is given by a convolution of (gaussian) inserted random jitter and actual data jitter, which consists again of a convolution of (gaussian) random jitter and (typically non-gaussian and of unknown distribution) deterministic jitter.

Nevertheless, a rough estimation for the actual phase margin can be obtained from automatically measured phase margins. For this, the difference between a mechanically and an automatically measured phase margin at a given BER threshold has to be determined once for the used data pattern. The difference can then be added to adjacent automatic phase margin measurement results at the same BER threshold.

Related Literature	Pub. Number
Need to Test BER?, Brochure	5968-9250E
Agilent ParBERT 81250, MUX/DeMUX Application, Application Note	5968-9695E
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Photo Card	5980-0830E
Agilent Productivity Assistance for 43G BER Test Solutions	5988-3923EN
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester Product Overview	5968-9188E
Need to Test 40 Gb/s? Brochure	5988-2038EN
ParBERT 81250 Technology Refresh	5988-4174ENUC

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