Designing with Agilent's SFF LC OC-48 Fiber Optic Transceiver

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Abstract

The purpose of this paper is to document different OC-48 physical layer design solutions. These solutions pair the HFCT-5942 with various physical layer chips. SONET compliance at OC-48 for both short reach and intermediate reach applications will be demonstrated.

Reference designs of the optical transceiver with Mux/DeMux chips from three major vendors are available and the test results from each reference board will be discussed. These reference boards are meant to provide users with an interface circuit between the optics and electronics along with information concerning jitter generation, transfer, and tolerance for the optics with the electronics.

Introduction

This paper presents interoperability and multi-rate results of Agilent's HFCT-5942 2.488GB/s LC small form factor (SFF) fiber optic transceivers with three major Mux/DeMux chip vendors. The HFCT-5942 is an industry standard 2x10 footprint single mode fiber optic transceiver for Synchronous Optical Network (SONET) and Synchronous Digital Hierarchy (SDH) short reach applications.

Three reference designs with three different applications were completed. The key elements of these designs are the Agilent HFCT-5942 fiber optic transceiver along with the following chips:

- 1. AMCC SONET/SDH OC-48 16:Bit Mux/DeMux with integrated CDR.
- 2. Vitesse Multi-rate 16:1 SONET/SDH Mux/DeMux with Multi-rate SONET/SDH clock and data recovery IC.
- 3. Broadcom OC-48 with forward error correction, 4:bit, ultra low power SONET/SDH Mux/DeMux

The block diagram, measurement setup, and results of each design will be presented. Each reference board is designed to facilitate measurement of jitter generation, jitter transfer, and jitter tolerance.

The outline of this paper will be as follows:

- Overview of the HFCT-5942
- Major functional blocks of AMCC reference design
- Characterization results with AMCC chip

- Major functional blocks of Vitesse reference design
- Characterization results with Vitesse chipset
- Measurement setup for Forward Error Correction (FEC) Mux/DeMux with the Agilent HFCT-5942
- Characterization results with Mux/DeMux chip
- Schematic block diagram of Mux/DeMux, framer, and HFCT-5942
- Characterization results with framer.

Overview of the HFCT-5942

Agilent's HFCT-5942 LC small form factor (SFF) transceiver is a high performance, cost effective module for serial data at 2.488 Gb/s. The transceiver performs all light to logic and logic to light functions in conformance with SONET/SDH transmission standards. Both the short and intermediate reach links are SONET/SDH compliant at 2.488Gb/s. The fiber optic transceivers are meant for single mode operation at a center wavelength of 1310nm, with output power of -5dBm. The short reach module is fabricated with a Fabry Perot (FP) laser while the long reach module utilizes a Distributed Feedback (DFB) laser with an optical isolator for excellent back reflection.

The transceiver requires a positive power supply in the range of 3.14 to 3.47 V, with nominal bias at 3.3V and power dissipation of 0.66 W. The power dissipation is distributed as follows; the transmitter typically requires 90mA of current, while the receiver typically needs 120mA of supply current.

The HFCT-5942 fiber optic transceivers are supplied in the industry standard $2 \ge 10$ DIP style package with the LC fiber connector interface and are footprint compatible with SFF Multi Source Agreement (MSA).

Transmitter-Optical Eye Quality at OC-3/12/48

In this report, all data are based on the short reach optical transceiver, fabricated with a Fabry-Perot laser. The differential inputs to the HFCT-5942 are AC coupled and 50 Ohm terminated internally. Acceptable input data voltage swing levels range from 200 mV to 800 mV pk-pk. For good signal integrity, it is imperative to have 50 Ohm characteristic impedance on data lines. Furthermore, single-ended operation is not



recommended for good signal integrity operation. The transmitter is designed for a 50% duty cycle. Failure to operate under a balanced code will distort the optical parameters specified in the data sheet.

Under normal operation the HFCT-5942 exhibits excellent eye quality. SONET OC-48 mask margin of 15% at room temperature is typical, as shown in Figure 1. The typical extinction ratio of the optical transceiver is 10dB and the optical output power is -5 dBm, as shown in Figure 1. Figures 2 and 3 are the optical eye and margin for the HFCT-5942 at the OC-12 and OC-3 data rates.



Figure 1. Optical eye using SONET OC-48 optical filter and SONET OC-48 eye mask. Mask margin of 15% and extinction ratio greater than 10dB are typical.



Figure 2. Optical eye of HFCT-5942 at OC-12 using the OC-12 mask and filter.



Figure 3. Optical eye of HFCT-5942 at OC-3 using the OC-3 mask and filter.

Receiver Section

The data and data_bar outputs are internally AC coupled and biased. The output voltage swings levels range from 575 mV to 800 mV pk-pk. The receiver is fabricated with an InGaAs PIN photodiode. InGaAs photodiodes provide excellent responsivity and are designed to operate for wavelengths from 1270 nm to 1570 nm.

The receivers are designed so that the typical sensitivity is -24 dBm at BER of 10^{-10} for OC-48 applications. Figure 4 shows the typical receiver sensitivity as a function of data rate. The measurements were made in optical loopback configuration using a 2^{23} -1 PRBS pattern.



Figure 4. Sensitivity at BER 10⁻¹⁰ as a function of data rate.

Multi-Rate Jitter Result of HFCT-5942

The HFCT-5942 exhibits excellent jitter performance. In a SONET/SDH transport system, the jitter generation specification is 100 mUI pk-pk and 10 mUI rms. The HFCT-5942 transceiver



measures jitter less than 50mUI pk-pk and 5 mUI rms at OC-48 data rate. The intrinsic jitter of the optical transceivers is measured using the Agilent 37718A OmniBER, as shown in Figure 5. The Agilent Pattern Generator 70841B transmits a 2.48832Gb/s PRBS 2^{31} -1 electrical signal to modulate the transmitter inputs of the HFCT 5942. The optical output is attenuated 10dB and received by the Agilent OmniBER.



Figure 5. Measuring jitter generation of HFCT 5942.

Jitter measurements were also completed at OC-3/12/48 using the Agilent OmniBER. As the results in Table 1 indicate, the HFCT-5942 transceiver exhibits extremely low jitter at all data rates.

Table 1. Multi-rate jitter performance of Agilent HFCT-5942at OC 3/12/48

Data Rate	Pk-Pk [mUI]	RMS [mUI]	
OC-3	8	1	
OC-12	35	2	
OC-48	50	5	

Interoperability of Agilent's OC 48 SFF Fiber Optic Transceiver with AMCC S3055

For more detailed information on this reference design, please read the Application Note available from Agilent Technologies, "OC-48 Agilent Small Form Factor Transceiver HFCT-5942 with AMCC S3055 Chip". For more information on the AMCC S3055, please read the data sheet available at www.amcc.com.

The purpose of the OC-48 reference design is to demonstrate interoperability between the AMCC S3055 16-Bit Transceiver with Clock and Data Recovery and the Agilent HFCT-5942 SFF. The board requires only an external +3.3V supply to operate when using a reference clock of 155.52MHz. When using an external reference clock of 2.488GHz, the board requires a -5V supply for the divide by 16 circuit. Interoperability testing may be accomplished via optical access with an LC patchcord to the fiber optic transceiver, or through the high-speed electrical serial ports via SMA connectors.

The AMCC S3055 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-48 (2.48832 Gbps) interface device. The S3055 receives an OC-48 scrambled Non-Return to Zero signal and recovers the clock from the data. The chip performs all necessary serialto-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards.

The major block diagrams of the reference design along with the setup for jitter testing of the AMCC reference design is shown in Figure 6.



Figure 6. Block diagram and measurement setup for AMCC S3055 reference design.

The reference board produces jitter results well below the SONET requirements. The typical results of jitter generation at 0 °C, 25 °C, and 70 °C with the Agilent HFCT-5942L and AMCC S3055 are shown in Table 2.

Table 2. Jitter generation results of AMCC S3055 and	d
Agilent HFCT-5942L reference board	

Temperature [°C]	Pk-Pk Jitter [mUI]	RMS Jitter [mUI]
0	40	3
25	45	3
70	55	5

The AMCC reference design fulfills the jitter tolerance requirements for SONET GR-253 when tested with the HFCT-5942L. The jitter Tolerance



was measured with an optical attenuator B set so that the optical signal received is +1dB above sensitivity, or -17dBm. Figure 7 shows the jitter tolerance results for this setup.



Figure 7. Jitter tolerance results of AMCC S3055 with Agilent HFCT-5942L.

The jitter transfer is measured in the same setup as explained above. The results are displayed in Figure 8 and 9 for the low and high frequency jitter transfer respectively. The outcomes indicate that the jitter transfer requirement is fulfilled for this reference design.



Figure 8. Low frequency jitter transfer of AMCC S3055 and Agilent HFCT-5942



Figure 9. High frequency jitter transfer of AMCC S3055 and Agilent HFCT-5942

Multi-Rate operation results with Vitesse VSC 8141 and VSC 8122.

For more detailed information on this reference design, please read the Application Note 1247 available from Agilent Technologies, "OC-48 Agilent Small Form Factor Transceiver HFCT-5942 with Vitesse VSC8122 and VSC8141 Multi-rate Chip Set Reference Design". For more information on the VSC8122 and VSC8141, please read the data sheet available at www.vitesse.com.

The purpose of the Vitesse reference design is to demonstrate Multi-rate interoperability at OC-3/12/48. This board only requires an external 3.3V supply to operate. The components on this reference design include:

- Agilent's OC-48 SFF fiber optic transceiver, HFCT-5942
- The Vitesse VSC 8122 multi-rate clock and data recovery IC capable of OC-3/12/48 rates.
- The Vitesse VSC8141 multi-rate 16-bit serializer/deserializer capable of OC-3/12/48 rates.
- On board 19.44MHz crystal oscillator

Interoperability testing may be accomplished via optical access of the HFCT-5942 with an LC patchcord. The schematic block diagram is shown in Figure 10.



Figure 10. Block diagram and measurement setup for the Vitesse/Agilent OC-48 reference design.

The Vitesse reference design produces jitter generation results, shown in Table 3, that meet SONET requirements at OC-3/12/48 data rates. Jitter generation was measured using the OmniBER following the schematic in Figure 10.



Table 3. Multi-rate jitter generation results of Agilent/Vitesse OC-48 reference design. At room temperature.

Data Rate	Pk-Pk [mUI]	RMS [mUI]	
OC-3	8	1	
OC-12	38	3	
OC-48	62	6	

This reference design also satisfies jitter tolerance at OC-3/12/48 as per the SONET GR-253. Jitter tolerance was measured as shown in Figure 10, except attenuator B was adjusted so that the received optical power is +1dB above sensitivy.

Figures 11, 12, and 13 show jitter tolerance results at OC-3, OC-12, and OC-48, respectively.



Figure 11. Jitter tolerance of Agilent/Vitesse reference board with GR-253 mask at OC-3



Figure 12. Jitter tolerance of Agilent/Vitesse reference board with GR-253 mask at OC-12.



Figure 13. Jitter tolerance of Agilent/Vitesse reference board with GR-253 mask at OC-48 data rate.

The Agilent/Vitesse Multi-Rate reference design meets the SONET GR-253 requirement for Jitter transfer. Jitter transfer is measured in the same manner discussed above. The low frequency jitter transfer for OC-3/12/48 is shown in Figures 14, 15, and 16 respectively.



Figure 14. Low frequency jitter tolerance of Agilent/Vitesse reference board at OC-3.



Figure 15. Low frequency jitter transfer of Agilent/Vitesse reference board at OC-12.





Figure 16. Low frequency jitter transfer of Agilent/Vitesse reference board at OC-48.

High frequency jitter transfer for the GR-253 mask is shown in Figures 17, 18, and 19 for OC-3/12/48.



Figure 17. High frequency jitter transfer of Agilent/Vitesse reference board at OC-3.



Figure 18. High frequency jitter transfer of Agilent/Vitesse reference board at OC-12.



Figure 19. High frequency jitter transfer of Agilent/Vitesse reference board at OC-48.

Interoperability between HFCT-5942L and Broadcom BCM 8220, a 4-bit Mux/DeMux with Forward Error Correction

For more information on the Broadcom BCM 8220, please visit, <u>www.broadcom.com</u>

This demonstration was completed using the evaluation boards of each respective product. The electrical inputs and outputs of the HFCT-5942 evaluation board were connected via SMA cables to the high-speed electrical ports of the evaluation board for the BCM8220. Figure 20 illustrates the measurement setup and schematic.



Figure 20. Block diagram of jitter measurement setup between the Agilent HFCT-5942 and the Broadcom BCM8220.

The BCM8220 is a 4-bit OC-48 SONET/SDH electrical transceiver with a voltage requirement of 1.8V. Even though the BCM8220 requires a different power supply than the HFCT-5942, there

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is no high-speed electrical interface problem since the HFCT-5942 is AC-coupled and accepts single ended inputs from 150mV to 800mV. The BCM8220 is fully integrated with high-speed serialization and 4-bit deserialization, a built in clock multiplication unit (CMU) and integrated clock and data recovery (CDR) circuit. The highspeed output is selectable at 2.48832Gbps or 2.667 Gbps for FEC-capability. The BCM8220 evaluation board requires a 2.48832 GHz clock input, a 1.8V supply for the BCM8220 and a –5.2V supply for the divide by 16 clock.

The measurements for jitter generation, transfer, and tolerance were completed using the above diagram.

The jitter generation of the Agilent HFCT-5942 and BCM8220, shown in Figure 21, is well within the SONET specifications.

The BCM8220 and HFCT-5942 fulfill jitter tolerance and transfer requirements for SONET GR-253. The jitter tolerance and transfer were measured with the optical attenuator set so that the optical signal received by the transceiver is +1dB above the SONET sensitivity specification at OC-48. Figure 21 shows the jitter tolerance results for this setup. Figures 22 and 23 show the low and high frequency jitter transfer characteristics.

RESULTS JI HITS AMP TUD	TTER CUM ILI IE	IULATIVE	
+UE PE -UE PE PEAK-P RMS FILTER ELRPSED TIME	RK (RK (ERK (S	0.024UI 0.018UI 0.042UI 0.003UI 12KHz HP 20MHz HP 20MHz HP	
STATUS: CUMUL ATIVE	SHORT AUTO FERM TOLERNCE	TRANSFER Function	MULTIPLE WINDOW

Figure 21. Jitter generation result as measured with the setup described in Figure 20.



Figure 22. The HFCT-5942 and BCM8220 fulfills the GR-253 jitter tolerance mask.



Figure 23. The HFCT-5942 and BCM8220 fulfills the low frequency GR-253 jitter transfer mask.







Summary

Interoperability between the Agilent HFCT-5942 has been proven with the AMCC S3055, Vitesse VSC 8141 and 8122, and the Broadcom BCM 8220. These results offer a guideline for jitter performance under various applications such as multi-rate, FEC, and 16-bit LVPECL with CDR. Measurement configurations and block diagrams of the reference designs have been provided.

More information on the layout of the reference design is available at www.semiconductor.agilent.com.

References

- "Agilent HFCT-5942xx Single Mode Laser Small Form Factor Transceivers for ATM, SONET OC-48/SDH STM-16" Data Sheet available at <u>www.semiconductor.agilent.com</u>
- [2] Application Note AN 1232 available from www.semiconductor.agilent.com
- [3] "OC-48 Agilent Small Form Factor Transceiver HFCT-5942 with AMCC S3055 Chip" available at <u>www.semiconductor.agilent.com</u>
- [4] Application Note AN 1247, "OC-48 Agilent Small Form Factor Transceiver HFCT-5942 with Vitesse VSC8122 and VSC8141 Multi-rate Chip Set Reference Design" available at www.semiconductor.agilent.com
- [5] 2.488/2.667 Gbps Ultra Low Power SONET/SDH Transceiver available at www.broadcom.com

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