Jitter Fundamentals: Jitter Tolerance Testing with Agilent 81250 ParBERT

Application Note

Introduction

This document allows designers of medium complex digital chips to gain fast and efficient insight into the operation and performance of CDR, clock system and jitter tolerance. This type of testing is different to conformance testing and manufacturing test; this type of testing targets fast and efficient results on GO – NOGO and some qualitative behavior. Whenever appropriate, this document gives hints to close the gap for conformance and manufacturing test requirements, especially possibilities to calibrate the proposed test approach.

Agenda & Target

- Fast results needed when new ASIC comes out off fabrication
- medium complex digital chips
- performance of CDR, clock system and jitter tolerance
- GO – NOGO testing, some quantitative results
- Extrapolation to Conformance Testing

Figure 1: Agenda & Target

Agilent Technologies

Jitter Tolerance

Jitter Tolerance is:

-Jitter Tolerance – SONET, adapted by nearly all standards

-Sinusoidal Interference, Stressed Eye – 10GbE,optical

-Jitter Amplitude Tolerance (edge displacement!) – XAUI

-Compliance EYE, Common & Differential Mode Noise – PCI Express

-Jitter Tolerance Mask, Jitter Mask

All these expressions deal with the same issue: a receiver of digital data shall tolerate a certain amount of jitter. The expression 'Jitter Tolerance' was originally established by the SDH/SONET standard; in the meantime it is adapted into most of the modern standards of 10GbE, Fibre Channel, PCI Express, etc.. Some other expressions have emerged, fundamentally describing the same thing: Stressed Eye (especially for Optical RX).
When dealing with jitter tolerance, we also find the so called Jitter Tolerance Mask, or simplified Jitter Mask within the documentation.

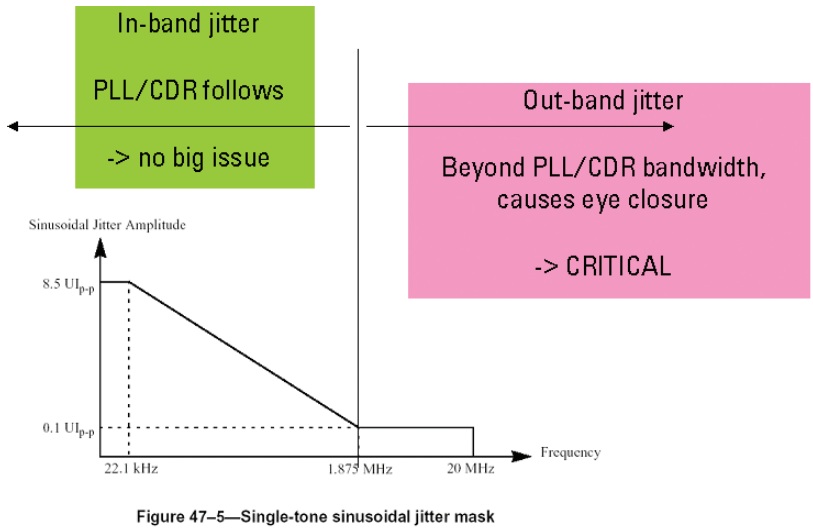

Figure 47–5—Single-tone sinusoidal jitter mask

Figure 2: Jitter Toleramce Mask

This Jitter Tolerance Mask (see Figure 2) is taken from the 10Gbe standard (802.3ae, XAUI) [2], a similar mask appears for the 10G serial side. This is also similar within other standards, but parameter values may be different.

The intention for such a jitter mask is to ensure margin for all types of frequency jitter, wander, noise, crosstalk and other variable system effects. Under these conditions a receive circuitry shall run properly for a very low BER figure (often 10^-12 or lower).

The Jitter Mask defines two different areas:

In-band Jitter
Phase Lock Loop (PLL)/ Cloak-Date-Recovery (CDR) are able to follow, and do not cause eye closure, so this is compensated on the receiver side and does not contribute into the jitter budget. This is the case if the PLL/CDR is able to compensate for >1 UI. The jitter mask can define a very high number of UI's for low frequencies, this number depends on the architecture of the FIFO buffers. So this is not affected by the physical layer circuit performance; a test for it should be once conducted within conformance testing. So for a first Receiver Test it is sufficient to check if the PLL/CDR circuitry works properly.

Outband Jitter
These jitter components are beyond the bandwidth of PLL/CDR, they cause eye closure and are therefore critical for the BER performance, and so they need special care for evaluation. Apart from the sinusoidal part, the total out-band jitter is composed of random and further deterministic content. In the case of XAUI, the deterministic content should be at least .37UI on to of the .1UI sinusoidal. Furthermore, there should be .18UI random jitter. All together this amounts to .65UI total jitter. So a XAUI receiver has to work properly with only 112ps stable data within a 320ps data cycle.

Test Strategy

Outbound jitter causes Eye Closure. As this is most critical, it needs careful characterization and is the most important issue to look at. Therefore, within the Test Strategy proposed here, it is the first step to deal with.

Inband Jitter should be tolerated by the DUT. A functional test should answer if the compensation works as expected. If the compensation works, it is basically a matter of the design, it is able to compensate for a given number of IUs (depending on the F.FO depth). So to once verify for IUs is a task for Conformance Testing.

For manufacturing tests the question is if a single device is working and if it is good enough. So a functional test with some low speed clock jitter/wander will answer this. Depending on how much the process tolerances affect the outbound jitter tolerance, such tests are necessary. But it is not uncommon that chip customers request outbound jitter measurements on a 100% level to avoid surprises.

A (BERT-) pattern generator stimulates the DUT with a pattern (PRBS, DJ/RJPAT or customer/ application specific) that contains a well defined (norm-conformant or customer/application-specific) amount of jitter possibly of all types (RJ, DJ, ISI, PJ, DCD,..) while simultaneously an external BERT-error detector or a built in pattern checker/error counter checks (quantifies) the DUT's error performance to stay below a specified limit.

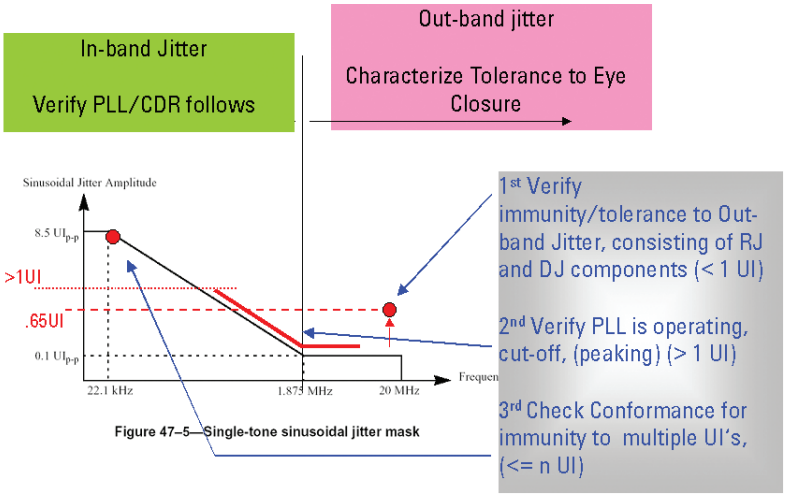

Figure 3: Jitter Tolerance Test Strategy

The tactic to get insight step-by-step is:

Prerequesite:
verify the receiver is working at nominal settings for operation, with no stress.

1st step:
- verify immunity to Out-bound Jitter
- stress the receiver input by eye closure with different jitter components
- inject a modulated eye with all RJ, DJ and PJ components up to and beyond the maximum allowed values
- check for the BER figure.

2nd step: verify that the CDR is operating. For this test there are two alternative scenarios possible:
a) Use the Spectral Decomposition Tool with white Noise Jitter on the Pattern Generator Data; this is possible with any ParBERT analyzer.

b) Use a modulated clock as ext. Clock for Pattern Generator AND Error Detector. For this test it is important that the test system error detector follows the modulation. For a ParBERT 3.3G this test needs to be performed below 10kHz due to embedded PLL restrictions. A ParBERT 13G can do that at any modulation frequency.

3rd step:
Test for conformance to maximum number of UI's at low frequency with help of FM or QM modulated clock sources. Again for a ParBERT 3.3 G the restriction of <10KHz applies.

The First Step: Outbound Jitter

The first step of the Test Strategy is to verify Jitter Immunity/Tolerance to Outbound Jitter:

Jitter injection/eye closure applies to the Out-band part of the Jitter Mask. Here this is pure edge displacement (without Sinusoidal Interference (SI). The edge displacement is basically a Phase Modulation (PM) of the edge. As the Jitter Mask contains the sinusoidal jitter component only, the total eye closure consists of sinusoidal + deterministic (ISI) + random jitter.
In case of XAUI the total jitter budget is .65U; this consists of .1 UI sinusoidal + .37 UI deterministic + .18 UI random jitter.
A flexible and accurate combination of jitter components as: X % sinusoidal + Y % deterministic + Z % random Jitter reduces the hassle of setup.

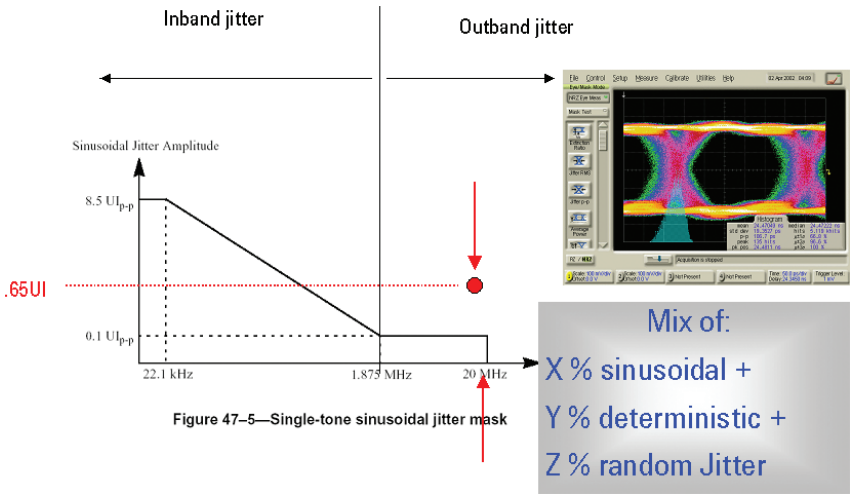

Figure 4: Eye Closure by edge displacement

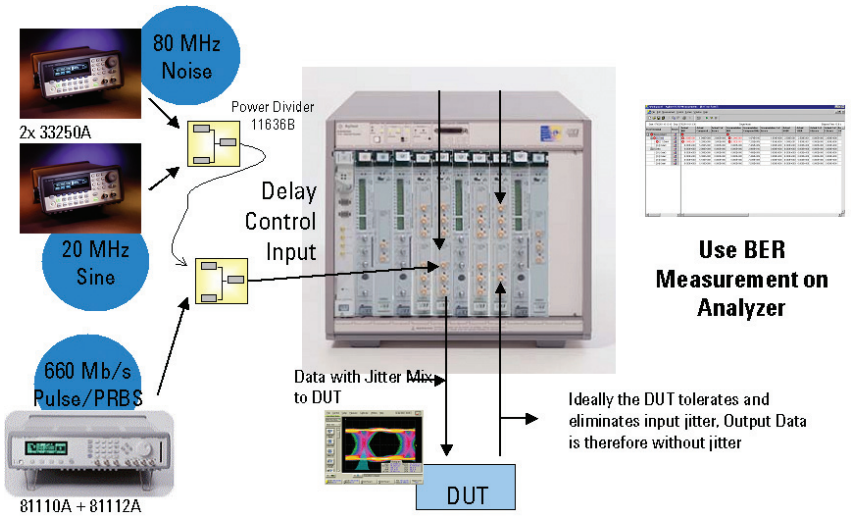

Figure 5: Jitter Injection

Figure 5 shows the setup for Jitter injection/eye closure by edge displacement (w/o SI): A ParBERT generator (3.3G, E4862B or 13.5G, N4872A) is modulated via the 'Control Input'. We use Noise with 80 MHz bandwidth, Sine at 20MHz (or variable) and Pulse/PRBS at up to 660Mb/s. The signals are put together with help of power dividers 11636B. In this case we use power dividers to back-match the signals, and even this causes 6dB loss of the amplitude of the modulation signal sources; the amplitudes provided are still sufficient.

Using a Pulse/Pattern Generator with PRBS capability is a nice approach to emulate ISI. With data rate of 660Mb/s, which is above the bandwidth of the E4862B control Input, some additional 'data smearing' (randomization) is achieved. Short polynomials like 2^5-1 and 2^7-1 are preferred. For a bi-modal jitter behaviour, the Generator can be used in Pulse mode, this delivers two discrete peaks. The generator output connects to the DUT sending the data modulated with a mix of jitter components.

Calibrating the Jitter Injection

The edge displacement setup can be calibrated with help of the ParBERT Output Timing Measurement (see Figure 6). This measurement separates and reports RJ and DJ jitter components. In this case the DUT is replaced with a loop-back cable. This makes it possible to reascertain the eye opening of the modulated generator output. For close tolerances it is recommended to check the eye closure for each modulation content independently.

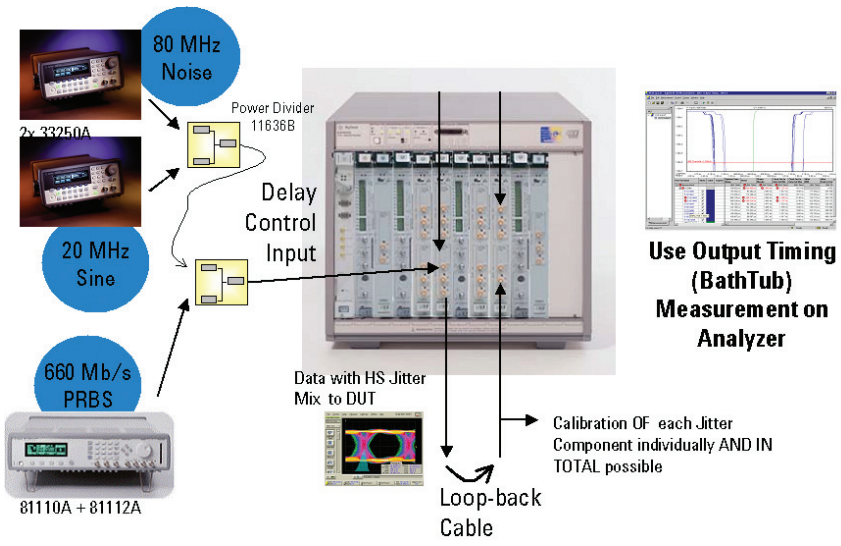

Figure 6: Calibrate the Jitter Injection

Stressed Eye

E/O converter testing in particular requires stressed eye including Sinusoidal Interference (SI), as Figure 7 demonstrates. This adds a sinusoidal signal to the already discussed edge displacement for further horizontal (amplitude wise) eye closure. This is performed with high frequency (<1GHz typically). To simplify the setup, the random part of the FM components can be omitted as the sinusoidal amplitude is already asynchronous.

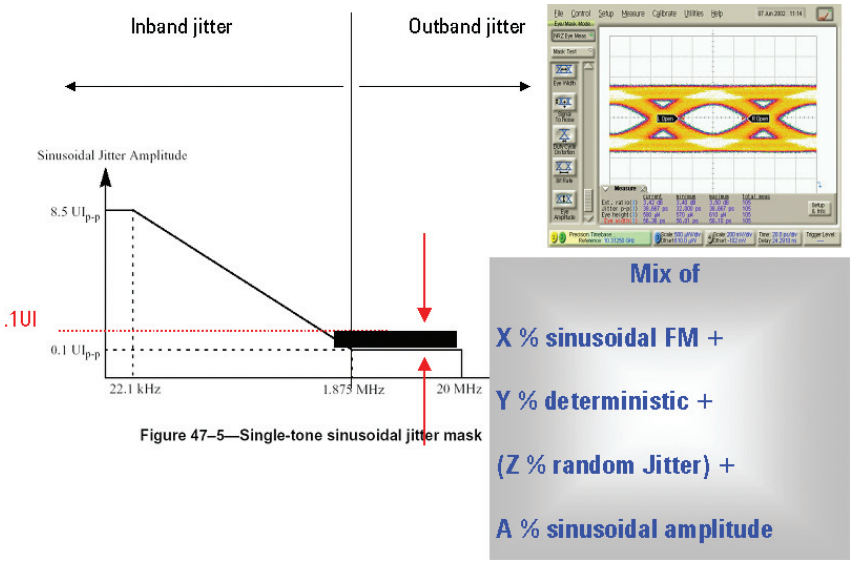

Figure 7: Stressed Eye

Figure 8 shows the setup for Stressed Eye including edge displacement and amplitude noise (SI).
The amplitude noise component is added to the data output with the help of a power divider.

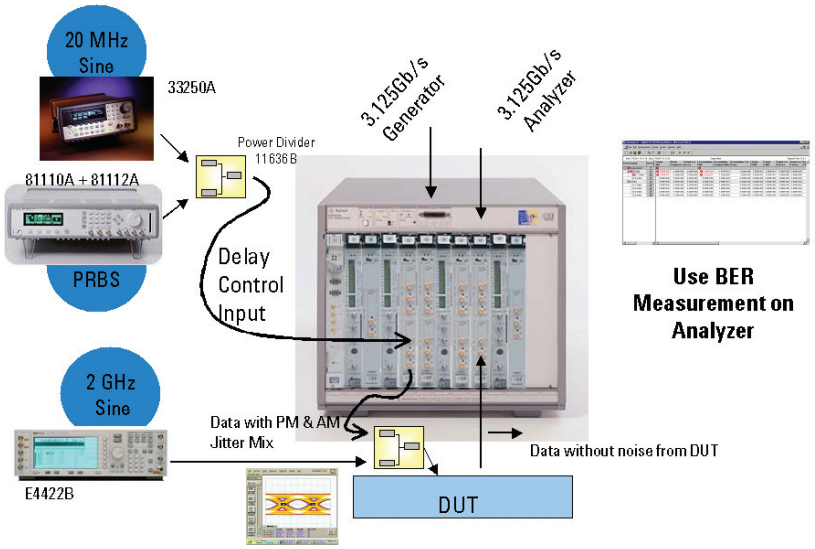

Figure 8: Stressed Eye Setup

The calibration of the amplitude modulation can be performed with the help of the ParBERT Output Level Measurement (see Figure 9).

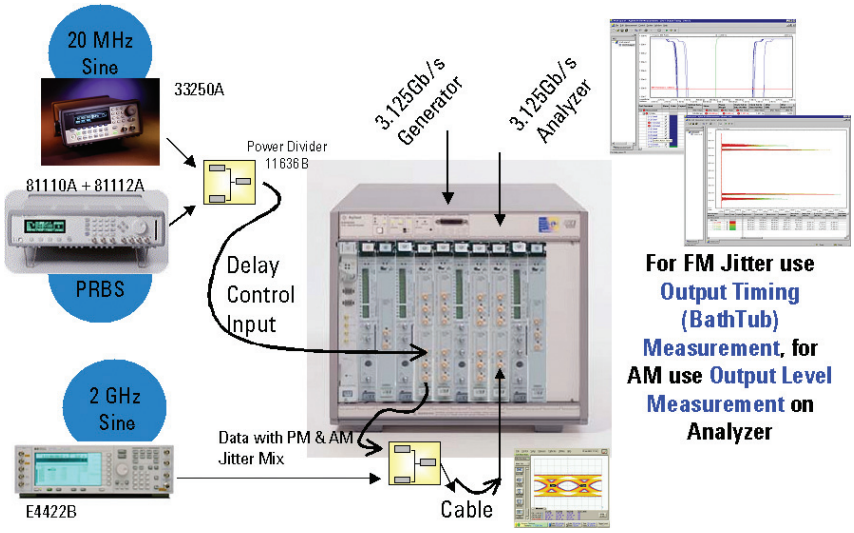

Figure 9: Calibration for Stressed Eye

Stressed Eye Signals

Stressed Eye applies to single ended signals driving the optical PHY. A Stressed Eye is made by a combination of Edge Displacement (PM) and Level Modulation (AM). The edge modulation is a combination of sinusoidal and deterministic jitter. The amplitude/level modulation is sinusoidal.

On a differential signal, the amplitude/level modulation creates either common mode noise, which is harmless as it cancels at the receiver. Or it creates differential noise, which is dangerous, as it reduces the eye opening at the receiver (see Figure 10).

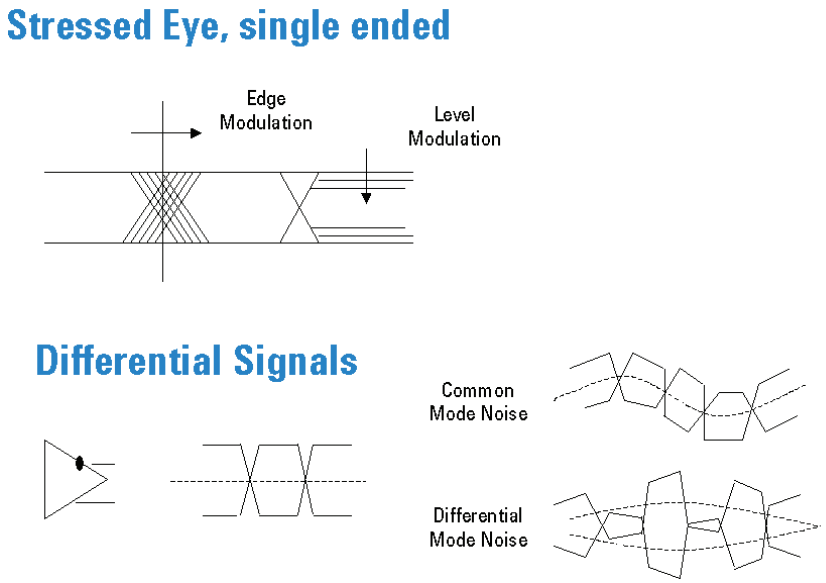

Figure 10: Stressed Eye Signals & Noise on Differential Signals

The ParBERT 81250 generator provides the data on differential lines. To add the modulation signal, there must be power dividers added into both signal lines. When adding these power dividers, the electrical length for both data lines between generator output and DUT RX input must be the same to keep the signal differential.
The power dividers are built of three resistors to ensure proper termination in each direction. Trade-off is amplitude loss of 50 % through the divider. So for a specific swing, the data generator must be set for double amplitude. For common mode noise it is necessary to modulate both data lines with the same signal. Therefore the noise modulating from the Arbitrary Waveform Geenrator (AWG) must be split, with the help of a power divider. This will provide the same amount of noise to both data lines with clean isolation between data and complement data line.

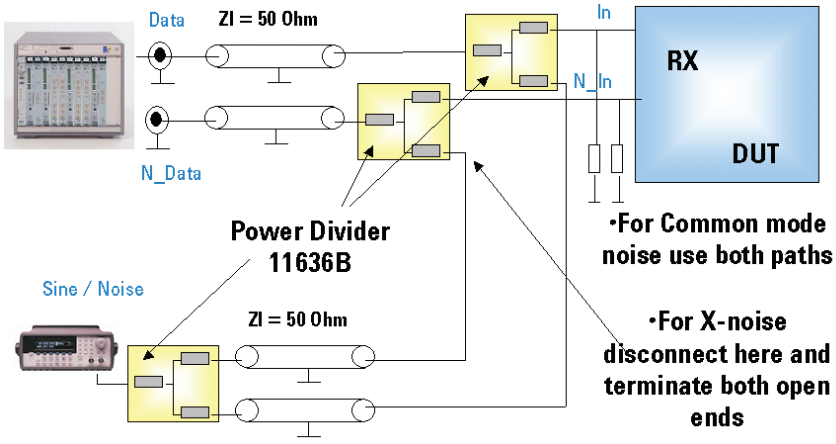

Figure 11: Common/Differential Mode Noise Setup

Step 2: Verify PLL/CDR

The 2nd step of the Test Strategy is to verify that the CDR is operating. For this test there are two alternative scenarios possible:

a) Use the Spectral Decomposition Tool with white Noise Jitter on the Pattern Generator Data, this is possible with any ParBERT analyzer.
b) Use a modulated clock as ext. Clock for Pattern Generator AND Error Detector. For this test it is important that the test system error detector follows the modulation. For a ParBERT 3.3G this test needs to be performed below 10kHz due to embedded PLL restrictions. A ParBERt 13G can do that at any modulation frequency. This is same setup discussed under step 3.

This is the setup for CDR/ Cut-Off Verification: A ParBERT generator (3.3G, E4862B or 13.5G, N4872A) is modulated via the 'Control Input'. We use Noise with 80 MHz bandwidth provided from Agilent 33250A AWG.
The generator output connects to the DUT, sending data with random jitter. The amount of jitter modulation should be small compared to the limit of maximum input tolerance. A practical value is 5 .. 10% of UI typically. The DUT will tolerate this amount of jitter. The CDR follows the low frequency content, but filters the high frequency content. The ParBERT analyzer therefore will detect the low frequency content and report this as constant jitter amplitude up to the cut-off frequency in the Jitter Decomposition Tool. From the cut-off the energy decreases.

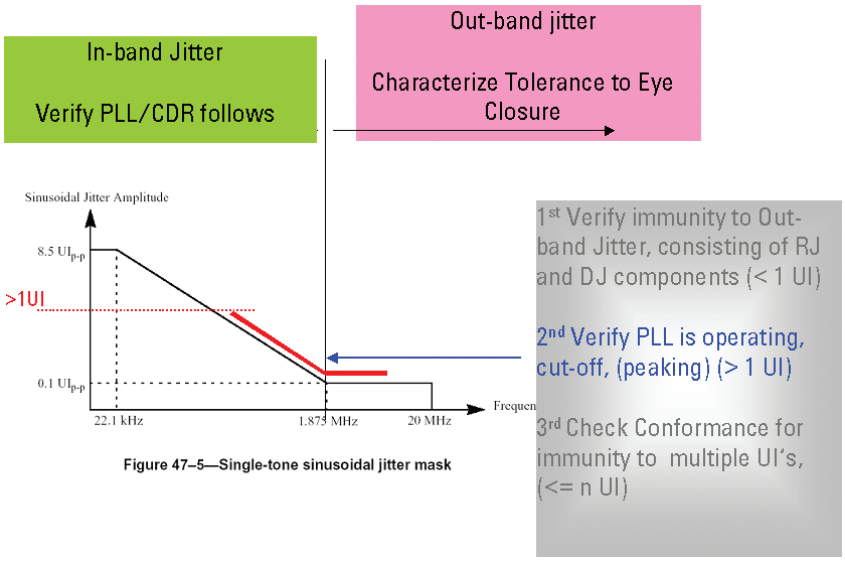

Figure 47–5—Single-tone sinusoidal jitter mask

Figure 12: Verify PLL/CDR

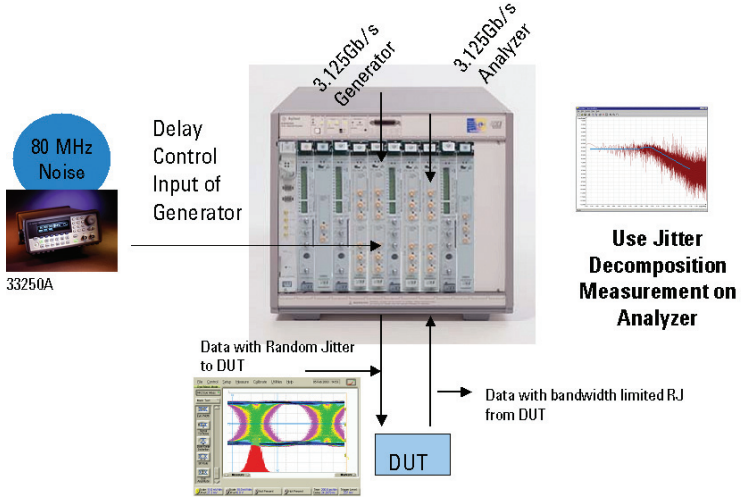

Figure 13: PLL/CDR Verification Setup

Result of PLL/CDR Verification

One model of the Jitter Decomposition Tool is the charactertization of a CDR/PLL device. This asumes the device is stimulated with a data signal modulated with jitter of wide band noise (white noise). The CDR will filter this noise according the bandwidth of it's feedback loop design. The feedback has a certain bandwith, so there will occur jitter supression above this frequency. Or in other words: the device output will follow the low frequency jitter but suppress the high frequency contents of the jitter. The figure here gives such an example with cut-off at 1MHz, and there is some peaking at the roll-off point.

- **Frequency Range of Random Jitter is not bandwidth limited**
- **In-band Transfer is linear, Out-band gets filtered**

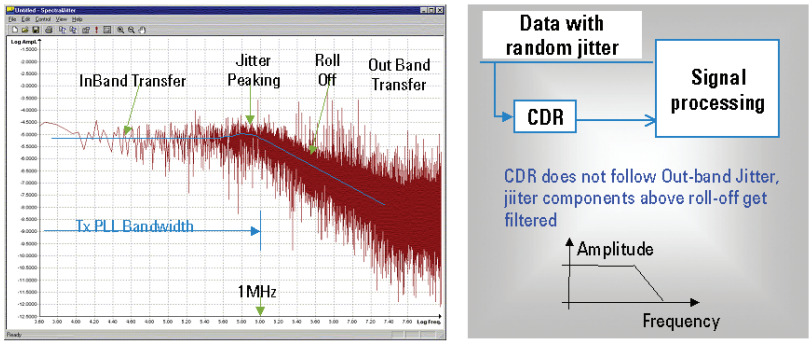

Figure 14: Result of PLL/CDR Verification

Step 3

The third test step deals with the capability of compensating jitter >1Ui up to a maximum number of UI's at low frequency. So this can be jitter or wander.
Here we have to take the limitations of the ParBERT clock distribution into account, as there is some bandwidth limitation in the E4808A clock module as well as within the E4861B data module. This does not apply for the E4809A clock module working together with the N4872A 13.5Gb/s data generators.
The jitter modulation is sinusoidal, the modulating frequency should be the lower value from:
either 10 kHz (limit by E4808A + E4861B) or minimum
frequency from jitter mask, in this case 22.1 kHz In this example the modulating frequency should be chosen for 10kHz.

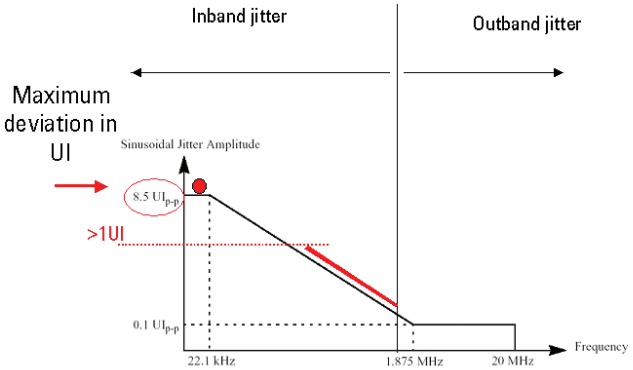

Figure 47–5—Single-tone sinusoidal jitter mask

Figure 15: Verify Jitter/Wander of Multiple UI's

The ParBERT with 13.5G modules does not have such a bandwidth limitation, as there is a mode with direct clock distribution. Therefore this kind of jitter modulation with multiple UIs can be performed at any frequency.

Step 3: Multiple UI Clock Jitter by FM Modulation

To achieve a clock signal modulation with multiple UI's, there is the need for a source which can provide such a modulated clock. There are several possibilities for obtaining such a modulated clock. This setup here describes the use of a signal generator with FM modulation capability. The FM modulation can be achieved either with internal or external modulator. In the case of ext. Modulator the 33250A AWG can be used. Using ParBERT 3.35G limits clock modulation to 10kHz. The desired amount of jitter/wander in terms of UI's can be achieved by a FM (Frequency Modulation) defined by its deltaF (modulation frequency). The delta F can be derived with help of this formula [3]: DeltaF=2π *Jr*Ja, Jr: Jitter Frequency, Ja: Jitter Amplitude. With the XAUI example (needs 8.5 UI's @ 10kHz) this results in a delta F of 534kHz.

So the AWG is set to: Sine, Frequency: 10kHz, Amplitude: 534mV. The Modulator within the Signal Generator is set to FM with modulation range of 1MHz/V

For the analysis we need to consider two scenarios:

1: the DUT output is in phase with the recovered clock. In this case the ParBERT analyzer runs on the same jittered clock as the generator, a single clock configuration is sufficient. If the DUT follows properly, the real-time BER measurement can be performed.

2: the DUT has an embedded reference clock. In this case the DUT includes Fifo's to compensate for clock tolerance. So the output data needs to be sampled based on the reference clock, which needs a two clock

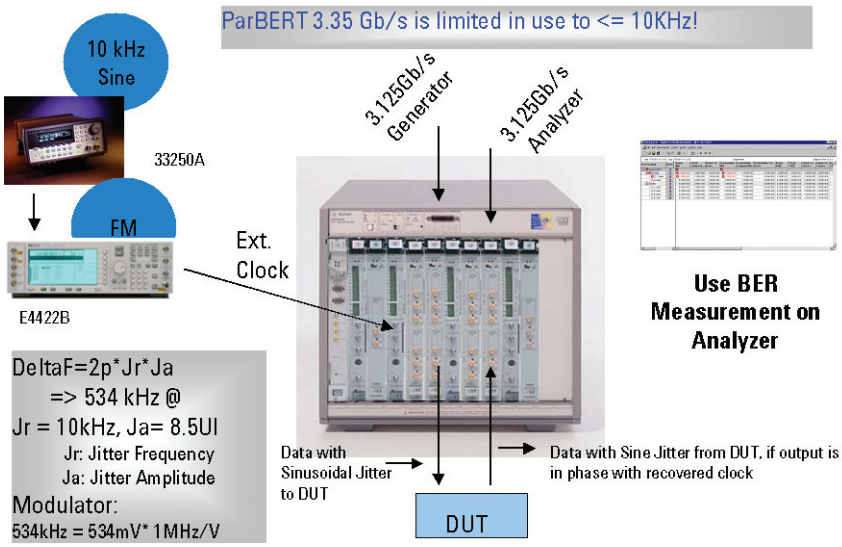

Figure 16: Multiple UI Clock Jitter by FM Modulation

Setup 3B: Multiple UI Clock Jitter

Another approach to obtain clock modulation is with help of QM (quadratur modulation) [4]. This is the most flexible setup for clock jitter generation, limited only by bandwidth of AWG and carrier frequency of the modulator. Now the setup here describes the use of a signal generator with IQ modulation capability. The IQ modulation can be achieved either with internal or external wideband AWG. QM enables a large amount of UI's up to high modulation frequencies, see the comparison of FM and QM modulation below. To make use of the high frequency clock modulation, the ParBERT 13.5G modules with clock bandwidth from DC to max clock rate are used are used in this setup.

In case of XAUI (modulation BW 22kHz, 8.5 UI's) we setup the I / Q signal as can be seen in Figure 18.

Table 1 compares the principle limits of FM vs. QM modulation. QM can provide more UIs at higher modulation rates. The maximum number of UI that could be generated by the using the full 1 GHz bandwidth at 10 kHz and 1 MHz modulation rates. Using the equation:
$B = 2*(\pi*UIpp + 1)*fm$
(Carson's Rule - NOTE: This is an approximation. Bandwidth is actually infinite.) where B = bandwidth (1 GHz) and fm = modulation rate (10 kHz and 1 MHz) we can solve for the maximum peak-peak jitter, UIpp.
Solving for UIpp and substituting for fm, the results are: fm = 10 kHz ---- Max UIpp = 16,000, fm = 1 MHz ----- Max UIpp = 160 (Approximately)

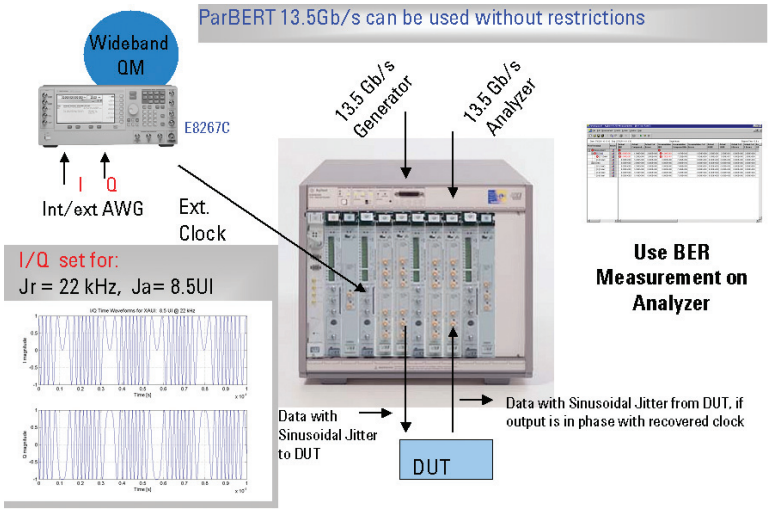

Figure 17: Multiple UI Clock Jitter by QM Modulation

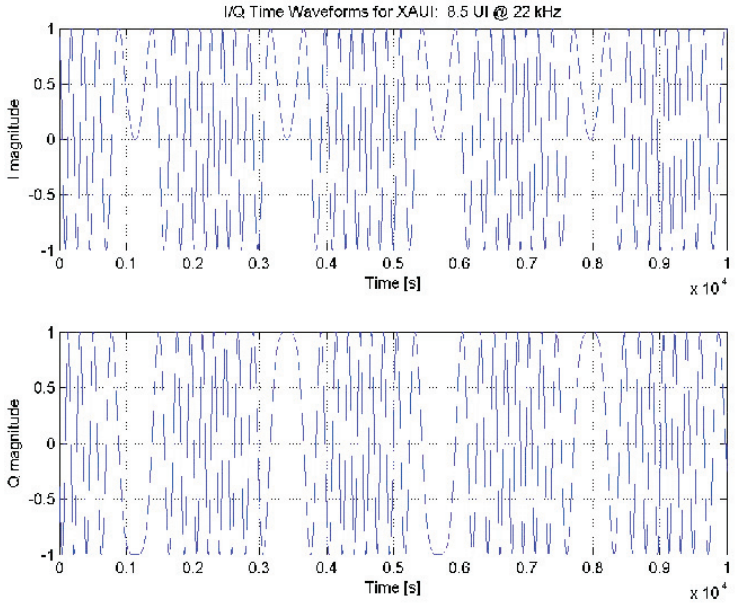

Figure 18: I/Q Signals for XAUI

Table 1: Comparing FM and QM for Jitter Generation

	FM	QM
Instruments	E4422B + 33250	E8267C PSG + hbw AWG
clock freq (carrier)	4 GHz	20GHz
modulation frequency	40MHz	1GHz
max # UIs (10kHZ / 1Mhz)	600 / 6	16000 / 160

References

[1]: Agilent 81250 ParBERt Jitter Injection and Analysis Capabilities, Agilent 5988-9756EN

[2]: IEEE 802.3ae, 10GbE Standard

[3]: Understanding Jitter and Wander Measurements and Standards, Agilent 5988-6254EN

[4]: Quadrature Modulated Jitter Injection, Timothy J. Peters, Agilent Technologies, Inc, Jul 03

Related Literature	Pub. Number
Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Photo Card	*5988-9201EN*
10GbE Technology and Device Charaterization, Product Note	*5988-6960EN*
Agilent Productivity Assistance	*5980-2160E*
Agilent ParBERT 81250 43.2G, Product Overview	*5988-3020EN*
Agilent 81250 ParBERT Product Note (The influence of Generator Transition Times on Characterization Measurements)	*5988-5948EN*
Agilent Technologies ParBERT 81250 Automatic Phase Margin Measurements at 43.2 Gb/s	*5988-5654EN*
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Printed in the Netherlands 2nd December 2003
5989-0223EN

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