Designing High Speed Backplanes Utilizing Physical Layer Test System and Advanced Design System Tools

Application Note

Agilent Technologies

Abstract

Telecommunication systems are required to achieve high-speed data transport up to data rates beyond 10 Gb/s. One of the biggest challenges facing digital designers today in their quest for 10 Gb/s and beyond is that of backplane packaging. An emerging process in the design cycle for the high-speed digital designer includes the use of measurement-based modeling. The success level of this methodology can be very dependent upon which tools are employed in the design lab and how well they work together. This paper will look at the problems introduced into the backplane assembly design by the many linear passive components that create reflections due to impedance discontinuities. Using a typical backplane design case study utilizing two popular design tools, the Physical Layer Test System (PLTS) and the Advanced Design System (ADS), we will evaluate the benefits of the measure, model, and simulate methodology and the advantages it provides to the practical designer.

Typical 10 Gb/s Telecom System

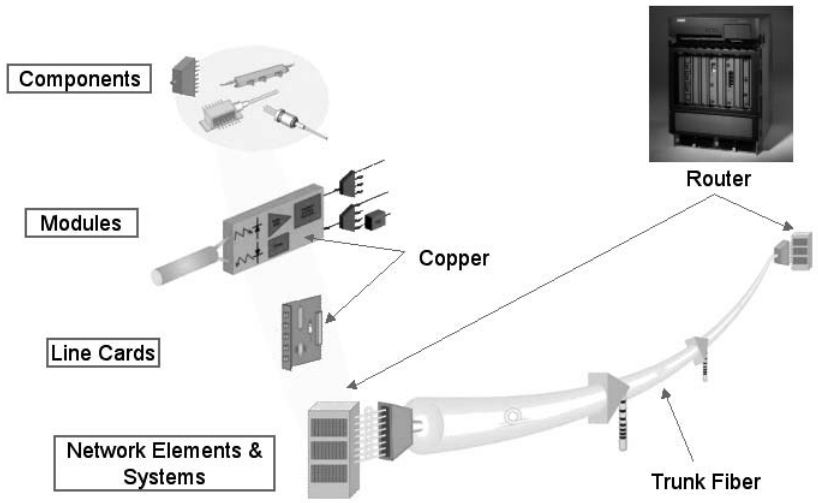


Figure 1. Typical high-speed networking applications.

Today's advanced telecommunication systems are required to achieve high speed data transport up to data rates beyond 10 Gb/s. Modular chassis-based systems, such as core routers, Ethernet switches, and storage sub-systems are becoming evermore challenging for the digital design engineer due to signal integrity problems in the physical layer. Printed circuit boards, connectors, cables, and vias used to be simple components that were easily incorporated into a system with little or no thought. Now, the data risetime from a zero logical level to a one logical level can be less than 100 ps, thus creating microwave transmission line effects in formerly simple structures. In most high-speed networking applications such as those shown in Figure 1, the chassis-based system interface will be used to carry communications between the control-plane processors on each line card. This physical layer copper interface creates many challenges for signal integrity engineers designing, developing, and testing network elements. One of the most challenging and interesting areas for high speed design is in backplane applications. Performance of routers and switches are fundamentally limited by the bottleneck created by the backplane components and therefore this is an area rich for technology breakthroughs and innovation.

An emerging process in the design cycle for the high speed digital designer includes the use of measurement-based modeling. Many design tools are available on the market today that support the iterative process of measure, model, and simulate. The success level of this methodology can be very dependent upon which tools are employed in the design lab and how well they work together. This paper will discuss a typical backplane design case study utilizing two popular design tools, the Physical Layer Test System (PLTS) and the Advanced Design System (ADS).

Impedance Problems are Everywhere!

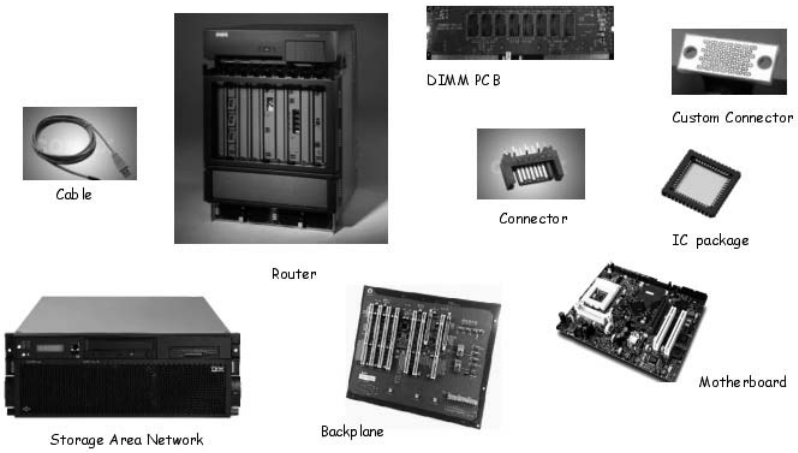


Figure 2. Examples of telecom system passive components.

The physical layer within a telecom system has many linear passive components that create reflections due to impedance discontinuities. As shown in Figure 2, these systems consist of backplane assemblies that contain redundant switch cards, line cards, connectors, IC packages, printed circuit boards and power supply modules. The copper backplane itself is probably the most challenging design project due to the fact that it must have the longest lifecycle in the field. A total router system upgrade allowing a complete retrofit of a backplane is unlikely, therefore the most advanced backplane design tools and methods are required to give the highest backplane performance so as to achieve an extended lifetime in the field. All modular chassis-based systems feature a high-speed backplane and multiple line cards. Performance and capacity improvements are done by adding more line cards and increasing the port density on the line cards. These systems are modular and scale independently without requiring an entire forklift upgrade or replacement. These telecom systems must be designed for high availability with redundant components to ensure uptime.

Agilent's Signal Integrity Portfolio

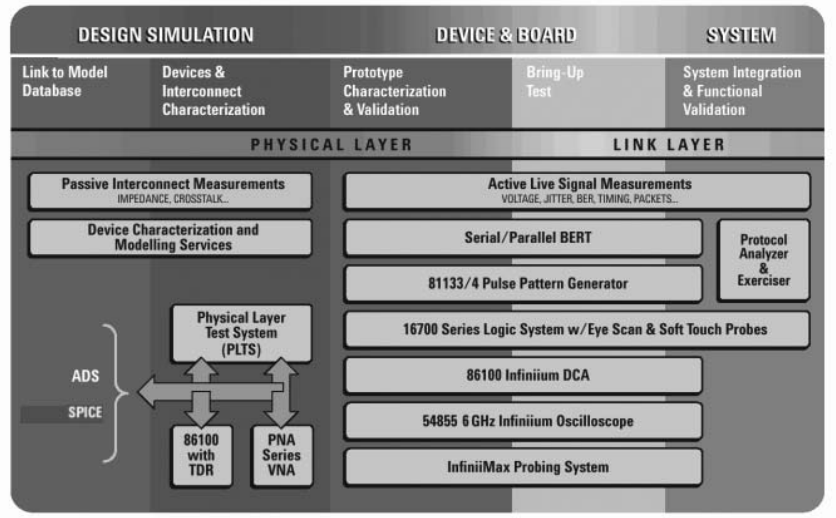


Figure 3. Relationship of Agilent test equipment and software tools.

There are many ways to design high speed digital networks and many tools to accomplish this task in the laboratory. As a general overview, Figure 3 describes the Agilent test equipment and software tools that are used today in many phases of advanced design, development, debug, validation, and standards compliance testing. The area that we will focus on with this application note is the physical layer. More specifically, we will go into detail about the passive interconnect measurements, device characterization, and modeling. A strong synergy can be developed with specific tools within the design cycle that enables a measurement-based modeling approach. The PLTS and ADS tools have cross functional compatibility with importing and exporting data.

Where Today's Solutions Are Used

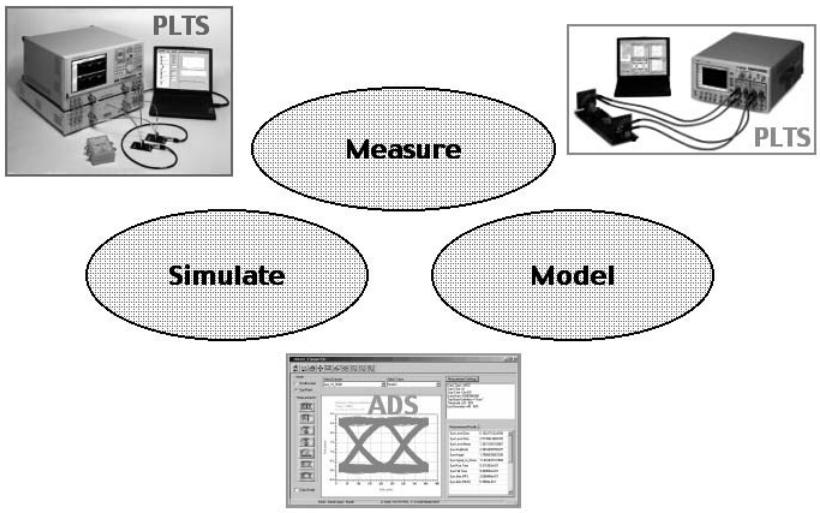


Figure 4. Three phases of design.

The methodology of measure, model, and simulate that has been developed, provides distinct advantages for the practical designer. The iterative process of the three key phases of design shown in Figure 4 allow refinement and optimization, ultimately reducing the overall backplane design cycle time. The value of design software is to reduce the number of iterations through the build and test methodology by providing an environment for virtual testing. The time required to design, produce, and measure is long, and the associated expenses are large. However, there are many practical advantages to producing intermediate prototypes, such as simplifying complex electrical interactions into a measurement-based model, and providing feedback to verify the designer's knowledge of the important physical effects.

Once the first prototype is fabricated, then various instrumentation can be used to obtain a measurement-based model, which then can be easily imported directly into common simulators. PLTS, which controls and calibrates either a Vector Network Analyzer (VNA) or a Time Domain Reflectometer (TDR), will make the measurement and then export the appropriate format of data to the simulator application, ADS software. Touchstone or Citifile are the most common PLTS exported file types.

Simulation Engines for the SI Designer

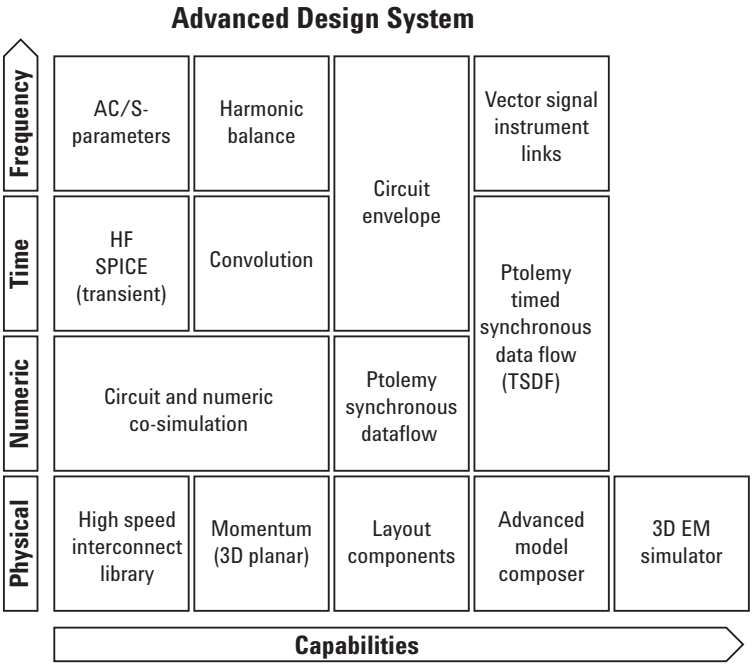


Figure 5. ADS environment.

ADS is a technology rich simulation environment. The most important simulation technologies for signal integrity work are highlighted in Figure 5, with Ptolemy being given specific emphasis. Ptolemy is used to simulate the complete transmitter to receiver link, including coding, pre-emphasis, and equalization techniques. Circuit level co-simulation allows the inclusion of linear and non-linear circuit based models and data based models, including IBIS. Co-simulation at the numeric level allows the inclusion of Matlab® and VHDL models. This co-simulation is a key component to simulating the complete differential backplane channel. Also, physical simulation is tightly integrated into the ADS environment with electromagnetic analysis integrated into the layout and schematic environment.

Backplane Design Flow

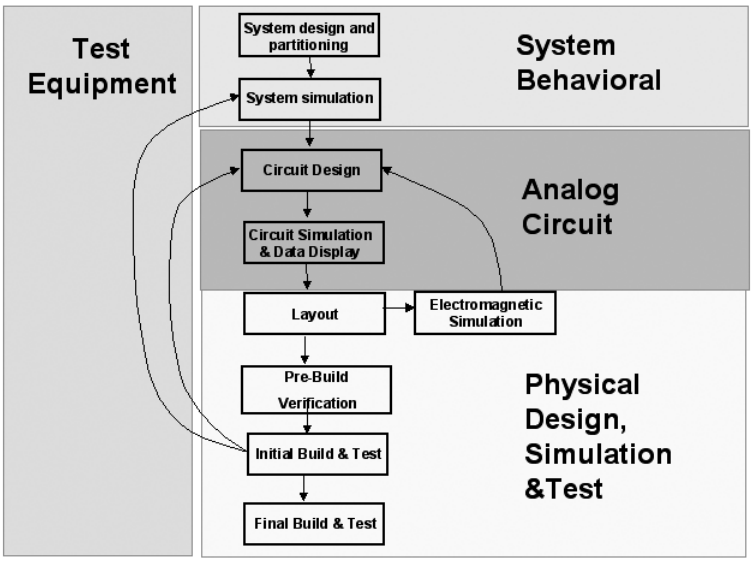


Figure 6. Typical design process.

The design flow for backplanes shown in Figure 6 starts by constructing abstract blocks to define the overall behavior of the system, and then moves to more detailed designs as specific circuits become available. The backplane design process starts by knowing the system performance requirements for the standard being implement. System requirements will determine the need for pre-emphasis or equalization, typical or maximum distances for transmitting a signal, and what type of coding/decoding is included in the signal. Ptolemy can be used to simulate the entire link from transmitter to receiver, including coding and pre-emphasis and equalization techniques. Ptolemy is described as the Integration simulator, with it's ability to co-simulate with analog models from ADS, with Matlab models, with Verilog-A models, and with RTL-HDL. Designers can start with intellectual property (IP) from a variety of these sources, and integrate them into a single simulation using Ptolemy.

The next step is to partition the system design to the specifications for individual blocks. The designer starts to move from the more abstract specs toward circuit-level implementation. The typical process might look like the following;

1. The system designer partitions the design and gives the specifications to the circuit designer for input signals, power consumption, and output signal from the circuit in terms of signal level, noise and allowable error rate.
2. The initial circuit design starts with ideal signal sources with impedance defined for the source and load, and with ideal connections between components.
3. Then, as the basic functionality of the analog circuit is determined, some of the connections are replaced with more realistic transmission lines as knowledge is gained about the actual connection between components (using microstrip / stripline).
4. Finally, replace individual transmission lines with coupled lines that interact (added parasitic effects, coupling, impedance discontinuities).

One thing that enables complete system design is a powerful capability called co-simulation. Co-simulation is a way to combine models that are best simulated in one type of simulator with the models from another type of simulator. For example, system behavioral models are best simulated with a *numeric* domain simulator such as ptolemy, but microstrip transmission lines are best described with frequency domain analog simulators, such as Linear or Harmonic Balance. ADS co-simulation enables a single schematic to contain system behavioral models along with detailed analog circuit-level models. ADS enables co-simulation between system (Ptolemy), analog circuit (Transient, Convolution, Circuit Envelope), and EM physical simulators (Momentum). Behavioral models occur both in system simulation as well as analog simulation.

In terms of analog circuit simulation for high-speed backplane design, the most commonly considered simulators are the time-domain simulators (Transient and Convolution). Other simulators, such as the frequency domain S-Parameter and Harmonic Balance simulators, can be used for some aspects of the backplane depending on the nature of the test. For example, Harmonic Balance is used for fast simulations if there is a steady-state periodic signal which includes active devices. S-parameter analysis is used for determining the frequency response of the transmission path. Physical simulation is tightly integrated into the ADS environment with electromagnetic analysis integrated into the layout and schematic environment.

Throughout the design cycle, it is helpful to construct smaller circuits to test your understanding of the important electrical effects. Smaller test circuits can be used as quick verification of simulations and they can be used as measurement-based models within the simulator. ADS has many ways to link physical tests back into the simulator, including S-Parameters from PLTS as mentioned, or capturing waveforms from scopes, such as the DCA-J (86100C). Eventually, after enough design knowledge has been built up through the iterative use of circuit simulation, electromagnetic analysis, and measurement-based modeling, the designer should return to the system simulation. It is within this environment that the designer should update the system design to include the more specific designs created (check to see if the system performance is maintained per the specification). If compliance to the specifications is achieved, then the backplane is ready for the final build and test. This may mean that the layout produced by ADS is the final layout ready for building, or it may mean linking to other tools for layout through formats such as Gerber or GDS-II.

Physical Layer Test System

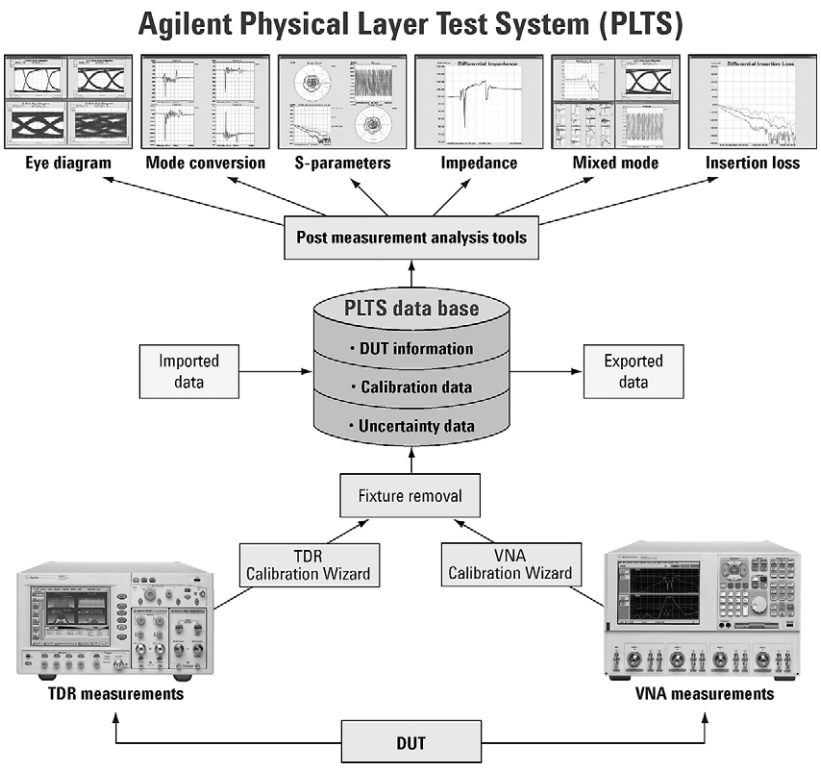


Figure 7. The Physical Layer Test System.

Physical Layer Test System has been designed specifically for signal integrity analysis. As shown in Figure 7, PLTS software guides the user through hardware setup, calibration, and data acquisition. Both Time Domain Reflectometers or Vector Network Analyzers can be used as the measurement engine and the calibration wizard for each will allow advanced calibration techniques. This is helpful when trying to remove unwanted test fixture effects such as cable loss, connector discontinuities, and dielectric loss of printed circuit board material. The PLTS device data base is used to view the performance characteristics in many useful ways. Frequency domain analysis is now becoming mandatory for high speed digital standards such as PCI Express II and Serial ATA. Since high speed data has fast risetime edges that create microwave transmission line effects within the backplane channel, input differential insertion loss (SDD21) is now a required test for compliance. The familiar time domain analysis (TDR &TDT) is complemented by a Novel eye diagram synthesis engine. A virtual bit pattern generator feature allows either a user-defined binary sequence or standard PRBS to be applied to the measured data to convolve eye pattern diagrams. In addition, PLTS applies patented transformation algorithms to present the data in both frequency and time domains, forward and reverse directions of signal flow, transmission and reflection terms, and in all possible modes of operation (single-ended,differential,and mode-conversion).

Measurements on Various Trace Lengths

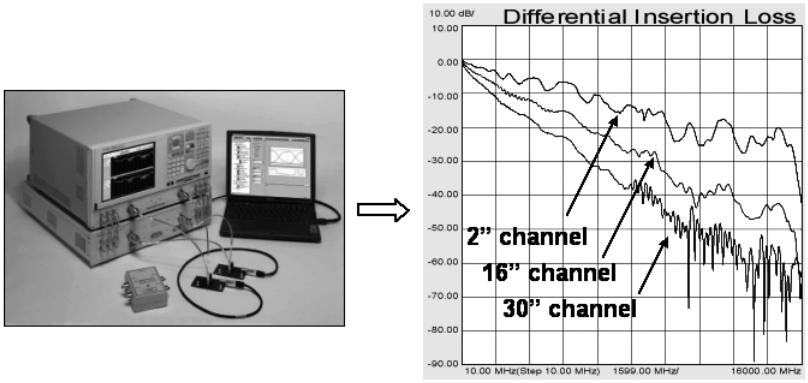


Figure 8. Measured differential insertion loss.

Once the hardware components in the complete backplane channel are locked down, a prototype can be built and evaluated. In the measurements shown in Figure 8, a press fit connector was used to build up a backplane test vehicle. The PLTS system was utilized to measure all 4-port parameters and the differential insertion loss (SDD21) for three different length traces. Most digital standards are now requiring this SDD21 as a performance figure-of-merit. This parameter can be thought of as the frequency response seen by the differential signal as it propagates through the backplane channel. The amount of attenuation verses frequency is a good way to judge performance. Naturally, the shorter the channel, the less the attenuation as a function of frequency.

Mode Conversion

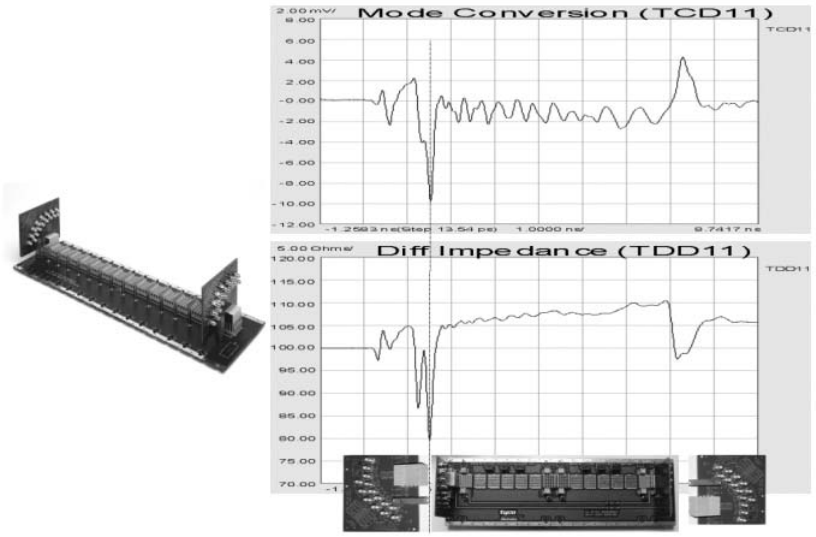


Figure 9. TCD11 to TDD11 aligned in time.

One of the biggest challenges that delays time to market for backplane designs is the presence of crosstalk within the channel (between one differential pair to an adjacent differential pair). Of course, crosstalk within a pair is highly desirable and we call that coupling. This strong coupling provides high common mode rejection ratio (CMRR). However, pair to pair, any mode conversion will create crosstalk. A practical application of how mode conversion can be identified in physical layer devices is shown in Figure 9. This shows a XAUI backplane with two daughter cards that typically transmit data at 3.125 Gb/s. The design objective for this high-speed differential channel is to minimize the crosstalk between adjacent differential PCB traces throughout the length of the channel.The channel consists of the linear passive combination of the backplane and two daughter cards. Any mode conversion from differential mode to common mode will generate EMI and create crosstalk that will be incident upon other channels and will degrade performance. Locating the exact structure within the channel that creates the most mode conversion is a useful debug tool for backplane design.

Looking at Figure 9, the differential to common mode conversion time domain reflection parameter (TCD11) is time aligned with the differential impedance profile of the channel (TDD11) below it. A marker is placed on the largest magnitude peak of TCD11.This is where the physical structure within the channel is creating the most mode conversion and thus the source of the most crosstalk.We can align the TDD11 to the TCD11 in time and therefore spatially co-locate the problematic structure on TDD11.To relate this structure to the channel, we use the differential impedance profile as a reference. It is known that the two capacitive discontinuities on TDD11 are the daughter card via field and motherboard via field, respectively. Since the marker falls upon the second discontinuity on TDD11, it is discovered that the motherboard via field is the biggest culprit to causing crosstalk in adjacent channels. The motherboard via field should be re-routed and the crosstalk generation will be reduced. This measurement and analysis can be done completely within the PLTS tool environment.

Backplanes are a Critical Link

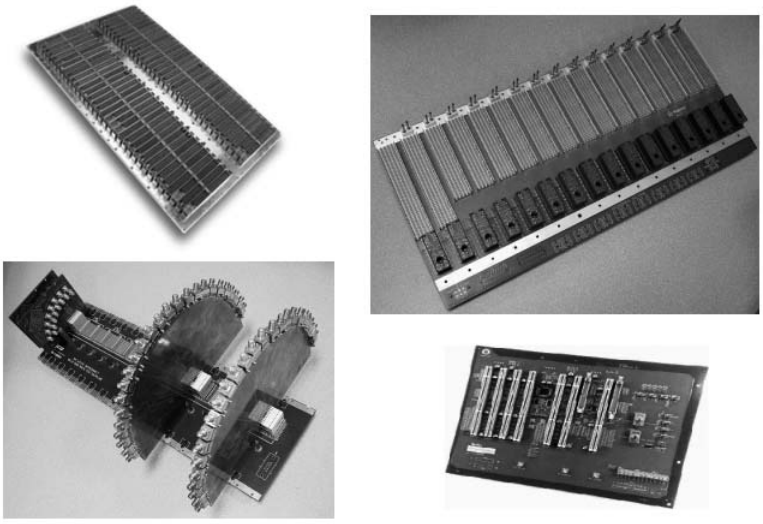
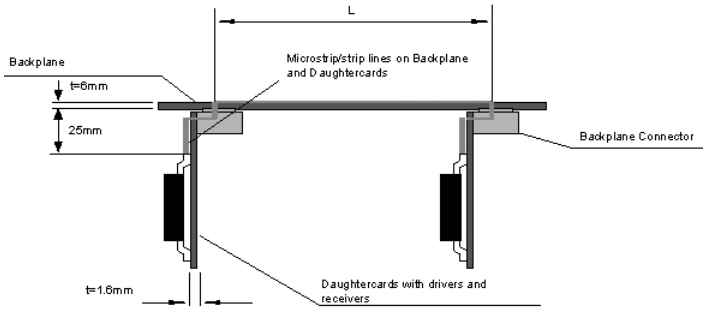


Figure 10. Examples of typical backplanes.

The telecommunications network design engineer does not usually have the flexibility to design the complete system from the ground up. A more realistic situation is where a portion of the system is a legacy, that is, some network components exist and must be utilized in the new design. For example, a new transmitter line card must be developed for a legacy backplane within a ethernet router. The receiver card has already been designed and all that is required is a new transmitter card. In this particular case, the designer would like to simulate how his newly developed transmitter will function within the existing system. Rather than developing a complex model of the backplane channel that consists of complex via structures and connectors, a measurement can be made with PLTS. The 4-port s-parameter data from the measurement can be exported from PLTS as a Touchstone file and subsequently imported into ADS. This saves a tremendous amount of time and yields a very accurate behavioral model for a complex structure. This synergy saves modeling time, produces accurate simulations, and gets the transmitter card to market faster. Figure 10 shows examples of typical backplanes for various high speed serial protocols, including Extended Attachment Unit Interface (XAUI) and Advanced Telecommunications Architecture (ATCA).

System Simulation Setup



Design Parameter	Values for system with	
	micro vias / SMT connector	through hole vias / pressfit connector
PCB Material	Rogers	Rogers
Trace length backplane [mm]	380	190
Length of stub [mm]	-	0.5
Thickness daughtercard [mm]	3	3
Thickness backplane [mm]	3	6
Diameter via [mm]	0.35	0.7

Figure 11. Comparison of two different backplane/connector configurations.

Some decisions need to be made regarding the backplane architecture; namely, whether a star, mesh, or other topology is required. Furthermore, component selections need to be made based on performance cost and manufacturability requirements. Since the via field in a backplane is usually the most challenging structure affecting signal integrity, we will spend some time analyzing this area. In Figure 11, a comparison is made of two different backplane/connector configurations using either microvias in conjunction with a SMT connector or through hole vias with a pressfit connector. In a first step, both alternative scenarios are evaluated in the circuit simulator. The original goal of this investigation is to demonstrate the influence of several design parameters:

- distance between daughter cards
- connector to board interface
- width of transmission lines
- PCB material
- metalization layer in the PCB
- termination of the transmission lines
- type of transmission lines
- statistical variations

For this special application, two typical cases will be highlighted which demonstrate the superior behavior of micro via technology and SMT connectors compared to traditional pressfit connectors and through hole vias. The following general system scenario in Figure 11 is used for this simulation study. The signal path is a point-to-point connection between two integrated circuits on two different daughter cards. The daughter cards are plugged into a backplane printed circuit board. The connections are done using a connector with pressfit pins and alternatively a connector with a surface mount interface to the backplane. The characteristic impedance of differential striplines is Z_0diff = 100 W and the data rate applied is 10 Gb/s using a Non-Return Zero (NRZ) 8B10B code. The table in Figure 9 lists the different design parameters of the two experimental test vehicles.

System Simulation Setup

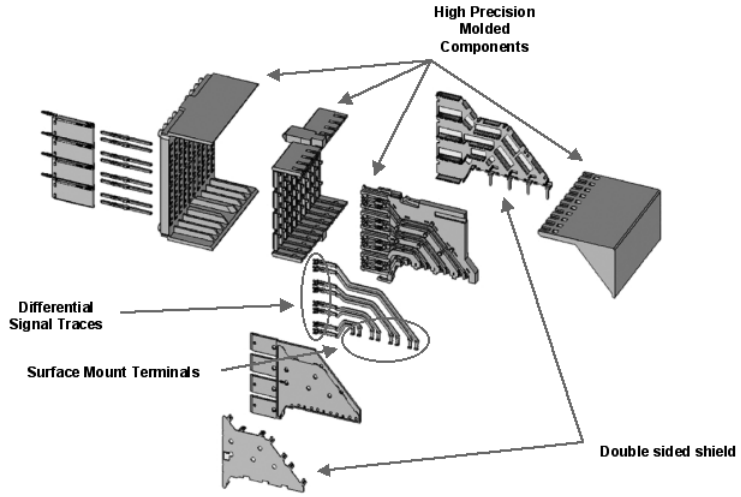
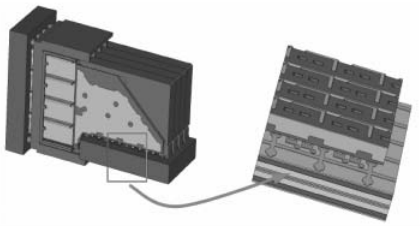


Figure 12. Exploded view of SMT backplane connector.

Designing a surface mount backplane connector has numerous challenges. First, the interface must withstand the mechanical conditions faced by standard board applications and be very rugged. Secondly, the connector must be able to transmit data at speeds exceeding 10 Gb/s. Recent designs of Surface Mount (SMT) backplane connectors have evolved from press fit connector technology including many of the same mechanical features such as the 1.5 mm x 2.5 mm pin grid. The two main differences in the connector designs revolve around the use of SMT signal leads and the 'C-shaped' pin-in-paste ground shield pin. A well designed high speed board to backplane connector integrates the mechanical, chemical, and electrical properties of the device seamlessly . Orientation of differential pairs, spacing of contacts, and selection of component materials all play key roles in the overall performance. It is a challenge to find the proper combination of these design criterion without impacting the signal integrity of the connector. A great deal of time and effort go into the design and modeling of these types of connectors before the first piece of steel is cut. The exploded isometric drawing of the connector in Figure 12 is courtesy of ERNI Corporation GmbH.

It is noteworthy to discuss the overall channel performance from transmitter to receiver within the backplane/daughter card system. A perfectly controlled impedance environment is the ultimate goal which will result in minimal reflections, best frequency response, and higher data rates. A typical source of reflections is thought to be the connectors within a system and this is certainly possible if the connector is being used at a higher data rate than recommended. However, the more likely scenario is this: inside the connector is a well controlled differential transmission line as in Figure 12, but the pcb to connector interface is poorly designed. This area called the "via field" is typically the most critical portion of the channel. It can easily make or break the overall bit error rate performance of the system.

Three Configurations Modeled with ADS



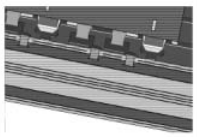
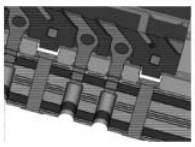
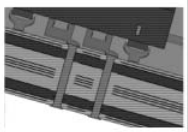
	Setup 1	Setup 2	Setup 3
Zoomed cross section			
Connector pad	SMT	Pressfit	SMT
Via type	Microvia	Throughhole with backdrill	Through hole
Via diameter	0.35	0.5	0.3

Figure 13. Three connector to board interface mechanisms.

The next step is to examine the particular advantages of various connector to board interface mechanisms including microvias, pressfit, and surface mount. The diagrams in Figure 13 show the connector to board interface of a connector receptacle which is soldered to a typical board with 16 layers and an overall thickness of 4mm. Using this realistic assumption, the following three typical configurations will be compared. Looking at the table entries in Figure 11, it can be identified that the selected signal layer is different for setup 3. The reason for this difference is that a connection to a signal layer very close to the bottom of a PCB is typically a non-critical case. This is due to the fact that the remaining stub is very small and the diameter of the via and the antipad can be optimized to achieve good matching behavior. The critical case, however, is the wiring from a connector to one of the upper signal layers in the PCB. Using conventional pressfit or SMT technology would lead to a via stub with a very large length. The very high capacitive load of this stub would result in a significant impedance mismatch which reduces the overall signal quality. This is the reason, why this “worst” case is not taken into account and the two solutions are compared which are currently used to overcome this limitation. One of these options is to apply back drilling to these critical vias while the second one is the implementation of micro via technology.

Characteristic Impedance & Crosstalk

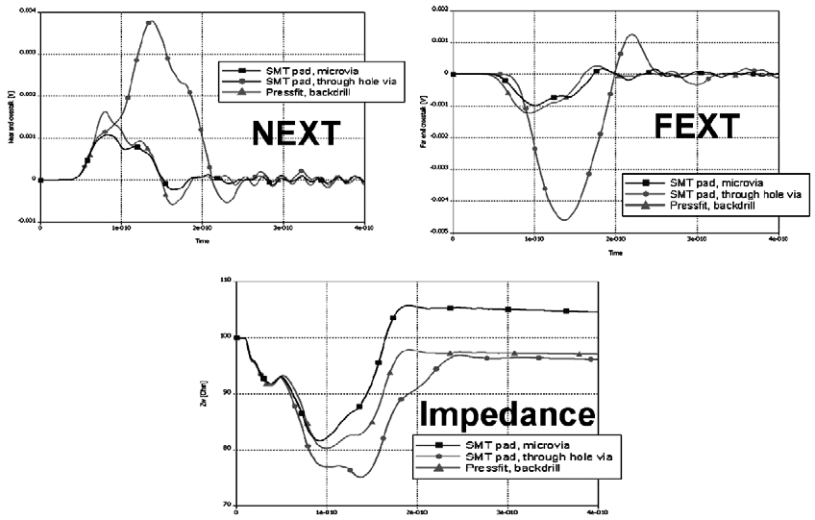


Figure 14. Comparison of the three connector to backplane configurations.

A comparison is done by a simulation in the time domain using a full 3D high frequency field solver, where a step signal with a rise time of 50 ps (20 to 80 %) is applied to the device under test. The differential signal is fed into the remaining part of the connector. Such a waveform is typical for a 10 Gb/s serial transmission. As an outcome of the simulation experiment, the characteristic impedance Z_0 of the system can be evaluated together with near end crosstalk (NEXT) and far end crosstalk (FEXT), as shown in Figure 14. Looking at the impedance mismatch, it is evident that the microvia approach showed the smallest impact on the impedance profile compared to the other two setups. It can be seen that the crosstalk in the relatively short vias of the setups with microvias and backdrilled pressfit connections is much lower compared to the long through hole vias. In both cases (far end crosstalk, near end crosstalk), the microvia approach showed a better crosstalk behavior.

Differential Eye Diagram Analysis

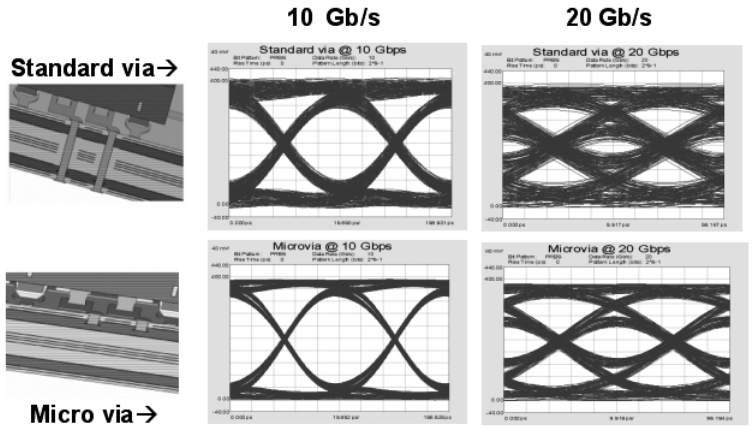


Figure 15a. Standard via and micro via eye diagrams.

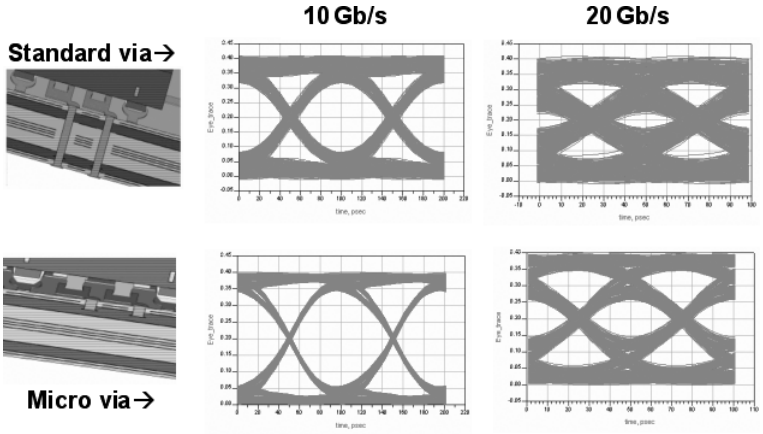


Figure 15b. Very good correlation is shown between PLTS-based eye diagram analysis and ADS-based eye diagram analysis.

The PLTS eye diagrams in Figure 15a are synthesized from the 4-port s-parameters obtained for both standard via and microvia structures in our test vehicles described in Figure 11. PLTS allows multiple views to be compared side by side for ease of use. The eye diagram is synthesized by extracting the impulse response of the backplane from it's s-parameters, then convolving this impulse response with a user programmable arbitrary binary sequence. It is useful to have standard PRBS patterns available for this convolution operation, so PLTS allows a standard PRBS pattern to be used up to a length of 2^{15}-1. This method of creating eye diagrams correlates well with the standard method of compliance testing with a pattern generator and a sampling scope with standard masks. As can be seen in Figures 15a and b, the eye diagrams for the microvia are clearly more open than the standard via, even at 20 Gb/s.

Eye diagram analysis is very useful when characterizing a device for a specific digital protocol. For example, we know that Advanced TCA backplanes need to work well at 10 Gb/s. If the eye is sufficiently open and data transitions don't encroach into a standardized mask, then we say we have compliance to that standard. Another useful way to use eye diagram analysis is determining how much pre-emphasis or equalization is required by the associated silicon SERDES chipsets to provide compliance. It can be seen from Figure 15 that the microvia could work at 20 Gb/s with pre-emphasis or equalization, but most likely the standard via would not.

Simulation through Measured/Simulated S-Parameter Data

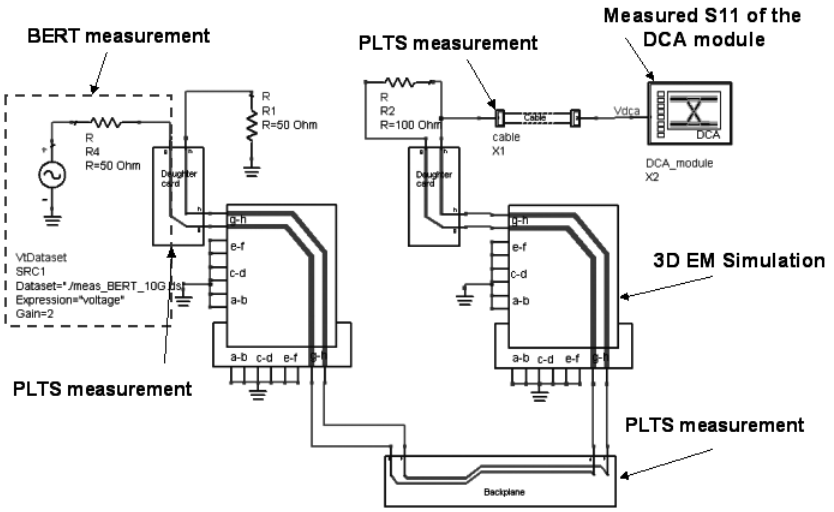


Figure 16. ADS generated schematic.

ADS is an environment for combining models and waveforms from many sources into a single simulation. The ADS schematic shown in Figure 16 describes a simulation environment specifically containing some measurement based models. Measured S-parameter data is used as the model for the backplane (4-port PLTS), the two daughter cards (4-port PLTS), the coaxial cable (2-port VNA) and the DCA module as the load (1-port VNA). The card connectors were modeled as S-parameters using a 3D EM Simulator. The input waveform is a PRBS source from a BERT tester which was captured with the DCA-J and imported into ADS.

Backplane Model Using ADS

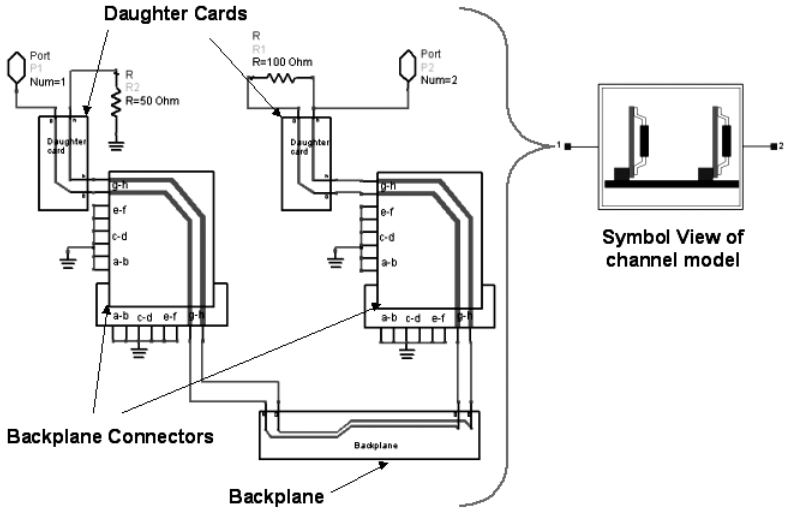


Figure 17. Backplane channel model.

It is necessary to set up the backplane channel model as a subnetwork for use in a system-level simulation. This is done in ADS by adding ports and creating a symbol that represents the whole backplane channel as shown in Figure 17. Note that this complete symbol view is the linear passive interconnect circuit that consists of the daughter cards, backplane connectors, and the backplane itself.

Simulation of Pre-emphasis and Equalization Through Channel Model

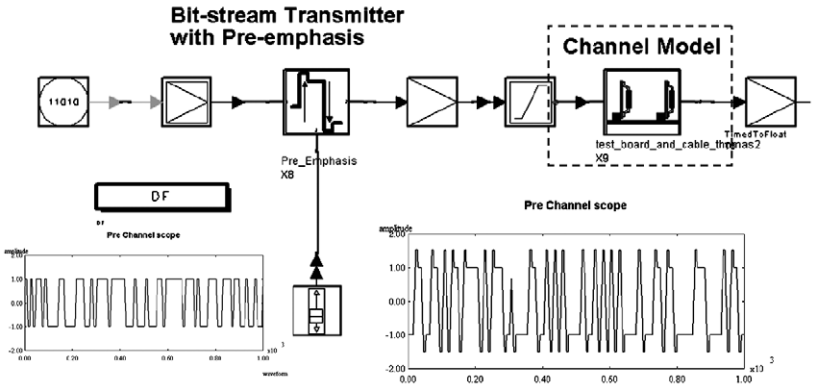


Figure 18. Model with pre-emphasis.

The ADS schematic in Figure 18 shows a Ptolemy co-simulation silicon channel with transmitter pre-emphasis and receiver equalization. It is common practice to utilize transmitter pre-emphasis and/or receiver equalization to improve signal quality of high speed backplanes/channels. This technique will minimize bit errors and open the eye diagram. Through the use of Ptolemy in ADS, designers can study the effectiveness of different pre-emphasis and equalization techniques through the channel model. The plots in Figure 18 show the transmitter waveform before and after pre-emphasis. A slider bar is available in the Ptolemy schematic that controls the amount of pre-emphasis added to the signal prior to going through the channel model. This gives the designer an interactive control to see the effect of different amounts of pre-emphasis and allows optimization of the channel design.

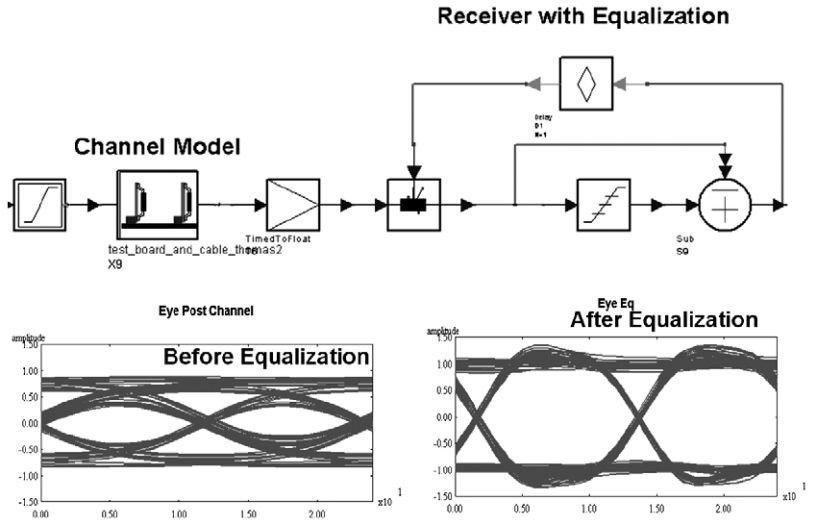


Figure 19. Model with adaptive equalization.

Figure 19 depicts a typical scenario where the receiver applies adaptive equalization after the signal travels through the channel. The EQ in this case is provided by a continuously running Least Mean Square (LMS) equalizer. This could be easily replaced by a Decision Feedback Equalizer (DFE) design. Such a design may already exist in Matlab or as VHDL code. If so this could be included directly through a co-simulation.

ADS Eye Diagram Front Panel

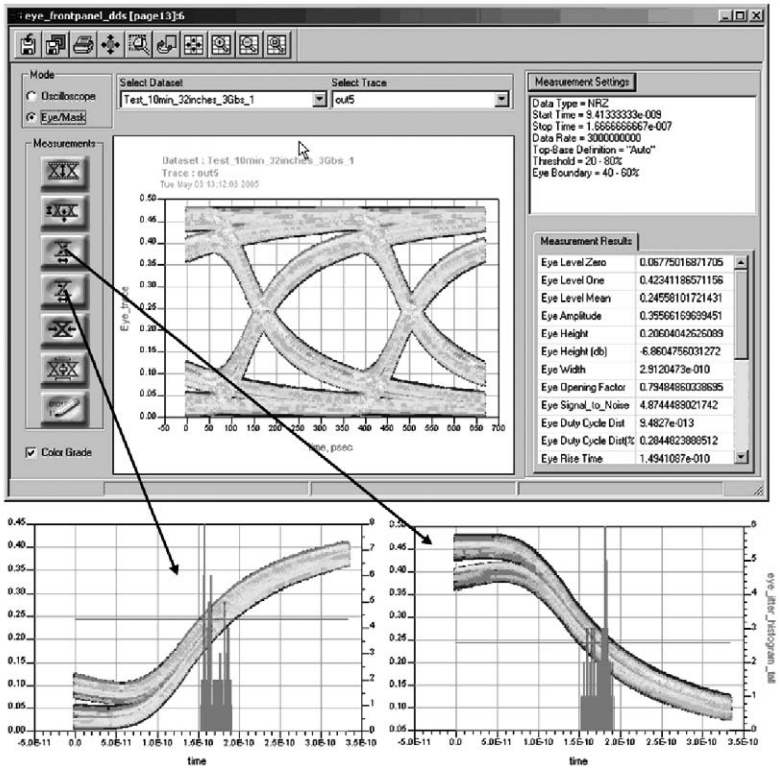


Figure 20. ADS tool showing rise time.

Eye diagram analysis is currently the most common method of assuring compliance to digital protocol standards today. For this reason, this figure of merit is found in both PLTS and ADS tools. The capabilities are complementary and have both been correlated to the industry standard reference receiver, the Agilent 86100C Digital Communications Analyzer. In brief, the eye diagram feature in both tools allows a way to view eye diagrams synthesized from accurate s-parameter measurements. PLTS eye diagrams are simple and easy to set up quickly, while the ADS tool allows advanced automatic measurements such as rise time and fall time parameters shown in Figure 20. In addition, ADS has useful histogram measurements similar to those found on the DCA-J. The eye diagram measurement algorithms are aligned with the DCA-J. This strong link to hardware is a critical factor in avoiding the pitfalls of simulation alone.

Summary

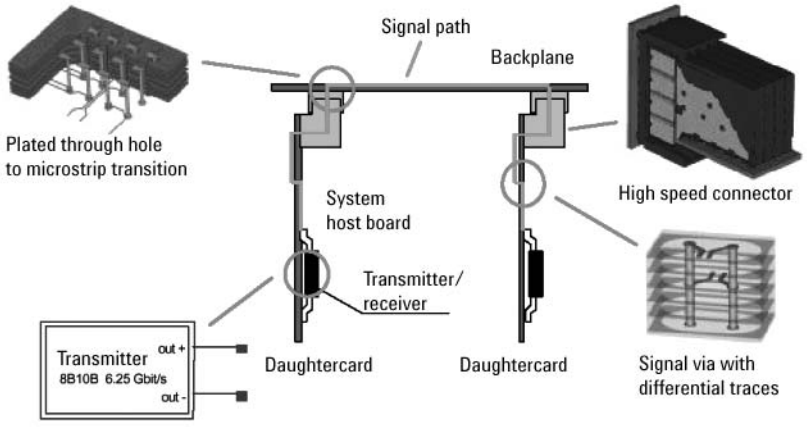


Figure 21. Some of the areas that make backplane packaging a challenge.

Original equipment manufacturers (OEMs) have an endless need for increased system bandwidth, whether for computer servers, mass storage, or internet-supporting equipment such as switches and routers. The backplane packaging challenge for multigigabit transmissions is to maintain attributes such as cost and reliability from a copper backplane while accommodating the signal integrity requirements of passing higher frequency content digital signals. A proven method of building these larger complex systems is to partition the design project into smaller tasks including measurements, modeling, and simulation. Furthermore, a backplane design flow should include both active and passive component design, co-simulation, pre-build verification, prototype build validation, and final test to compliance standard eye diagrams. Measurement-based modeling can save time in the design cycle by eliminating the need to build a model of legacy equipment from scratch. Having the right tools in the signal integrity laboratory will assure success in achieving the best performing backplane and ultimately the fastest telecommunications network. It is imperative that the high speed digital designer have a full understanding of the design tools available today in order to meet these challenges in the future.

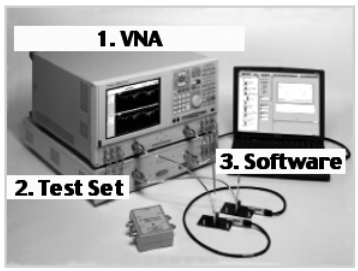
Acknowledgments

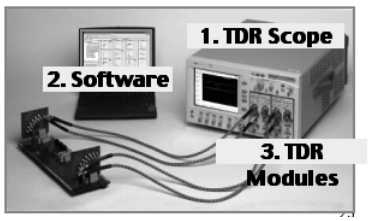
Agilent Technologies would like to acknowledge the work of Dr. Thomas Gneiting of AdMos Technologies in his contribution to this application note.

Configuration and Web Resources

PLTS

Physical Layer Test System
(PLTS) Configurations





PLTS version 3.0

- 4-port 67 GHz system
- One box 4-port 20 GHz (N5230A)
- Advanced file export
- TDR impedance correction
- E-cal support

Website

www.agilent.com/find/plts

Software

- PLTS Analysis Software N1930A
- Advanced Design Software

Hardware

- 4-port 67 GHz VNA-based PLTS
- 4-channel 20 GHz TDR-based PLTS

ADS

ADS 2005A

- ADS Signal Integrity Designer (E9009)
- ADS Signal Integrity Designer Pro (E9010)

Website

- Agilent EEsof EDA home page
  http://eesof.tm.agilent.com
- Signal Integrity Applications and Wireline Applications
  http://eesof.tm.agilent.com/applications/signal_integrity-b.html
  http://eesof.tm.agilent.com/applications/wireline-b.html
- Momentum
  http://eesof.tm.agilent.com/products/e8921a-a.html

ADS Training for Signal Integrity

http://www.agilent.com/find/education

- Signal Integrity Class: N3215A Designing for Signal Integrity with ADS
- Ptolemy training: N3206A

Agilent Partners

- Admos for active and passive model extraction services
  www.admos.com

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

For more information about Agilent Technologies test and measurement products, applications, services, and for a current sales office listing, visit:
www.agilent.com/find/tmdir

Printed in U.S.A. January 18, 2006
5989-4077EN

Agilent Technologies