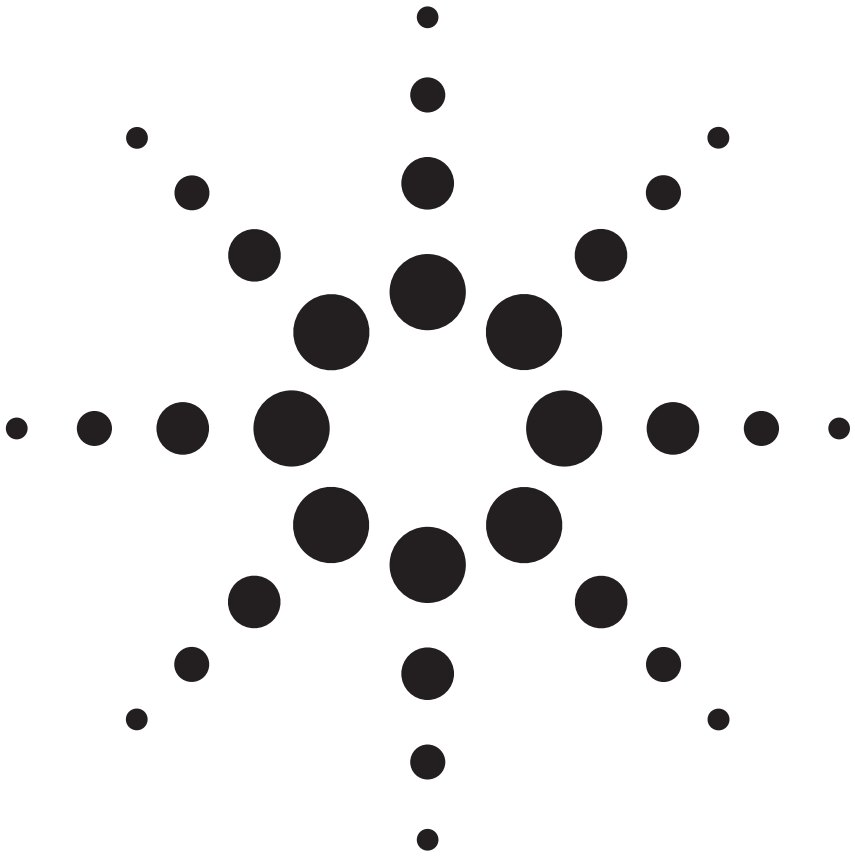
Agilent
Designing Scalable 10G Backplane Interconnect Systems Utilizing Advanced Verification Methodologies

White Paper



Agilent Technologies

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Introduction

The design and implementation of high-speed backplanes requires substantial effort both in pre-prototype modeling and post-prototype testing and measuring. Extant methods for modeling backplane signal paths have become very sophisticated and time consuming. Correspondingly, current test methods for verification of design have relied on direct measurement techniques which are often useful for only a single test condition requiring multiple test runs. This paper presents techniques for design which significantly reduce modeling requirements for the design of high-speed backplanes in conjunction with advanced testing techniques which provide maximum channel characterization with the minimum amount of time.

Companies requiring 10 Gb/s (and higher rates) backplane solutions all face the same challenges of cost, power, scalability and integration. The current standard design approach of embedding backplane SERDES I/O within ASICs, to save cost and extend performance, has been effective for 3G and for some 6G backplanes. At 10G, issues of signal loss due to material, cross-talk and power consumption make it, at best, risky and more costly to pursue the same design and testing approaches as previous generations.

Instead of relying entirely upon electronic enhancements based on SERDES technology, an improvement of channel capability is proposed for the high-speed signals. Multiple benefits are created by improving the channel for high-speed signals. First, materials can be selected which reduce the insertion loss and consequently reduce I/O power requirements. Signal path structures can be optimized to minimize signal distortion thereby further reducing I/O power consumption due to relaxed signal recovery timing requirements. Cross-talk, a major component of signal integrity, can also be significantly minimized contributing to a lowering of overall signal-to-noise considerations in the signal receiver.

Improved channel construction holds the promise of much higher bit rates than a particular design point. For example, a channel which has been improved for use at 10 Gb/s could easily be considered for use at 12, 15 or even 20 Gb/s given the proper I/O electronics. The current methodology for analyzing a channel and its performance is a resource intensive activity given the cost and time associated with test setup and analysis. Projecting the performance of a channel at multiple bit rates is time consuming and arduous when one considers the non-linearities associated with traditional channel construction operating at different frequencies. The idea of a singular design point has also permeated the back end of product design wherein testing and verification has been limited to the intended operating point (e.g. 10 Gb/s).

Given the challenges of 10G design and development, it is clear that an updated test and measuring methodology is needed to take advantage of improved signal channel capability. Performance data collected at a single operating point, while useful, is certainly not efficient when there is need to extrapolate product performance into the future. Thus the approach taken for this project is to expand the test and measurement of the signal channel to include a full characterization of its properties over a 10x range of operating frequencies. The resulting performance data, in the form of S-parameters, is then used to construct performance characteristics from different operating points through the use of accurate modeling transformations. Significant savings in testing are gained since accurate test results (TDR plots and eye-patterns) from different operating points are synthesized conveniently without having to continuously return to a test lab.

Current Design Approaches and Impediments

Powerful evolutionary forces in product design conspire to keep incremental improvement approaches in play for as long as possible to forestall the expense of new technology adoption. Backplane and chassis construction certainly adhere to these conditions and no doubt will continue on into the foreseeable future.

A traditional backplane implementation is shown in Figure 1.

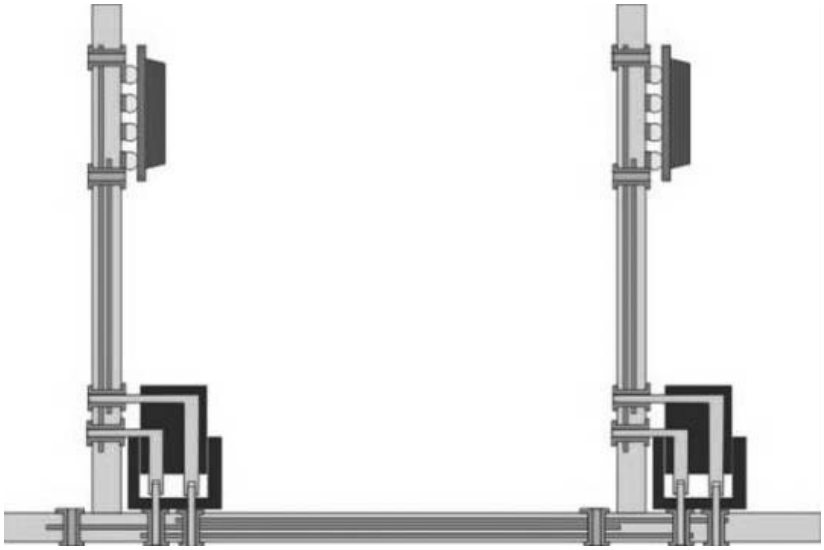

Figure 1. Traditional backplane construction

For many backplane generations, the issues of impedance, loss, signal stubs, lumped parasitics and cost have been in the forefront of design considerations. As bit rates have risen over time, the deleterious effects of the aforementioned elements on the signal quality have increased significantly and so also has I/O circuit design complexity. To combat the increase in signal degradation issues, electrical engineers, along with electro-mechanical engineers have waged independent battles. The electrical engineers have taken advantage of Moore's law by utilizing the ever increasing supply of cheap transistors on a die to serve leading-edge apps in I/O circuits. On the electro-mechanical side of the battle, the designers of connectors and IC packages have incrementally leveraged new material and processes into interconnection elements, that while substantially traditional, perform better at higher speeds.

One set of electromechanical impediments associated with backplane printed circuit boards are summarized in Figure 2.

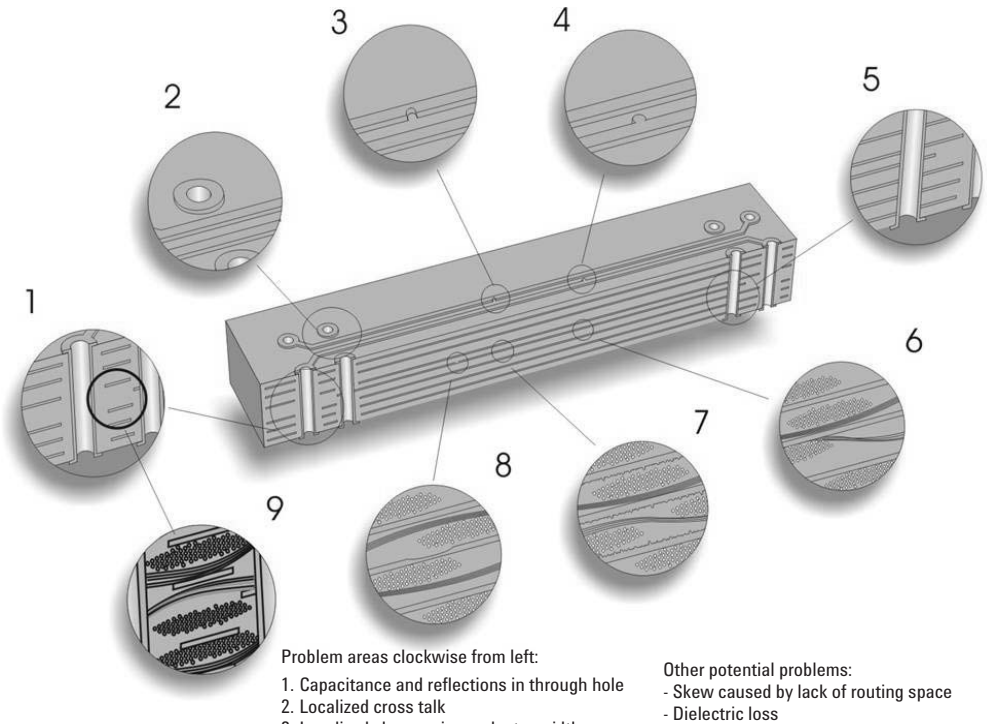

Figure 2. Printed circuit board problems

These printed circuit board and package structures translate directly into signal quality impediments. In particular, the device-to-package solder bump and package-to-board solder ball interfaces are high impedance structures that create impedance compensation difficulties. In addition, signal layer transitions, in both the package and board, needed to route the signal from device to device create significant low and high impedance changes in the signal path.

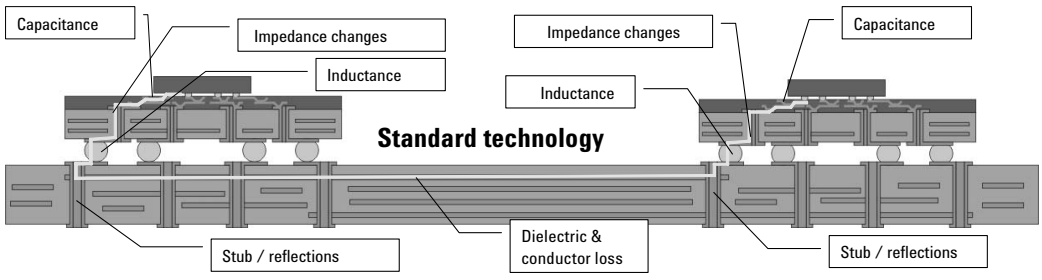

Figure 3. PCB signal integrity impediments

It is not only the structure of printed circuit boards but the type of material which determines the performance capability of a backplane system as illustrated in Figure 4.

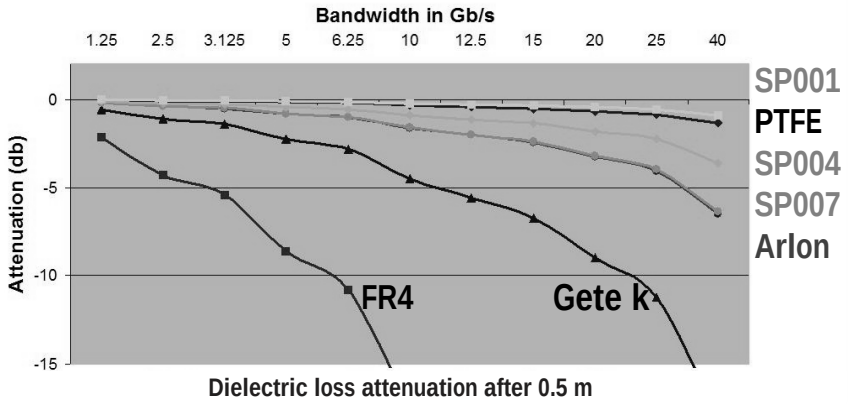

Figure 4. Loss performance for backplane materials

The chart in Figure 4 was generated by plotting the dielectric performance of a variety of commercially available printed circuit board laminate materials. There are many beneficial attributes of FR4 which continue to make it a favorite choice among system designers. Foremost among these attributes are cost and manufacturing familiarity. Unfortunately, the performance of FR4 falls off dramatically as the data rate approaches 10 Gb/s.

It is easy to see how the interconnection elements necessary to implement a 10G backplane create many challenges for the delivery of signals. To overcome signal quality issues, electrical engineers have implemented enhanced I/O electronics.

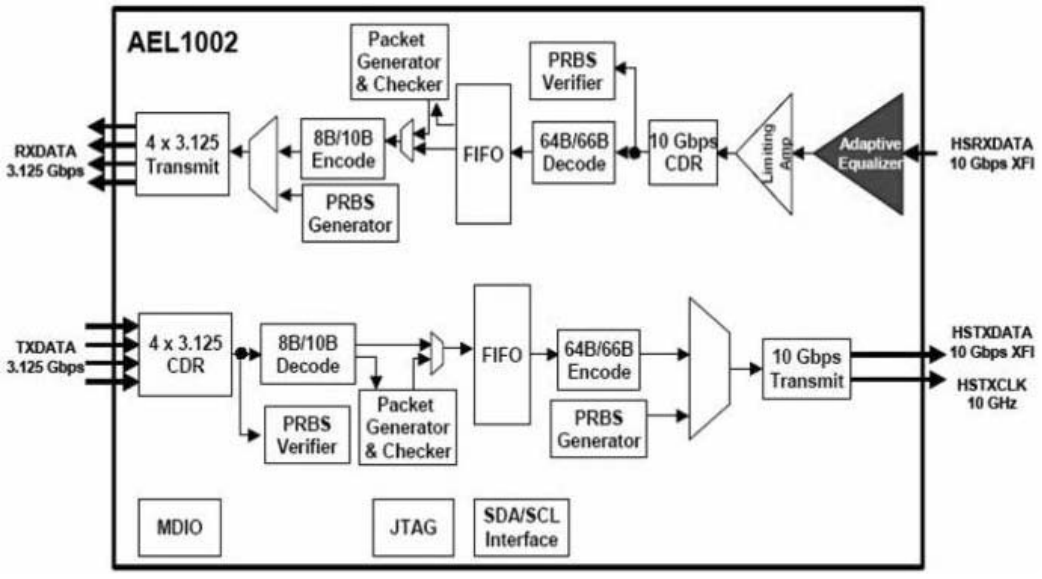

Figure 5. SERializer/DESerializer (SERDES) for 10G signal

Figure 5 illustrates a simplified block diagram of a SERDES designed to transmit and receive 10G signals. The SERDES provides the necessary signal processing to overcome the signal degradation which occurs through the signal channel. In the transmitter, the data stream is encoded using 64B/66B code words to reduce the effects of inter-symbol interference (ISI). In the receiver, a clock/data recovery (CDR) circuit provides the necessary separation of clock from the data while the 64B/66B decoder reconstitutes the original data stream. When the protocol allows, sometimes it is beneficial to encode the digital data with redundant bits of data with intent of adding error detection capability. This way, it is possible to detect certain type of common errors. Although such a scheme adds overhead to the data transmission and usually increases the raw rate of data bits being transmitted, error correction coding can be a very effective way to achieve lower bit error rates. Highlighted in blue in Figure 5 is an implementation of an equalizer to reduce some of the effects of the bandwidth non-linearity of the interconnection channel.

Signal conditioning techniques can be used to compensate the signal degradation due to the channel interconnections. One is to pre-condition the signal at the transmitter. This can be implemented with passive networks or active circuits using linear transversal filters. A linear transversal filter with a pre-determined bit time interval is relatively easy to implement, especially with current mode drivers. For example, most XAUI drivers implement a variable amplitude, one bit delayed tap that is opposite to the main signal bit. Such pre-emphasis has a net effect of reducing the low frequency component of a transmitted signal. Such a scheme effectively reduces the effect of long PCB traces on high-speed signals which attenuates high-frequency components due to skin effect and dielectric loss. The technique can be extended to multiple bits of signal pre-emphasis, and the spacing can be extended to sub-bit times as well.

Another place to implement signal conditioning is at the receiver, as shown in Figure 5. The same linear transversal filter for transmitter pre-emphasis can be implemented at the receiver before the signal slicer. The advantage of having the filter at the receiver is that the receiver can adaptively adjust the filter coefficients without cooperation from transmitter, while the transmitter cannot do so without the prior knowledge of the channel or cooperation from receiver. In addition to a linear transversal filter, the receiver can also use a nonlinear decision-feedback equalizer, which has certain advantages over the linear filter.

There are also other equalizer implementation techniques. A common approach for equalizing cable or PCB loss is a split-path equalizer, in which the signal is split into two paths with different frequency responses. The output signal is a weighted sum of the two signal paths. By adjusting the frequency responses and the weighting ratio, you can achieve a robust equalizer with relatively simple circuitry.

Aeluros 1002 Equalization

The optimal choice of signal conditioning technique strongly depends on the channel as well as the protocol used. In general, the cleaner the signal channel is, the less signal conditioning is required.

Feedback loop equalizes high and low frequency signal components

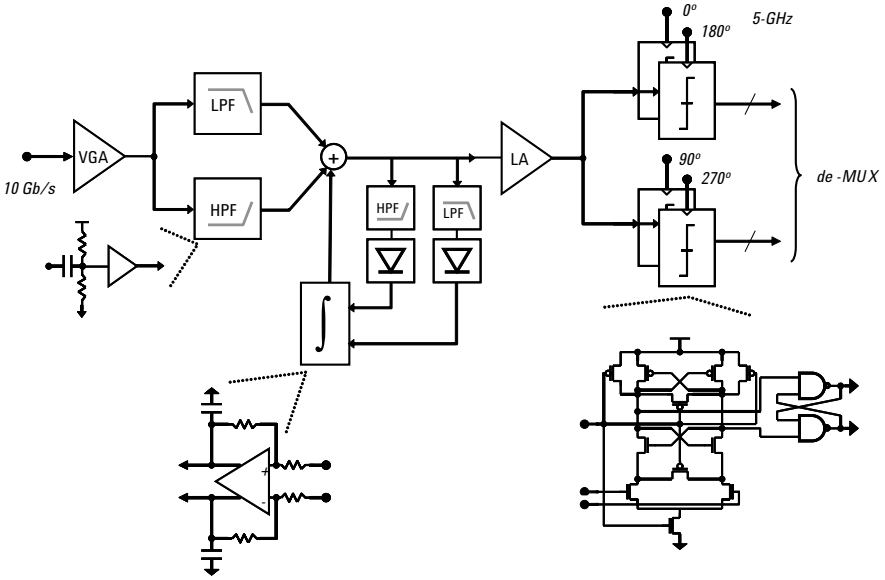

Figure 6. AEL1002 adaptive equalizer

The details of the AEL1002 adaptive receiver side equalizer are shown in Figure 6. The input signal is first amplified with a variable gain amplifier, and split into two signal paths. One with low-pass frequency response and one with high-pass response. By adjusting the ratio between the two signal paths, the circuit can compensate for the frequency-dependent loss introduced by PCB traces. The feedback is carried out with two peak detectors that sense the signal amplitudes at both high and low frequency portions of the combined signal. The goal is to have a relatively flat frequency response before the input circuit (right hand side).

Improving the Channel

As previously noted, powerful status quo forces in product design continue to keep incremental approaches in play for as long as possible to avoid the expense of new interconnection technologies. The electrical engineering design community has successfully addressed the problem so far through their proficiency at creating SERDES technology to address challenges related to interconnection issues. However, the ability of FR4 material to conduct high-speed signals drops off rapidly as the signaling rate climbs above 6 Gb/s (Figure 4). To address this and other signal degradation issues, an alternate channel can be constructed which significantly improves signal transmission characteristics.

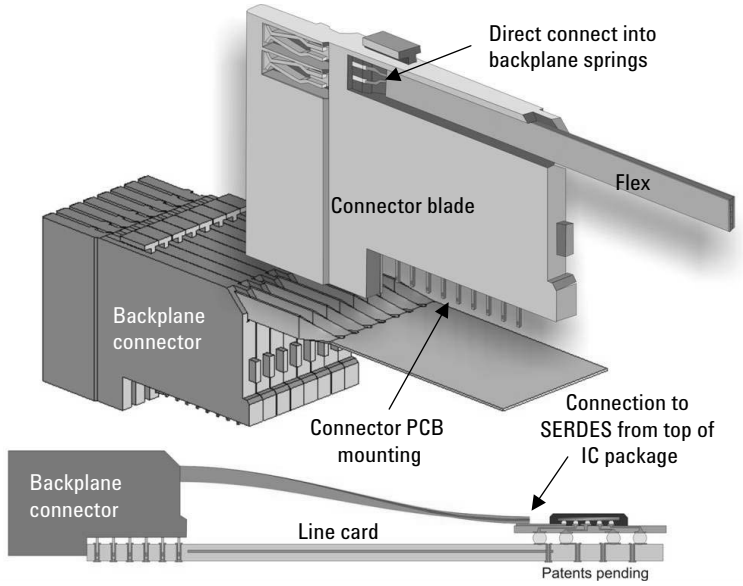

Figure 7. Improving the signal path for high-speed signals

Figure 7 illustrates how a high-speed signal path can be constructed for the separate transmission of high-speed signals from an IC to a backplane connector. As shown, flexible material with significantly better dielectric properties than FR4 (dielectric constant of ~ 4.4) provides reduced channel insertion loss. For this project, a polyimide material with a dielectric constant of 3.4 was used. In addition, the channel can be easily constructed with no through-hole in the signal path thereby providing fewer impedance discontinuities. Through-holes are also a significant source of signal cross talk.

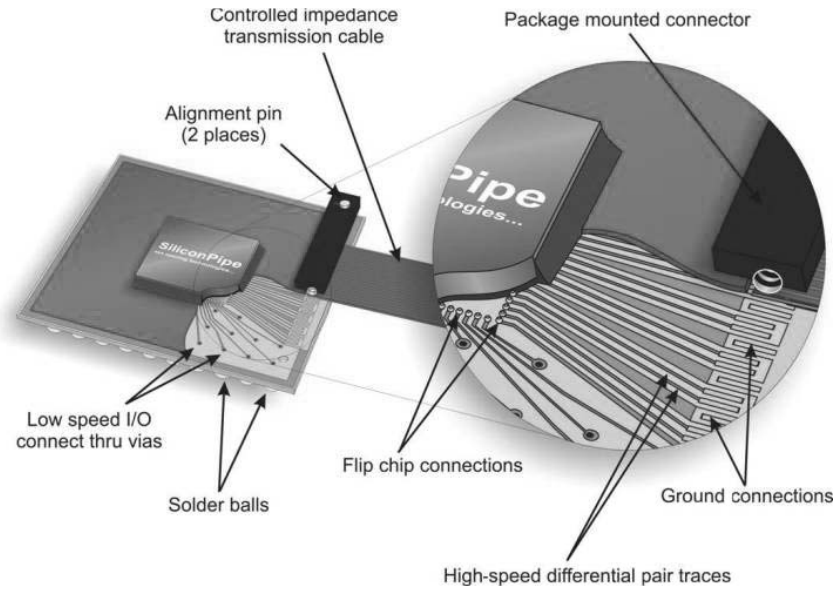

Figure 8. High-speed signal transmission with no through-holes

Figure 8 illustrates how high-speed signals can exit an IC package without the need for through holes. In this particular example, an IC connects into differential pair microstrip signal paths where they are routed to the IC package edge. At the edge of the IC package, a direct contact connector system with controlled impedance flex circuit is utilized to carry the signal further into the system.

The equivalent of a 30" 10G backplane was built utilizing this approach. Components from Aeluros, ERNI and Sanmina-SCI (10G SERDES, backplane connector and backplane) were used in the system.

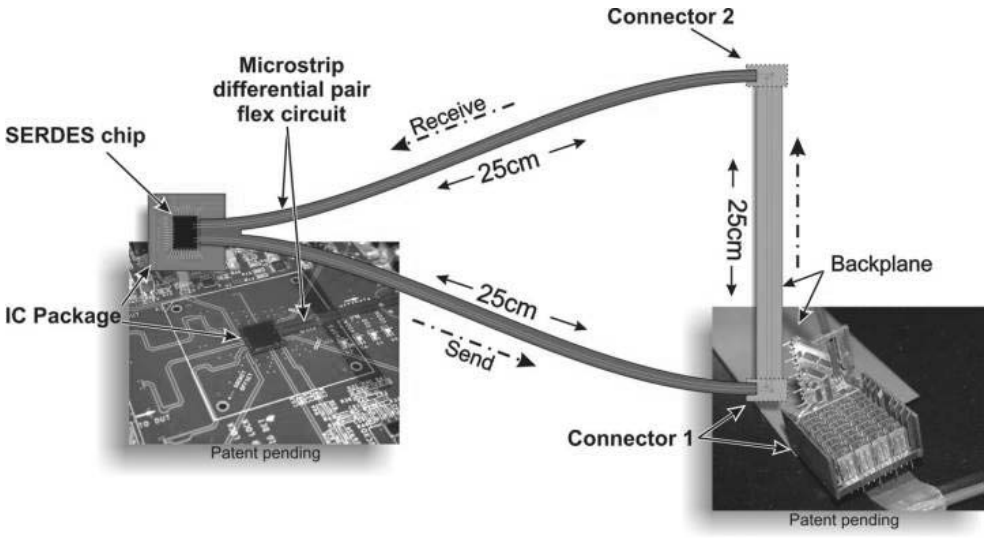

Figure 9. 10G Backplane interconnection system utilizing improved signal channel

A single 10G SERDES (Aeluros AEL1002) was used to provide both the transmitter and receiver for the test. A controlled impedance polyimide flex circuit (fabricated by Altaflex, Santa Clara, CA) was designed to mount onto the AEL1002 IC substrate and provide a direct attach for both transmit and receive differential pairs. The assembly was performed by Nxgen Electronics, San Diego, CA. The flex circuit was designed in a split fashion to allow the receive pair to be separated from the transmit pair at the opposite end of the flex cable. This provided an ability to insert the flex cables at each end of a 10" backplane. The 10" backplane was manufactured by Sanmina/SCI with FR4 except for the microstrip signal layers which were constructed with Rogers material (dielectric constant ~3). At the opposite ends of the flex, standard GBX connector blades (supplied by ERNI) were attached by bypassing the existing signal paths within the ERNI blades (Figure 9). The complete IC/Flex assembly was reflowed onto an Aeluros 10G evaluation board.

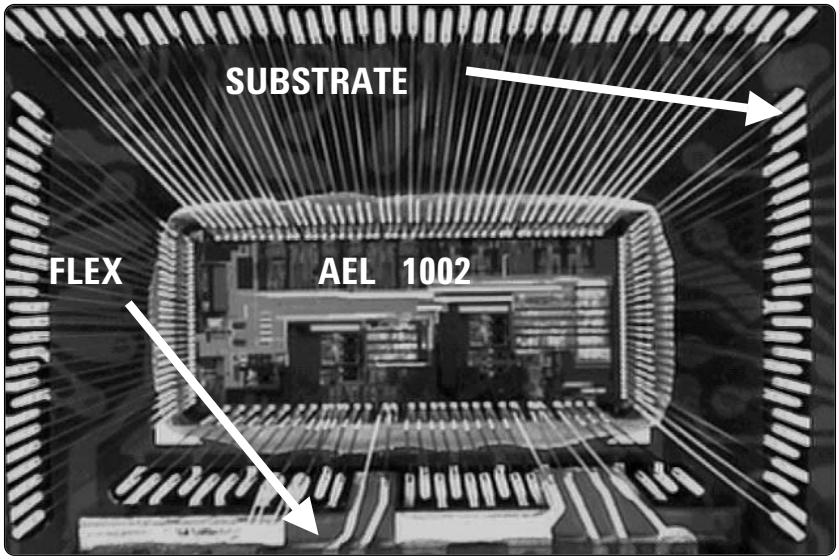

Figure 10. SERDES flexible circuit IC attachment

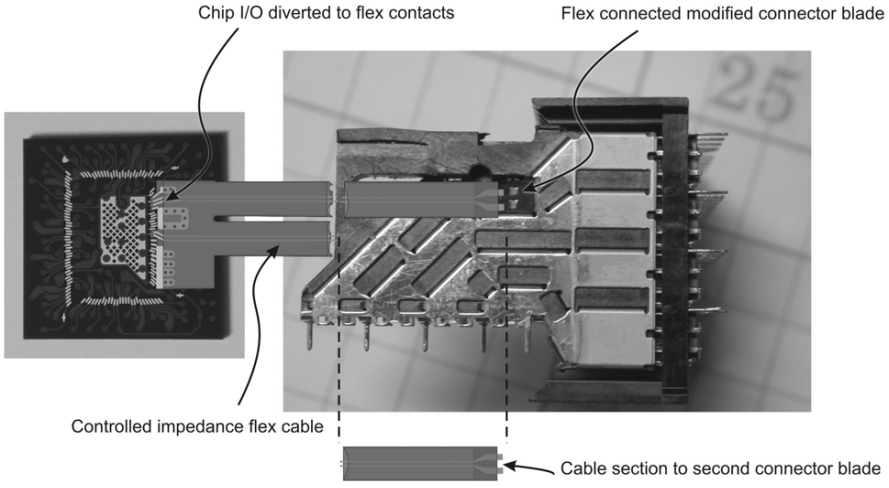

Figure 11. GBX flex blade attachment

The AEL1002 10G SERDES is not designed as a backplane SERDES. The AEL1002 is designed specifically for XFI (a serial 10-Gb/s electrical interface application), in which the chip is used as a bridge chip between an ASIC with an XAUI interface and an XFP optical module. In such applications, the distance between the SERDES chip and the XFP module can be up to 12 inches. The XFP module is an optical module that can be hot-plugged into a system with an XFP connector. The combined effect of the XFP connector and the potential long PCB trace will degrade the 10-Gb/s electrical signal such that signal conditioning is required. The AEL1002 is designed with an adaptive receiver side equalizer to mitigate the variable degrees of PCB loss for 12 inch FR4 signal traces.

The AEL1002, in addition to the required functionality of providing 10G signal processing also provides many test features that help reduce device testing time, and are useful for system performance analysis. Extensive PRBS (pseudo random bit sequence) and 10 Gigabit Ethernet packet generation and checking are included. On the parametric side, the transmitter incorporates programmable amplitude adjustment and the receiver timing is adjustable for checking the timing margins of the signal link.

In this demonstration application, the backplane test environment consisted of a total signal path length of 30” with 2 industry standard backplane connectors.

Initial Functional Testing

No attempt was made by the design team to determine, in advance through modeling, the capability of the test system. We anticipated a significant improvement in insertion loss and signal quality at a qualitative level from the use of the controlled impedance flex circuits and the elimination of through-holes in the signal path. Owing to the test features of the AEL1002, it was possible to implement the test system and determine general performance capability without the use of signal path test equipment. Instead, the use of a laptop computer provided the operating test results through the test features built into the AEL1002.

During initial system bring up, operating performance was observed at 10 Gb/s with 800 mVp-p driver signal strength through the Aeluros evaluation board software running on a laptop. Through the Aeluros evaluation board software, the test team was quickly able to adjust the operating conditions of the system and determined that the system operated with 60% receiver timing margin even at 100mVp-p driver strength. Unfortunately, the driver signal strength could not be adjusted down further to explore the boundaries of the operating margin for the system. The performance of the system surpassed expectations of the design team given no prior analysis had been performed.

Full System Analysis

While the operating results exceeded performance at 10G data rates by a wide margin, it was unknown as to why the system performed as well as it did. A thorough analysis was needed to understand and corroborate overall performance.

A full measurement of the 30” backplane system was performed to assess the system’s overall performance and data rate scalability for all bit rates, not just 10G. Unlike the traditional approach of using a TDR oscilloscope to measure the performance of the channel at a set rise time corresponding to, for example 10G, the team chose a new measurement methodology which made it possible to evaluate the performance of the system at any bit rate between 100 Mbps and 25 Gb/s, even months after the test fixtures have been removed.

Measurements were provided by GigaTest Labs and Agilent Technologies using a 4-port network analyzer and micro-probing equipment. Since a complete differential channel characterization was required for validation of the interconnection channel, the Agilent N1930A physical layer test system (PLTS) software was used as the calibration, measurement and analysis tool. A single connection of four cables (two input and two output) yields all 16 differential and mixed mode s-parameters, including differential insertion loss (SDD21). This measurement system allows extremely accurate, repeatable S-parameter data to be taken on a wide range of differential interconnect devices. For this measurement, 4-port single-ended and 2-port mixed-mode S-parameters were taken on the 30” channel in 25 MHz increments through 25 GHz. The resulting dataset of S-parameters for the channel allowed for the accurate synthesis of single-ended as well as differential and common mode channel performance (TDR plots and eye diagrams).

Figure 12. High precision/high frequency probe station (GigaTest probe station)

Equipment used:

- GTL-4060 probe station
- 26 GHz coaxial cables (3.5-mm SMA-compatible connectors)
- Agilent Technologies 8364B vector network analyzer (50 GHz) with 4-port test set
- GGB 40A-GS/SG/GSG-450-DP probes with CS-11 calibration substrate
- Agilent advanced design system software (ADS 2003C)
- Agilent N1930A physical layer test system software (PLTS)

Vector network analyzer (VNA) settings:

- Start frequency: 25 MHz
- Stop frequency: 25 GHz
- Frequency steps: 25 MHz
- Input power: 0 dBm (equivalent to 0.6Vp-p into 50 Ω)
- Calibration kit: CK11450, SOLT style

Measurement of the channel required the use of a flex cable assembly without the AEL1002 SERDES IC. Instead of the AEL1002 driving to and receiving from the flex, the IC was replaced by probes connected into the test equipment.

Generating accurate channel measurements of the interconnection channel demanded the use of accurately positioned, high-performance microprobes. Figure 13 shows a photograph of the end of the flex cable designed to connect into the SERDES. The SERDES is not attached. Instead, differential probes, with grounds, are positioned to make contact to the flex in the same area where wire bonds from the SERDES would be positioned.

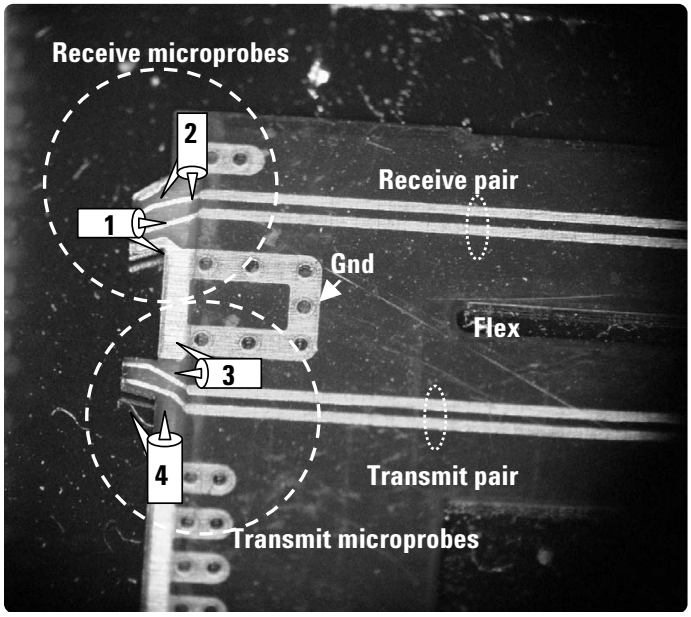

Figure 13. Flex cable probe locations

The overall view of the flex assembly and backplane as positioned on the probe station is shown in Figure 14.

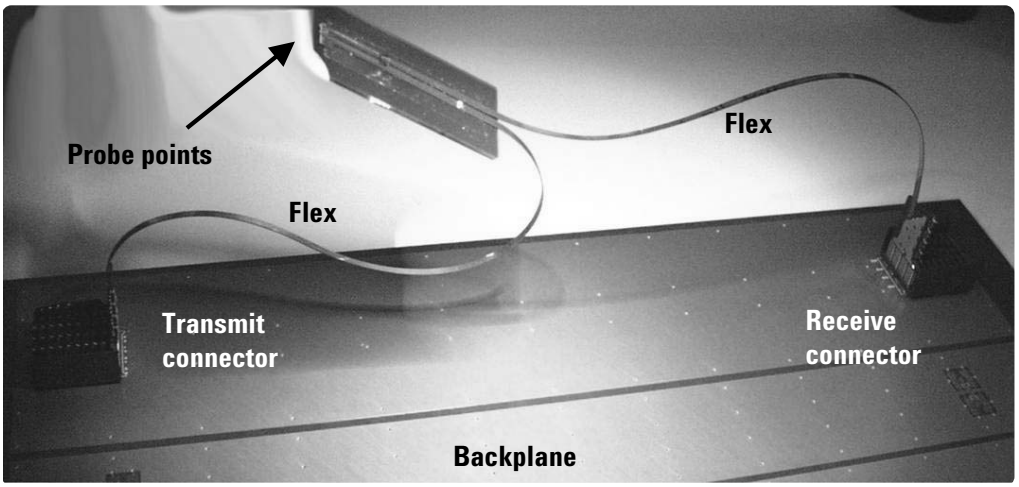

Figure 14. Flex and backplane setup for probe (GigaTest probe station)

The full interconnect assembly can be seen in Figure 14 being readied for the micro-probes. S-parameter data was taken for the system between 25 MHz and 25 GHz in 25 MHz increments. This data was captured using 4-port characterization with Agilent's PLTS software.

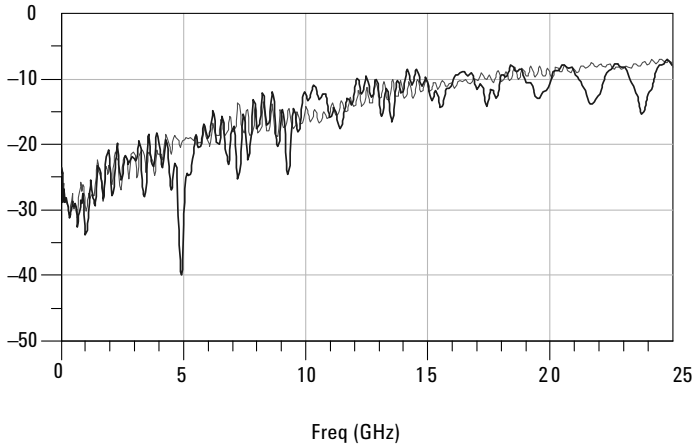

Figure 15. VNA differential reflection test results

The SDD11, differential return loss data is shown in Figure 15. This data shows the return loss to be better than –10 dB up to about 15 GHz. The notch at 5 GHz is the result of series capacitors (DC blocking) in the flex approximately 2” from the AEL1002.

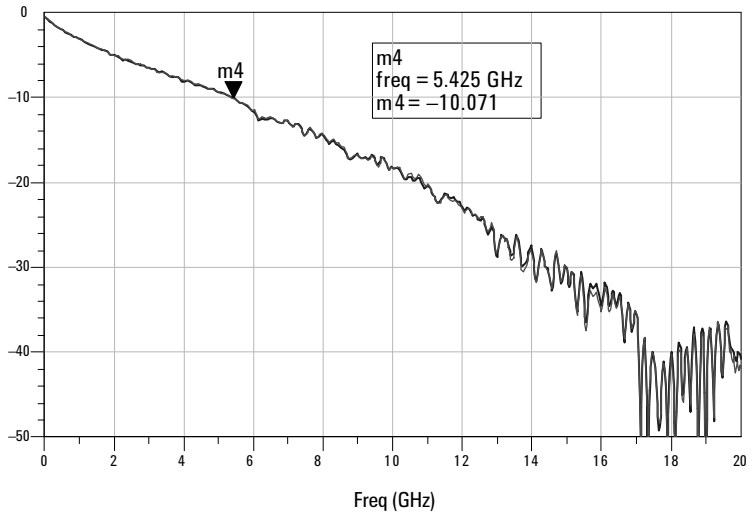

Figure 16. VNA Differential Attenuation Test Results

SDD21, differential signal attenuation is shown in Figure 16. Note the excellent linearity of the frequency response up to 16 GHz. This linearity improves the effectiveness of frequency compensation by the Aeluros equalizer.

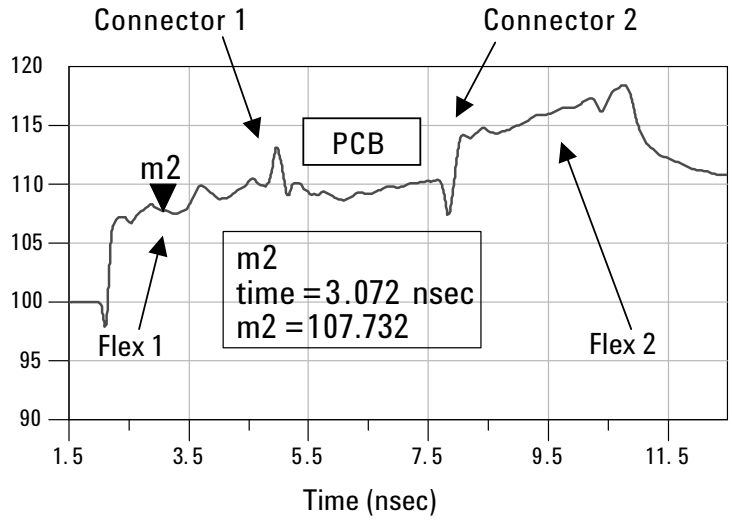

Figure 17. Differential impedance generated from S-Parameters

Differential TDR plot generated from the S-parameters shows the impedance in the interconnect channel. The impedance through the flex is approximately within the 100 Ohm ±10% specification.

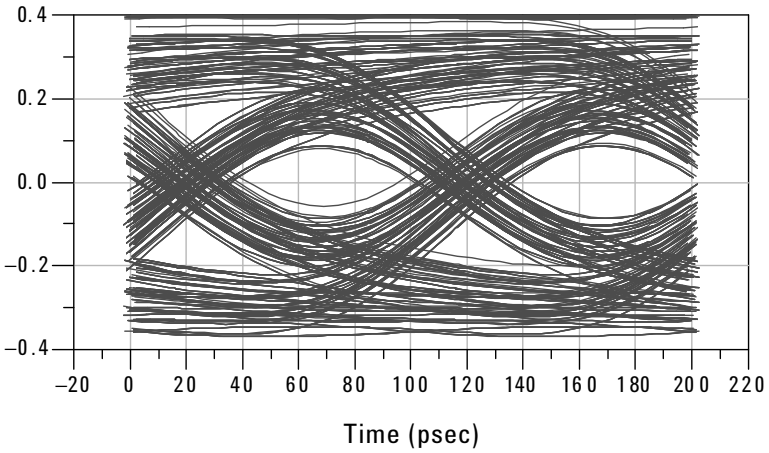

Figure 18. 10G eye with single pole pre-emphasis (10 Ω , 20pF) generated from S-parameters

A powerful advantage of S-parameter test methodology is that it gives test engineers the ability to generate “what if” scenarios for different design points. Figure 18 is an eye diagram generated for the test system channel at 10 Gb/s using a driver rise time of 25 picoseconds, wire-bond parasitics of 0.7 nH and 0.l3 pF, and a single pole 10 Ω , 20 pF pre-emphasis filter. The driver, wire-bond and filter model can each be independently manipulated to ascertain overall system performance without resorting to test bench setup changes.

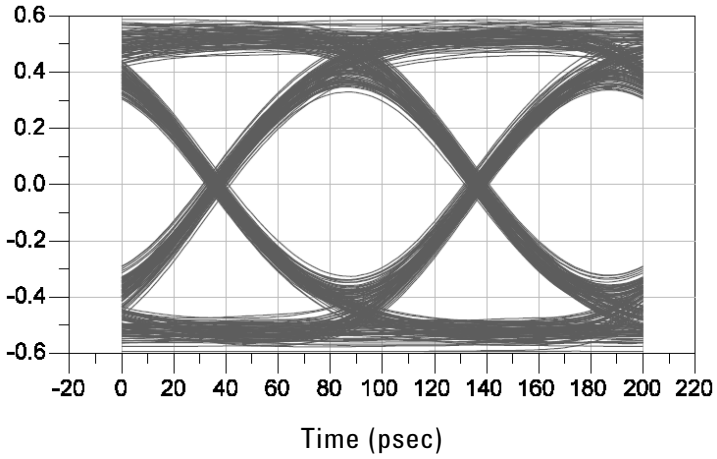

Figure 19. Simulated 10G eye diagram after AEL1002 adaptive filter

Figure 19 illustrates what the 10G eye diagram looks like within the AEL1002 at the input to the signal circuits. This eye diagram was generated from the same S-parameter data which generated the eye diagram in Figure 18. Clearly, the adaptive ability of the AEL1002 provides for much better overall performance and opens the door for increased bit rate operation.

Although the receiver equalizer is designed for XFI channels with 12 inches of FR4 trace and a high quality edge connector, it had no problem equalizing a backplane link with 30 inches of traces and two backplane connectors. This is the benefit of a clean channel construction. The simulated timing degradation due to the channel and the adaptive equalizer is around 10 ps. Using the built-in timing margin capability, the system timing margin is measured to be around 60% unit interval (UI). This is consistent with 70-75% UI timing margin measured with a clean back-to-back connection. In addition, since the channel has a very clean and well behaved insertion loss up to 20 GHz, it is expected that with a similar but extended receiver equalizer, it should be able to handle up to 20 Gb/s without difficulty.

Summary

The goal of building a 10G backplane interconnection system which minimized signal loss and distortion was achieved. The performance of the system was observed with actual signal transmissions in addition to being verified through a thorough channel test methodology utilizing S-parameters generated by the industry leading test equipment. Overall, the performance of the system was above the expectations of the team involved with the project. The goal of building a 10G backplane interconnection system which minimized signal loss and distortion was achieved. The performance of the system was observed with actual signal transmissions in addition to being verified by a thorough channel test methodology utilizing S-parameters generated by industry leading test equipment. Overall, the performance of the system was above expectation for the team involved with the project. The test methodology of using S-parameters was validated and resulted in much less engineering test effort to determine channel performance.

The project did not provide an assessment of several aspects of the new interconnection approach insofar as multiple signal paths (cross talk), manufacturing process, manufacturing costs, design and test costs, or overall usability in future backplane implementations. The authors believe that each of these issues, while important and relevant to the overall decision to adopt a new interconnection approach, will be shown to be acceptable and in-line with modern product design objectives.

Several intangible and unforeseen benefits presented themselves as a result of pursuing this project. The most celebrated of the benefits among the group was the savings in engineering time and cost needed to design high-speed systems. The trend in electronic product design has been to solicit and utilize increasingly sophisticated design tools and experts in order to implement seemingly complex high-speed designs. Unlike product designs of 20 years ago when signal integrity was tantamount to a Schottky clamping diode on an input, today's digital designers are beholden to by a wide range of tools and analysts making sure that the off-IC signals arrive at their destinations properly. With a cleaner channel, the time and cost of such analysis is eliminated or significantly reduced thereby speeding up product design and lowering product risk.

The second benefit learned by the team was that I/O power for high-speed signals can be significantly reduced and consequently relax the overall system power requirements. Upwards of 20% of an IC's power consumption can be attributed to processing needed to handle high-speed I/O. In particular, p..... (PLL) designed for clock/data separation can consume large amounts of power to achieve fine timing accuracy. This project indicated that an eight-fold reduction in driver voltage is possible for high-speed signals; this implies large system-wide power savings.

A compelling conclusion as a result of pursuing this project is the predicted performance of a backplane solution below 10 Gb/s. With the S-parameter data available up to 25 GHz, and a correlated result of the system at 10 Gb/s, an eye diagram for 5 Gb/s is presented in Figure 20.

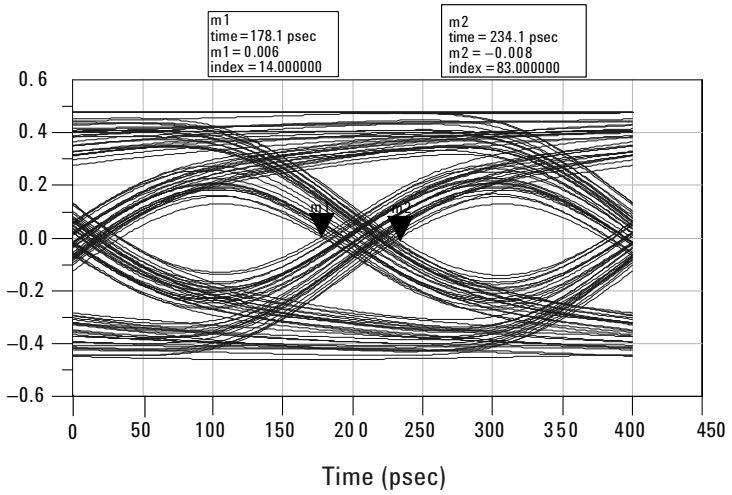

Figure 20. Eye diagram for 5G backplane

The 5 Gb/s eye-diagram in Figure 20 tells us that interconnection systems based upon clean signal channels can be constructed with simplified I/O electronics. The eye diagram in Figure 20 has no transmitter pre-compensation or receiver adaptive equalization included! Given the openness of the received eye-pattern, one can conclude that simple digital I/O techniques are possible well beyond today's design guidelines.

Acknowledgements

The project was made possible through the combined personnel, equipment and manufacturing contributions of the following companies:

Backplane – **Sanmina-SCI (http://www.sanminasci.com)**
SERDES and Evaluation System – **Aeluros (http://www.aeluros.com)**
Flex Cable – **AltaFlex (http://www.altaflex.com)**
Micro probing and Test Analysis – **Gigatest (http://www.gigatest.com)**
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Assembly – **NxtGen Electronics (http://www.nxgenelect.com)**
Connectors – **ERNI (http://www.erni.com)**
System – **SiliconPipe (http://www.sipipe.com)**

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Mr. Grundy is CEO at SiliconPipe. With more than 25 years of experience in reducing complex systems into semiconductor circuits, Mr. Grundy is a seasoned electronics industry executive. Mr. Grundy is also an innovator, noted not only for his many diverse patents, but also for his ability to create and manage an environment where high volume and high quality products are successfully brought to market.

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Haw-Jyh Liaw is Director of System Engineering, at Aeluros Inc. His professional interest includes simulation, measurement, and system level design of high speed interconnects.

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Gary Otonari is the Engineering Project Manager at GigaTest Labs. He is an expert in the use of high frequency EDA software tools, and signal integrity measurement techniques.

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