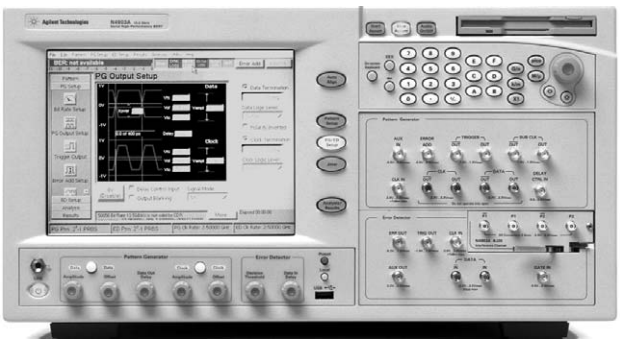
Calibrated Jitter, Jitter Tolerance Test and Jitter Laboratory with the Agilent J-BERT N4903A

Application Note

Quick and accurate characterization of gigabit devices with complete jitter-tolerance testing

The next generation of high-speed serial bus stadards, with data rates of 5 Gb/s and higher, will become available in 2006. The increasing speeds create significant signal integrity and jitter issues for design and test. New transmission techniques are also making performance characterization more difficult and time-consuming. The Agilent N4903A high-performance serial Bit Error Ratio Tester (BERT) provides the only complete jitter-tolerance test solution for fast, high-quality characterization of next-generation serial devices. The jitter laboratory shows the BERT is a reliable instrument for creating and measuring jitter. In some circumstances the RJ/DJ separation based on Dual Dirac Method over-extrapolates the RJ, thus the DJ is too small. But the total jitter reading remains accurate.



The new N4903A is the smartest characterization solution for emerging serial gigabit devices: it helps engineers make quick and accurate jitter tolerance tests, which have been complicated and hard to do in the past. The jitter sources cover the needs for compliance testing to the most popular standards.

Agilent Technologies

The Agilent N4903A high-performance serial BERT offers calibrated jitter composition and automated jitter characterization in a single box and is compliant with the latest serial bus standards. This simplifies stressed eye testing of receivers significantly, while increasing measurement performance.

Figure 1 shows the high-speed market segments and technologies the Agilent N4903A high-performance serial BERT, also known as the J-BERT, can address. In the computing segment there is the Fully Buffered DIMM (FBD), Serial ATA (SATA) and PCI Express (PCIe). In Storage Area Networking (SAN) it is Fibre Channel (FC). In the network segment this is the Common Electrical Interface (CEI) for backplanes, the Passive Optical Network (PON) and 10GbE

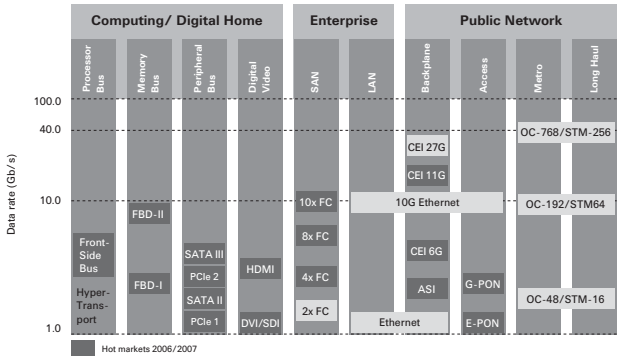


Figure 1: High-speed market segments and technologies

Trends in the High-Speed Serial Communications

Serial busses are becoming mainstream. As data rates go to 3, 5, 6 Gb/s and beyond, the technical challenges increase disproportionately.

- PCI Express at 2.5 Gb/s moves to 5 Gb/s
- SATA/SAS at 1.5, moves to 3 and 6 Gb/s
- FBD at 4.8 Gb/s going to 9.8 Gb/s
- CEI defining tests for 6 and 11 Gb/s
- External communications for computers
- Various Ethernet standards to 10 Gb/s
- Fibre Channel to 8 Gb/s

Physical layer testing trends

Physical layer testing puts a heavy burden on R&D to get it right, first time. The interdependencies mean this takes expertise on the entire system (transmitter/channel/receiver). Change in one area must be validated throughout. The tools available to the typical digital engineer cannot keep up. The jitter tests required are particularly time-consuming and complex.

The new communications system

Today's busses should be viewed as a communications system, even though spans are measured in inches or centimeters. It is not just chips connected to chips, it is a transmitter talking to a receiver over an imperfect channel. While the transmitter and receiver circuits got faster over time, the media or the channel did not.

Low-cost channels become channel involving loss and dispersive

The channel is the trace on the PC board. FR4 material has been used for decades for low cost PC Boards. At Gigabit speeds the material gets channel involving loss and dispersive. The loss causes jitter and can close the eyes. The loss is disproportionate to the frequency, so doubling the speed can cause serious eye closure, quadrupling the speed can close the eye totally (see figure 2).

Therefore a channel needs accurate characterization for impedance and transmission characteristics, including equalization and interactions with the transmitter and receiver. Only a time-domain reflectometer (TDR) oscilloscope and vector network analyzer (VNA) can characterize the channel. The interaction analysis is explored using the PRBS s-parameters, which takes a pattern generator and an oscilloscope.

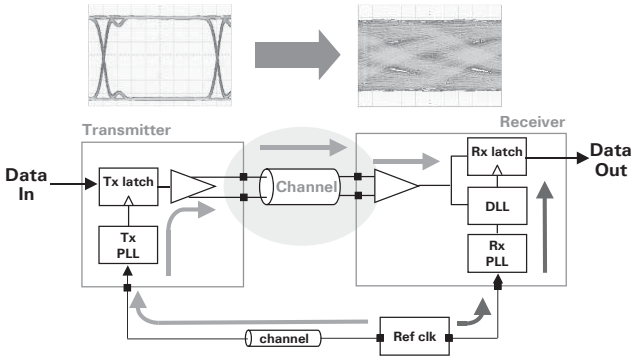


Figure 2: Low-cost channels involve loss and dispersion

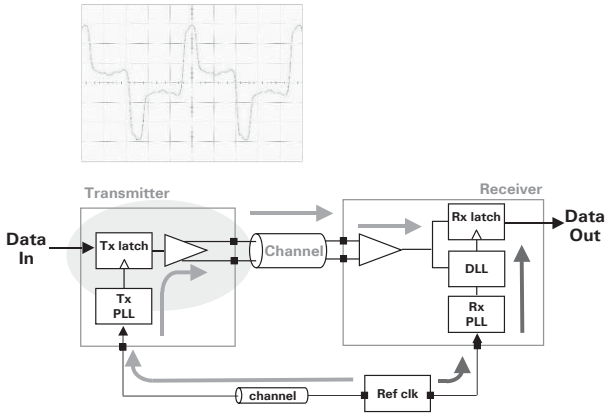


Figure 3: Transmitters must compensate for low-cost cables and boards

Transmitters must compensate for low-cost cables and boards
The method applied is called pre- or de-emphasis. This works by boosting signal amplitude for a transition (pre-emphasis) or reducing the amplitude when the bit stays constant for two or more consecutive cycles (de-emphasis). This needs thorough signal analysis (signal against channel performance) with precision waveform characterization for compliance (for an example, see Figure 3).

Receivers must tolerate degraded signals
"Impaired data streams" are needed to verify receiver robustness. Calibrated composition of various types of jitter (RJ, PJ, BUJ, ISI, SI) create such real-world stress conditions. BERTs offering complete jitter tolerance test capabilities in one box provide an opportunity to reduce the complexity of the test setup and to automate testing. An oscilloscope can verify the stress level, and analyze the waveform for any bit pattern.

Receiver testing needs known bit patterns. A pattern generator creates this stress signal, and the BERT error detector verifies against this pattern. Only by comparing the two bit sequences for differences (errors) the receiver performance can be deduced.

The most neglected topic: the receiver input - Why and where to use the BERT!
At speeds below the gigabit range it is enough to check the transmitter performance using waveform analysis. If this is satisfactory, conect to the receiver and perform a functional test.

In the gigabit speed range, the receiver performance becomes critical due to eye closure on the channel. The receiver needs to be characterized for the robustness with which it can cope with the various jitter components (see figure 5).

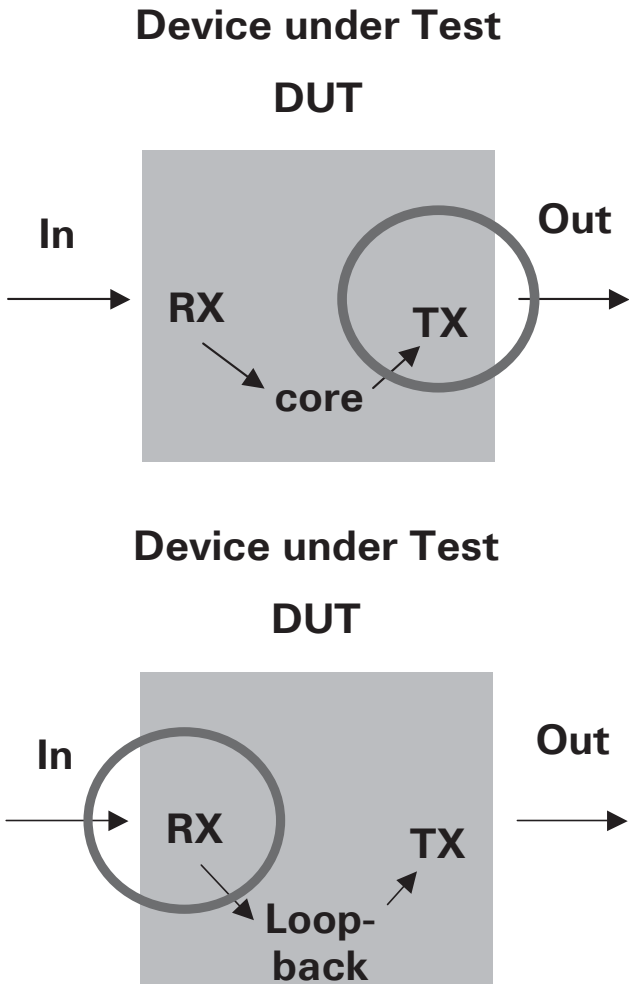


Figure 4: The most neglected topic: the receiver input. Use the BERT for receiver testing

Summary

Transmitter Test
Stimulate with any pattern generator or built-in BIST. Measure with an oscilloscope (real-time, sampler) or BERT analyzer (for total jitter (TJ) measurement).

Receiver Test
Stimulate with the BERT generator (any generator with jitter capabilities). Analyze with BERT analyzer, compare bits against the generator bit stream and count the errors.

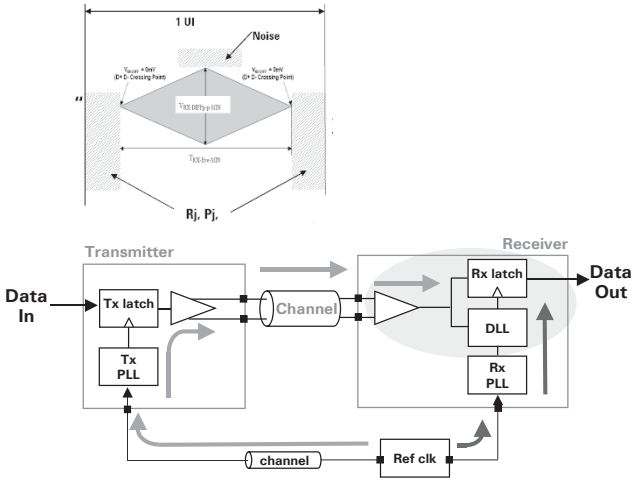


Figure 5: Receivers must tolerate degraded signals

Receiver (RX) Specification According to Standards

The receiver specification is based on three methods: 1st: Compliance eye diagram 2nd: Jitter tolerance curve 3rd: Dynamic voltage range.

Compliance eye

The compliance eye diagram in figure 6 is taken from Second Generation PCI Express® specification [1]. Such a description appears in every standard, but the naming may be different (for example, it may be called the eye mask). In essence it is a description for a minimum eye-opening in time (T_{rx_eye}) and voltage (V_{rx_eye}) that ensures the receiver works properly. In this case, for example, there should be less than 1e-12 sampling errors.

Jitter tolerance curve

The jitter tolerance curve in figure 7 is taken from the 10Gb standard (802.3ae, XAUI) [2], where it is called the sinusoidal jitter mask. Such curves appear in many, but not all standards, though the parameters are different for each. The goal of such a jitter mask is to ensure a margin for all frequency jitter, wander, noise, crosstalk and other variable system effects. Under these conditions a receive circuitry should run properly at a low BER (often 1e-12 or lower).

The jitter tolerance curve defines two different areas

In-band jitter

In this case the PLL or CDR is able to follow the jitter, thus compensating for the jitter. This jitter does not contribute to the jitter budget. The tolerance curve can define a high number of UI's for low frequencies.

Outband jitter

these jitter components are beyond the bandwidth of the PLL or CDR. They cause eye closure and are therefore critical for the BER performance. They need to be evaluated with special care. Apart from a sinusoidal part, the total out-band jitter can be comprised of random and further deterministic components. In case of XAUI, the deterministic content should be at most .37UI ISI and .18UI random jitter on top of the .1UI sinusoidal jitter. This adds up to .65UI total jitter. So an XAUI receiver has to work properly with only 112 ps eye-opening within the 320 ps data cycle (unit interval).

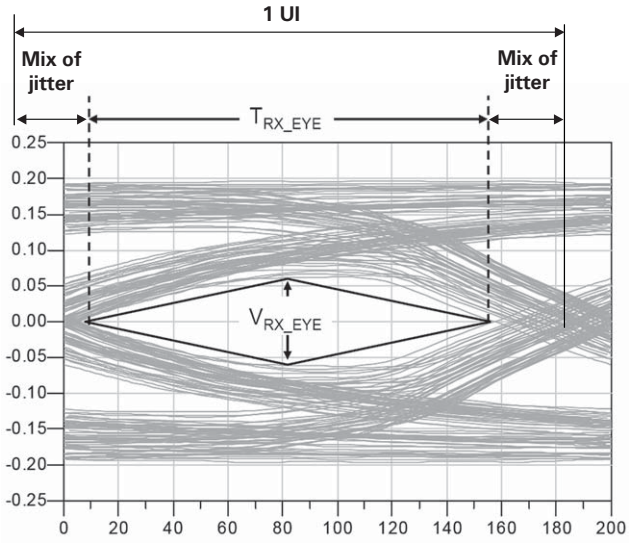


Figure 6: Compliance eye diagram

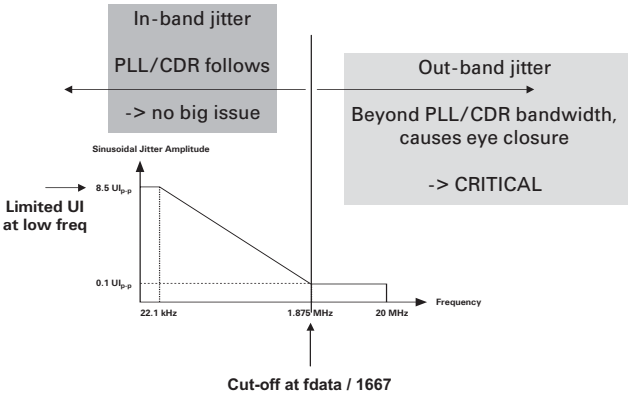
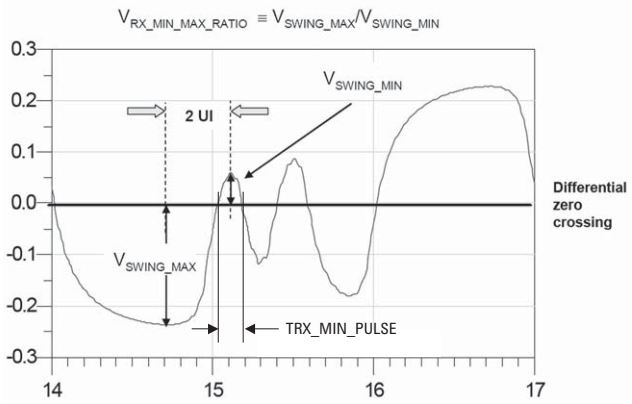


Figure 7: Jitter tolerance curve



Minimum Pulse Width
Minimum Pulse Amplitude
Amplitude Ratio

Figure 8: Dynamic voltage range

Dynamic voltage range

The dynamic voltage range specification in figure 8 is taken from Second Generation PCI Express® specification. The parameters minimum pulse width, and ratio of maximum to minimum swing describe the worst case loss in the channel the receiver has to tolerate. The 'lonely bit' is degraded in amplitude and pulse width by the loss of the channel. The specific jitter caused by the loss is called inter-symbol interference (ISI). A similar specification for the minimum pulse width at minimum amplitude is found in the FB-DIMM/AMB documents [3]. It is not used elsewhere, although it is an effective tool to describe the influence of a channel involving loss channel.

Comparing the requirements of the standard

Figure 10 summarizes the requirements of the various standards. This shows which standard uses which parameters. If no figures are given, this parameter is not used by the standard. The figures for compliance eye are the minimum eye-opening at which the receiver has to work. A figure for Min Pulse Width indicates the minimum pulse width of the lonely bit. A figure for tolerance curve shows how many UI of jitter is allowed at low frequency.

The next five columns (SJ/PJ, RJ, BUJ, ISI, Noise) quantify the amount of each individual jitter type required to build the compliance eye or specify the underlying jitter for the tolerance measurement. If there is only a tick, it means the standard recommends using this type of jitter, but does not give a figure for it.

The last column gives the modulating frequency and the deviation for spread spectrum clocking (SSC).

	Compliance Eye	Minimal Pulse Width	Tolerance Curve	SJ/PJ	RJ	BUJ	ISI	Noise (Stressed Eye)	SSC
PCIe 1.1 PCIe 2.0	.4 UI .4 UI	.6 UI		✓ ✓	✓ .16 UI		✓	✓	33kHz, 0/-.5%
10GbE XAUI	.7 UI .35 UI		5 UI @ 40kHz 8.5 UI @ 22kHz	.05 .. .15 UI .1 UI	.18 UI		< .25 UI .37 UI		
CEI 6/11G short	.4 UI .3 UI	.05 UI .. 5 UI	17 UI @ 2kHz	.05 UI	.15 UI .2 UI	.15 UI .25 UI	.3 UI .2 UI		
Fibre Channel 4.25 Gb/s	.38		1.5 UI @ 42.5 kHz	.33 UI	✓		✓	.1 UI	
FB-DIMM AMB 1.0/2.0	.4 UI	.55 UI	.5 UI @ 20kHz	.3 UI	.1 UI		.28 UI		33kHz, 0/-.5%
XFI/XFP	.35		15 UI @ 2 kHz	✓	✓		.2 UI	✓	
SATA II	.35 UI			.35 UI	.3 UI				33kHz, 0/-.5%

Figure 9: Jitter requirements by standard

Jitter Components

This section provides a short overview of the characteristics of the various jitter components

Sinusoidal (SJ) and periodic (PJ) jitter
Sinusoidal (SJ) and periodic jitter (PJ) are only different in how they are created. While SJ, which is in the lower frequency range (100 Hz .. 5 MHz), is created by clock modulation, PJ is created by delay modulation with help of a voltage controlled delay line. Both achieve multiple UI jitter at low jitter frequencies and a variable but time-limited amount of jitter at frequencies up to 1 GHz.

Random jitter (RJ): the Gaussian distribution
Random jitter (RJ) is caused by thermal and noise effects. These effects are statistical by nature, so the RJ is theoretically unbounded. It can be modeled by the Gaussian distribution, with the rms value equal to the $\hat{U}$ (sigma). There is a fixed relationship between sigma and the number of events. Typically the standards require a BER to be as low as 1e-12, which means 14.1 $\hat{U}$ for the total jitter budget. Practical noise sources deliver histograms up to 15 $\hat{U}$ a, which is specified as crest factor.

Bounded uncorrelated jitter (BUJ): the bounded distribution
BUJ, sometimes also called 'bounded RJ', can be created by filtering a PRBS data stream. The PRBS polynomial, filter frequency and the PRBS generation rate can be varied to create different jitter histograms (see also the section on calibration). Originally this is specified like random jitter without any tails; so it is specified by a peak-to-peak value. CE16 & CEI11 requires a bounded Gaussian distribution.

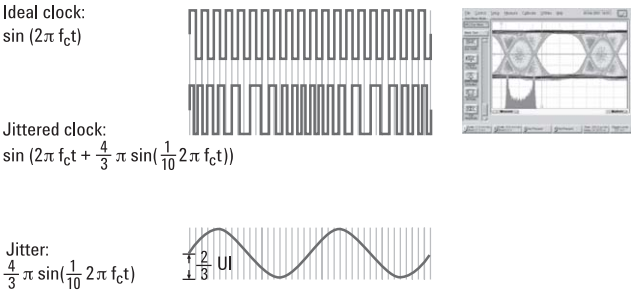


Figure 10: Sinusoidal and periodic jitter tolerance test setup

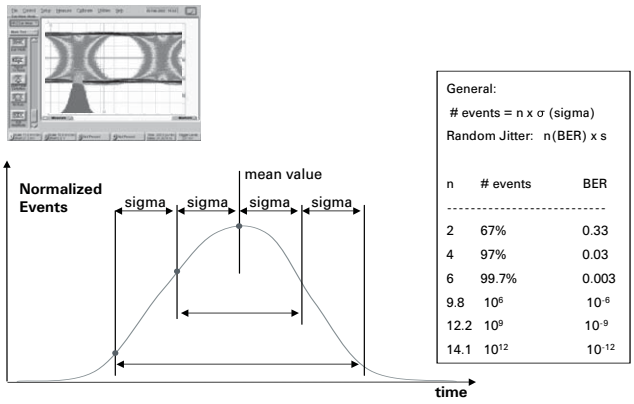


Figure 11: Random jitter: the Gaussian distribution

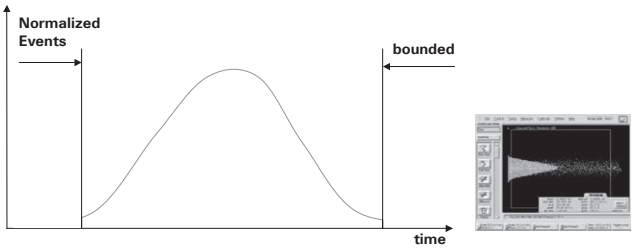


Figure 12: Bounded uncorrelated jitter: the bounded distribution

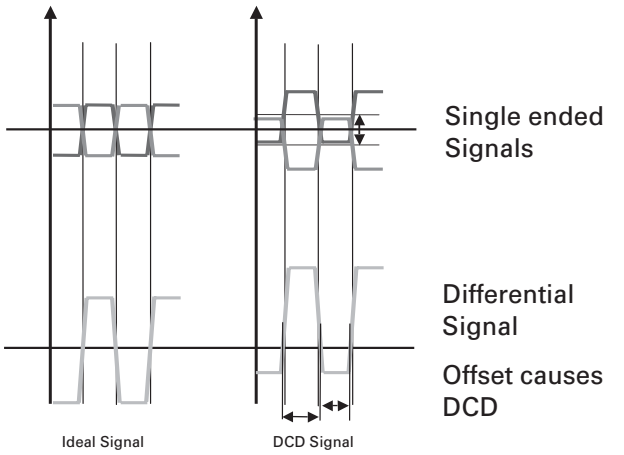


Figure 13: Duty cycle distortion

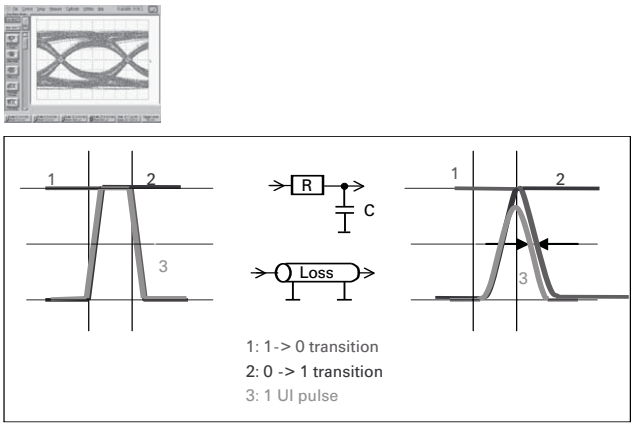


Figure 14: Inter-symbol interference

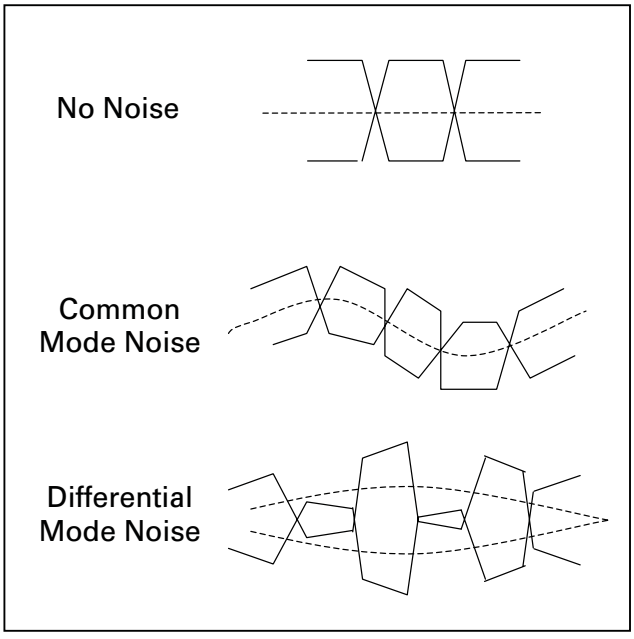


Figure 15: Common and differential mode noise

Duty cycle distortion (DCD)

Duty cycle distortion (DCD) can be achieved by offsetting the normal and complement signal. Without an offset, the bit width is the same for the logical '0' and '1'. A positive offset increases the bit width for a logical '1' and decreases the bit width of the logical '0' . A negative offset creates the opposite effect. The absolute amount of DCD depends on the transition time of the data signal. DCD can be created with help of differential noise (see below). Note that varying the cross point of the generator output does not create DCD.

Inter-symbol interference (ISI)

Inter-symbol interference (ISI) is jitter caused by bandwidth limitations and loss in the transmission media. This affects single bits with the opposite state to the surrounding bits. The trace (3) shows a '1' surrounded by '0's. ISI causes a shortening of this bit in time and amplitude, because there is not enough time for the signal to reach 100% before the next transition occurs. In the eye diagram the eye gets closed. ISI correlates with pattern and frequency. A given trace length provides different jitter depending on pattern and data rate.

Common and differential mode noise

Noise added to a single ended data signal creates first level modulation and thus edge modulation. On a differential signal, noise can be added as common mode noise (CM) or differential mode noise (DM). Common mode noise is the same on both signals. The differential signal is not affected. Differential mode noise modulates the amplitude of the differential signal and creates DCD.

Stressed eye

Stressed eye applies to optical signals. Electrically it can be described as a single ended signal that includes edge and level modulation. The edge modulation can combine several jitter components like ISI and RJ. A sinusoidal component is added as level modulation.

Jitter tolerance test setup according to standard

Some standards not only provide figures for individual jitter components, they also give details on how this should be setup, though without documenting equipment specific details. Figure 16 is taken from the Second Generation PCI Express® Standard [1]. The composition of the jitter is specified precisely.

The individual components are:
- Sinusoidal DJ up to 100 MHz
- Bandwidth limited random jitter
- Spread spectrum clocking
- High frequency phase modulation (sinusoidal jitter at f > 100 MHz)
- DM/CM crosstalk: this is common mode and differential mode noise
- Calibration channel: this is the ISI generation

This setup shall be calibrated into a 50 Ohms test load, which is the input impedance of an oscilloscope, for example.

A practical jitter tolerance test setup

One possibility to set up the various jitter components is to add various instruments as rack and stack. Figure 17 shows such a setup.

The instruments needed are:
- Signal generator to provide a modulated clock
- PC board with traces of various length for ISI
- Random noise source
- Pattern generator with PRBS pattern for BUJ
- Arbitrary waveform generator for PJ

All this functionality is now integrated into an innovative new instrument that can create all the necessary jitter components off-the-shelf. The complementary tool in both cases is always the DCA-J sampling oscilloscope for waveform and jitter analysis.

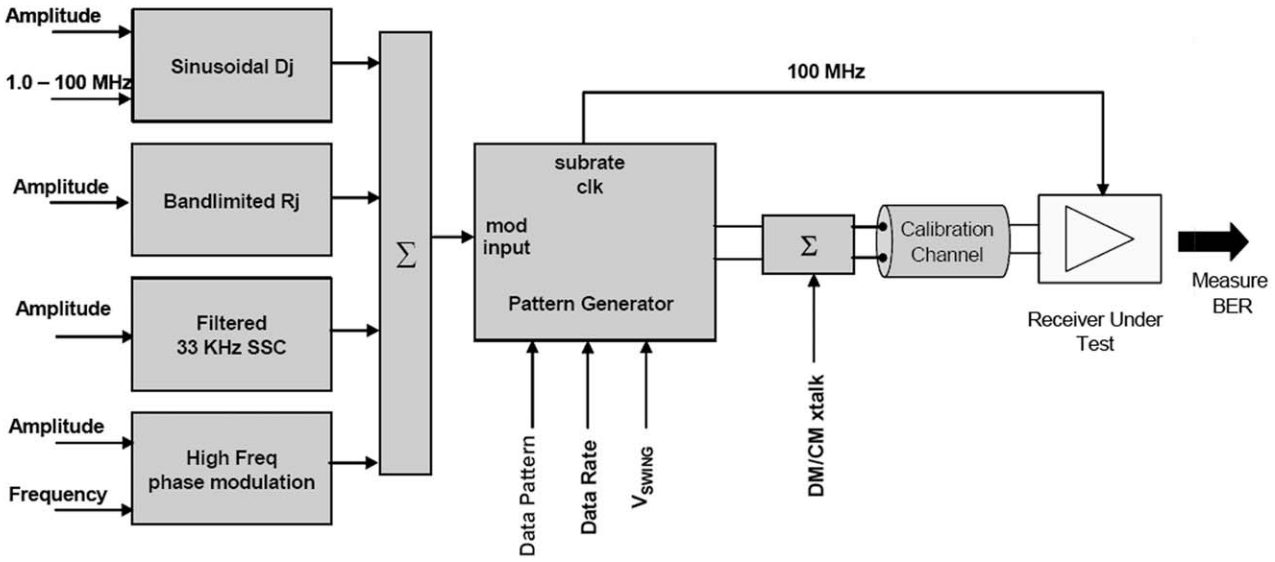


Figure 16: Second Generation PCI Express®-jitter modulation details

Jitter tolerance test setup integration

Figure 18 shows how the hardware in the Agilent N4903A J-BERT ensures full jitter composition capabilities.

The following terminology is used:

- SJ Sinusoidal (DJ) jitter is created by clock modulation.
- PJ High frequency phase modulation is created by edge modulation with help of the delay line. PJ is available with a sine, square or triangle wave form.
- BUJ Band limited RJ is created with help of the delay line.
- SSC SSC is created by clock modulation with help of a triangular modulation signal.
- ISI The calibration channel is implemented by the interference module providing filter switching for ISI generation.
- Common/Differential Mode Noise
  DM/CM crosstalk is created by the interfer ence module with help of the sinusoidal interference (level modulation).
- RJ Random noise is created with help of the delay line driven by a noise source.

There is also the possibility to feed any external Signal into the delay line for jitter modulation. This path of external input can be used to calibrate some of the jitter components (see the section on calibration).

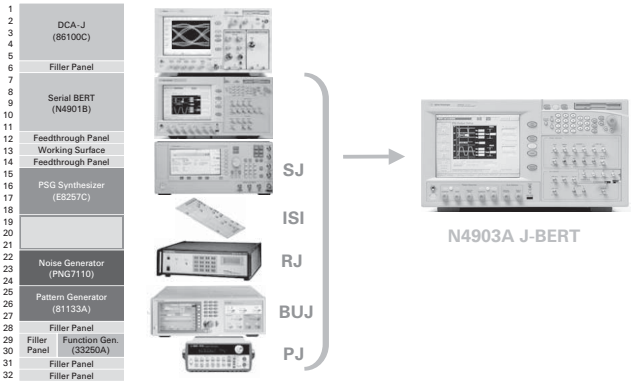


Figure 17: Jitter tolerance test setup

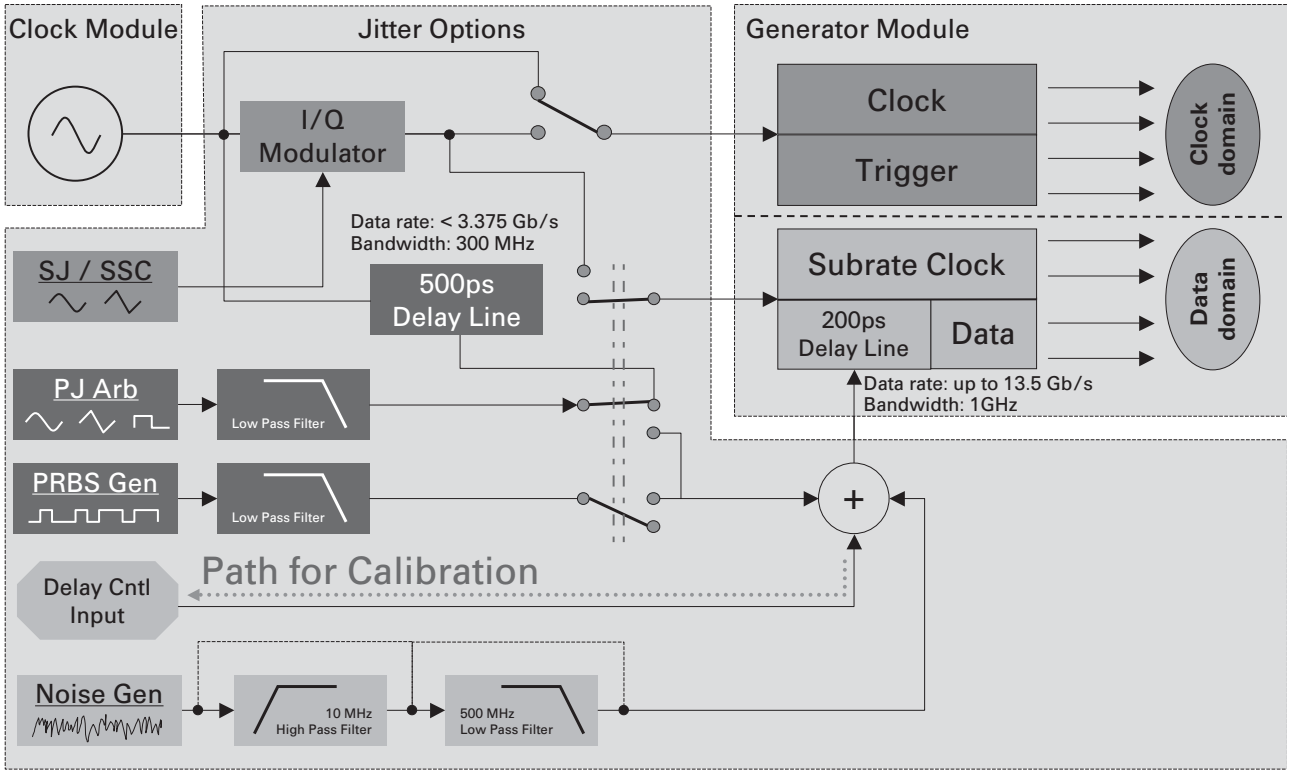


Figure 18: J-hardware overview

Agilent N4903A J-BERT High-Performance Serial BERT Jitter Generation

The jitter generation capabilities are carried out by two units. The first is embedded in the generator. This can create clock modulation (SJ), periodic jitter (PJ), random jitter (RJ), bounded uncorrelated jitter (BUJ) and spread spectrum clocking (SSC). This is option J10. The second unit is the interference module, which is highlighted in figure 19. This provides inter-symbol interference (ISI) and sinusoidal interference (common/ differential noise). This is option J20.

Figure 20 shows the jitter setup for option J10. The individual jitter components can be enabled and each jitter component has a submenu to control its individual parameters. The overview also shows the selection of the delay line. There is a 500 ps and a 200 ps delay line. The 500 ps delay line can be used for data rates up to 3.375 Gb/s; the 200 ps delay line can be used at any data rate. Periodic jitter (PJ) can be created using either delay line. Random jitter (RJ), bounded uncorrelated jitter (BUJ) and external signals are routed to the 200 ps delay line. inusoidal jitter is created by clock modulation, without using either delay line. Each jitter is specified as amplitude in milliUI (mUI). Calibrated jitter means a user specifies jitter in time or UI. In this case, there is no need for indirect values like modulation voltages.

Figure 21 shows the interference channel setup. This lets you specify a specific trace for ISI generation and the parameters for sinusoidal interference. The sinusoidal interference needs the minimum trace length in the ISI filter. Externally there are two ports: P1 and P2. The generator output needs to be connected to P1. This ensures the sinusoidal interference is inserted at the far end as required by the standards.

In summary the new N4903A is a smart characterization choice for testing emerging serial gigabit devices. It helps engineers make quick and accurate jitter tolerance tests, which have been complicated and hard to implement in the past. The jitter sources cover the needs for compliance testing to the most popular standards.

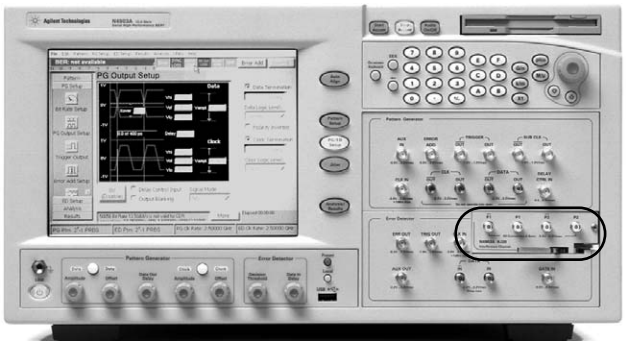


Figure 19: J-BERT jitter sources built into the generator and the interference channel (highlighted)

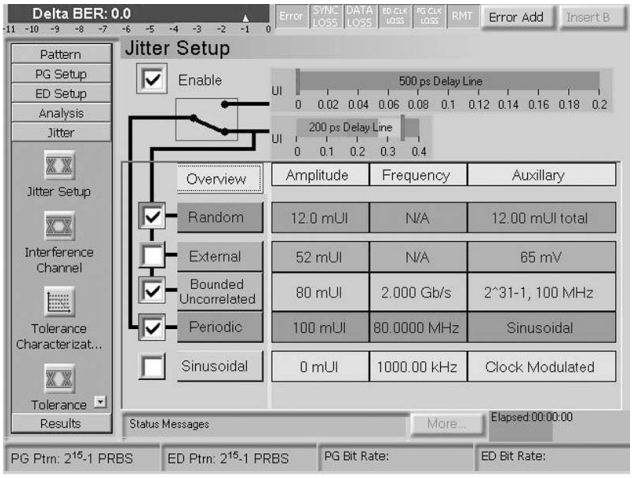


Figure 20: Manual jitter composition setup

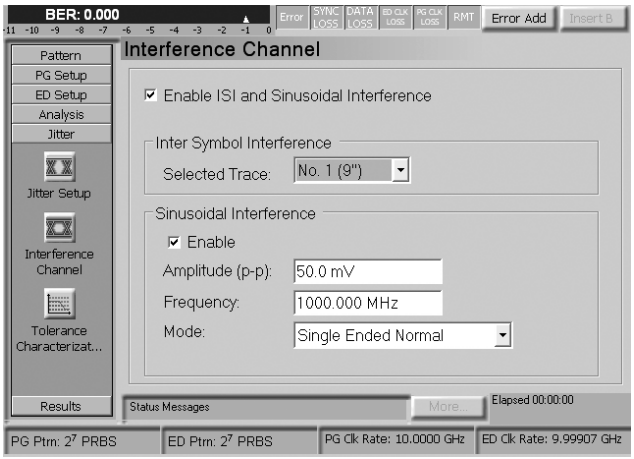


Figure 21: SI and ISI setup

J-BERT N4903A automated jitter tolerance test for receivers

The key measurements are:

- Tolerance characterization (option J10)
- Tolerance compliance (option J12)

Characterizing receiver tolerance (see figure 22), automatically searches for the maximum jitter value the receiver tolerates by sweeping SJ and PJ in frequency and amplitude. You can set various search parameters (linear, logarithmic, binary – upwards, downwards – step sizes.....)

The automated jitter tolerance compliance test checks whether the receiver meets the standards, and determines non-compliant points. The result is a diagram with pass/fail indication for the tested points (see figure 23). Compliance curves are available for SATA, XAUI, 10 GbE, and CEI.

See the next page for an example of jitter tolerance compliance testing for CEI.

J-BERT N4903A total jitter measurements for transmitters

Apart from receiver testing tools, the J-BERT provides measurements routines for transmitter test too:

- BERT scan measurement
- Fast total jitter measurement

The output timing measurement in figure 24 is a one-dimensional BERT scan showing the BER over time. The fast total jitter measurement in figure 25 measures the total jitter (TJ) in the fastest possible way. It is typically 40 times faster than the traditional BERT scan. It compares bits until it can decide with a 95% confidence whether the BER is above or below the desired level.

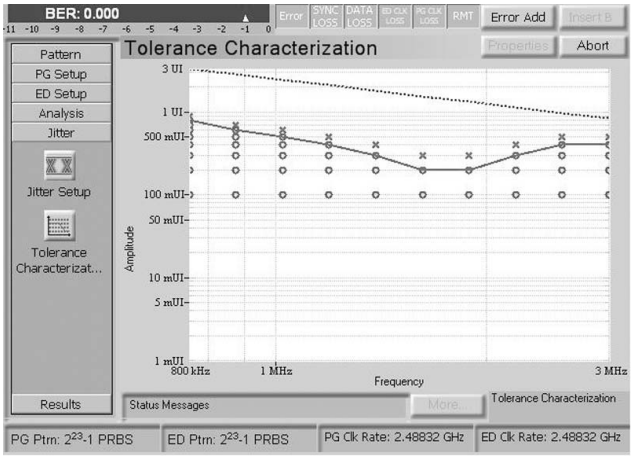


Figure 22: Jitter tolerance characterization

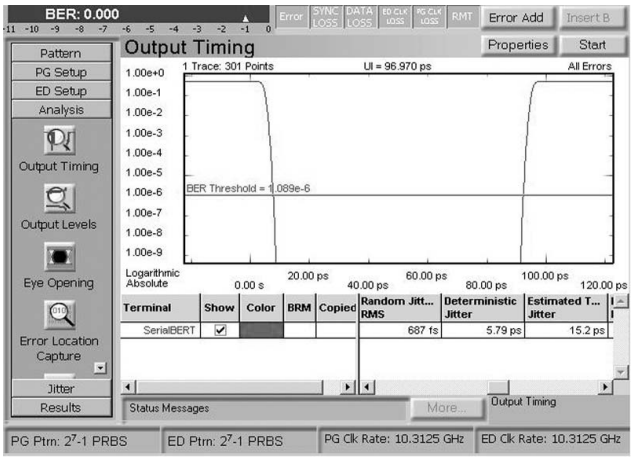


Figure 24: Total jitter measurement, BERT scan

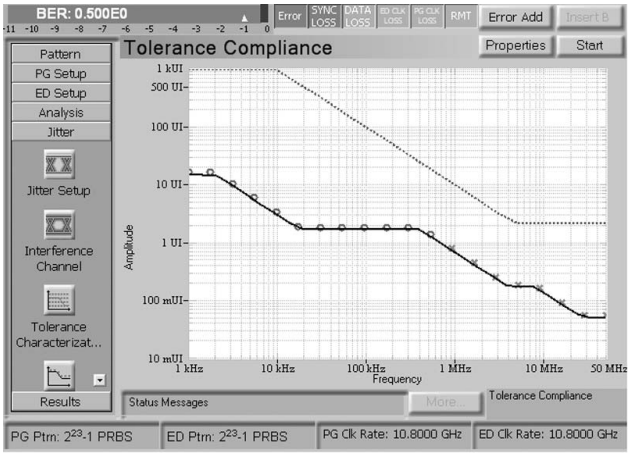


Figure 23: Jitter tolerance compliance

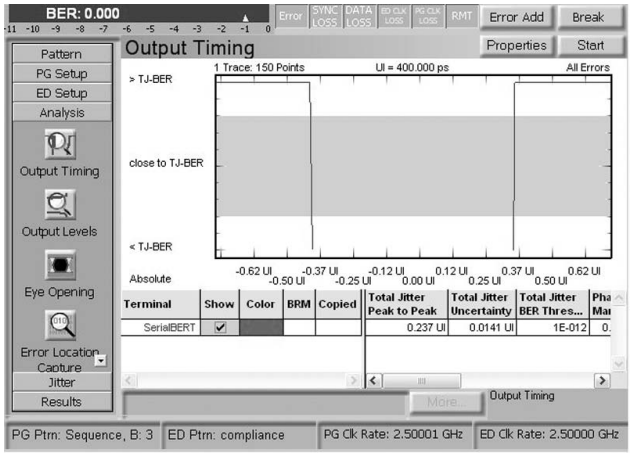


Figure 25: Total jitter measurement, fast total jitter

Receiver compliance test for CEI

Compliance testing ensures that a design meets the criteria defined by the reference values provided by the standard. Here is an example taken from CEI 6G SR [4]. The standard defines the tolerance curve (in this standard it is called the relative wander mask) and the total jitter budget. Both of these are shown in figure 26a. The tolerance curve defines a frequency and magnitude sweep of sinusoidal jitter. The magnitude of the sinusoidal jitter is defined as 5 UI for the 'Relative Wander Amplitude' and .05 UI for the 'High Frequency Amplitude'.

The total jitter budget defines the jitter components on top of the sinusoidal jitter. The terminology used by the standard translates to the jitter naming used in this document as:

UUGJ -> RJ = .15 UIpp = .15/14 UIrms
UHPJ = .15 UI -> BUJ = .15 UI
CBHPJ = .2 UI -> ISI = .3 UI

The given TJ does not include the sinusoidal component defined by the relative wander mask. ISI is pattern dependent. This standard requires as jitter tolerance and general test patterns a free running PRBS31 polynomial. Best fit for the ISI requirement is trace 2. RJ and BUJ can be set as required. The receiver input specifies the minimum differential input voltage to be 125 mV or 62.5 mV single ended. As ISI modulates the signal amplitude, the minimum amplitude is achieved when the levels at the generator are set to 250 mV. Figure 26 shows the single ended generator signal with RJ, BUJ and ISI enabled.

Figure 23 shows the compliance curve measurement. After selecting the proper curve, the measurement begins by pushing the START button.

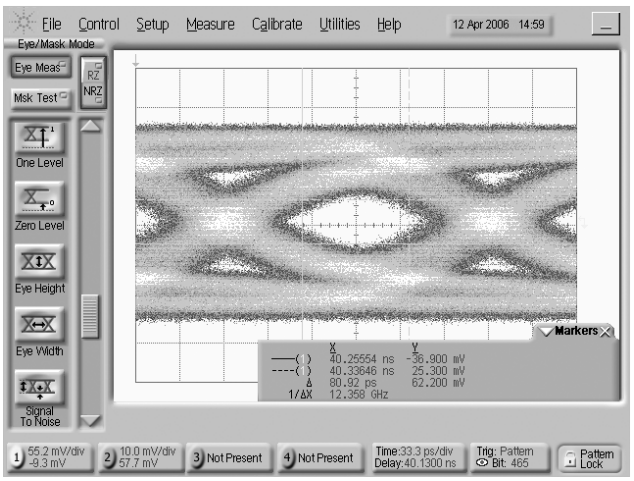


Figure 26: Composite signal for CEI-6G-SR

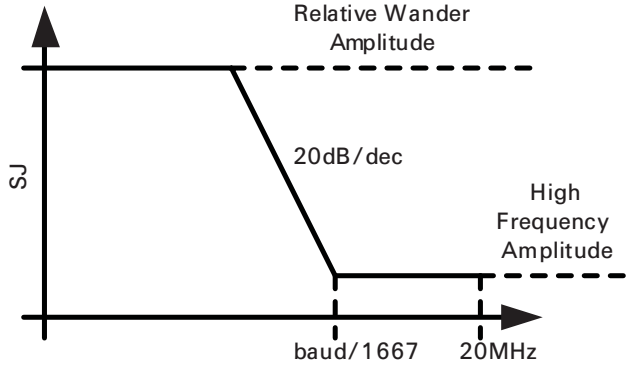


Figure 26a: CEI-6G-SR relative wander mask

CEI-6G-SR	Uncorrelated Jitter		Correlated Jitter		Total Jitter				Amplitude	
	Unbounded Gaussian	High Probability	Bounded Gaussian	Bounded High Probability	Gaussian	Sinusoidal	Bounded High Probability	Total		
Abbreviation	UUGJ	UHPJ	CBGJ	CBHPJ	GJ	SJ	HPJ	TJ	k	
Unit	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp	UIpp		mVppd
Transmitter	0.150	0.150		-0.200 See 1	0.150		-0.050	0.100		400.0
Channel				0.500						
Receiver Input	0.150	0.150	0.000	0.300	0.150		0.450	0.600	0.25	125
Clock + Sampler	0.150	0.100		0.100						-50.0
Budget	0.212	0.250	0.000	0.400	0.212	0.050	0.650	0.912	0.13	75.0

Figure 26b: CEI-6G-SR high frequency jitter budget

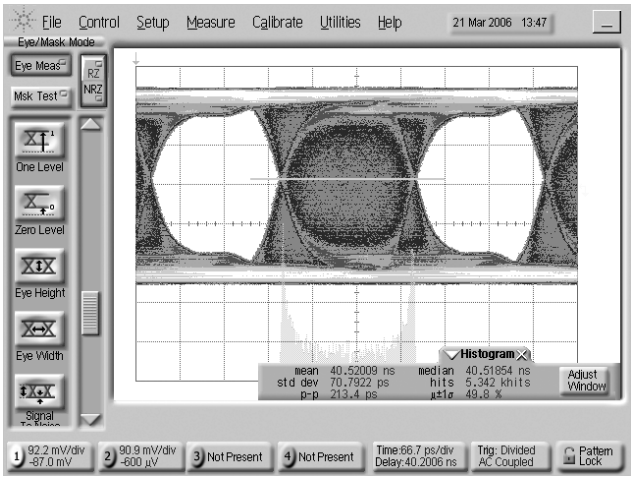


Figure 27: Histogram measurement on DCA-J

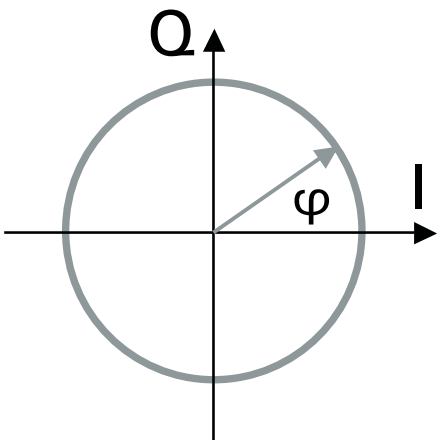


Figure 28: IQ modulation

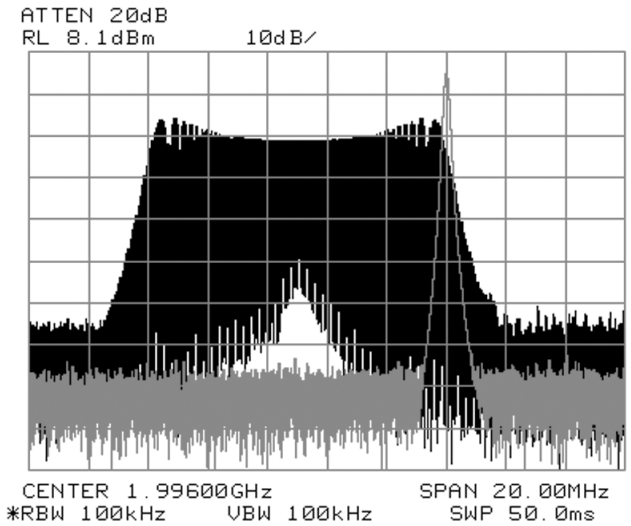


Figure 29: SSC modulation

Calibrating the jitter sources of the Agilent N4903A J-BERT

There are three ways to measure and calibrate jitter:

- The histogram
- The spectral analysis
- The BERT scan (bathtub)

The histogram samples events over time and presents them as a distribution, which can be evaluated for deterministic and statistical content. A histogram can be measured on any signal, so it can be done on the data signal directly. A histogram measurement is performed with help of a scope, such as a DCA-J.

The spectral analysis measures in the frequency domain using a spectrum analyzer. This analysis is best performed on a clock signal, as data adds further spectral content, which may make the analysis more difficult.

The clock modulator and the delay lines need on the J-BERT to be calibrated. The other jitter sources do not need calibration: ISI is implemented by fixed discrete traces, which do not need any calibration, and sinusoidal interference is specified as amplitude, so specific calibration is not necessary for jitter purposes.

Sinusoidal jitter (SJ) calibration

SJ is created by an IQ modulator. The I and Q signals are created from memory by digital-to-analog converters (DAC). SJ is accurate as long as the I and Q signals have the same amplitude (as shown in figure 28), otherwise the circle will be distorted, resulting in a phase error. From trigonometry, we can calculate that a phase error of less than .01 UI requires amplitude matching of 5%. The levels of the I and Q signals are calibrated to less than 3% by the calibration path (figure 18) with the help of an oscilloscope. The absolute amplitude is not of concern, as the modulated signal is fed to limiting amplifiers. Apart from calibrating the level, the modulator output is checked for the symmetry of I and Q: there must be a 90° shift (equivalent to a 1/4 period delay) between them. Typically, the total accuracy of sinusoidal jitter is below.

SSC

SSC modulation also makes use of the clock modulator, but now the modulation is triangular. The I and Q signal are more complex, but again the amplitude defines the deviation. In this case, as shown in figure 29, the amplitude is calibrated with help of spectrum analysis. In this picture one can see a deviation of –0.5% (10 MHz) at the 2 GHz clock rate. The figure shows both the unmodulated and the modulated clock. The gain of the deviation is calibrated by measuring the span. The symmetry of the I and Q signals affect the harmonics outside the modulation band. This is adjusted to be at least 40 dB below the modulation plateau.

Delay line

Figure 30 shows the typical linearity of the 200 ps delay line. The delay line needs is linear by design as any non-linearity cannot be calibrated. Delay linearity is expressed as ps/mV. The measurements show that accuracy is better than 10% over the full environmental conditions.

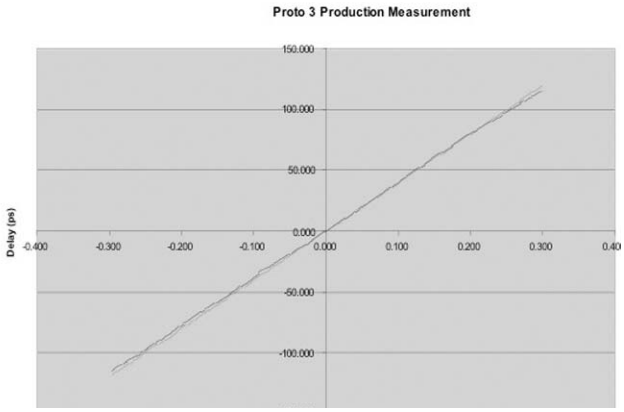


Figure 30: Delay line linearity

Periodic jitter (PJ)

For periodic jitter the delay line is modulated with a sinusoidal, triangular or square signal, as shown in figure 31. The sinusoidal signal is created by an arbitrary waveform generator. The levels from the arbitrary waveform generators are calibrated to 1% accuracy. Also, the modulated data signal is measured with the oscilloscope and the histogram measurement. The histogram measurement for sinusoidal jitter shows a distribution with two peaks, and a local minimum between them. The distance between the two peaks is the DJ (d-d) value. In cases where the RJ is negligible, this is close to the PJ.

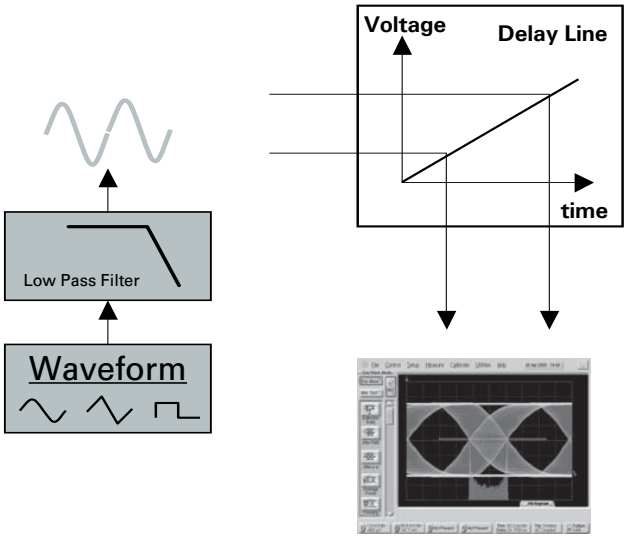


Figure 31: PJ calibration

Random Jitter (RJ)

Random noise (RJ) is created with help of the delay line, as shown in figure 32, using a random noise source. The noise source provides a crest factor of 14, which means the peak-to-peak noise is limited at 14 times the rms value. The amplitude of the noise source can be calibrated to ensure (14 x rms) creates 200 ps jitter, which is the maximum the delay line can handle. The oscilloscope is used to calibrate voltage and timing of the noise sources. This makes the jitter measurement independent of golden jitter references models. Random noise can be low-pass or high-pass filtered.

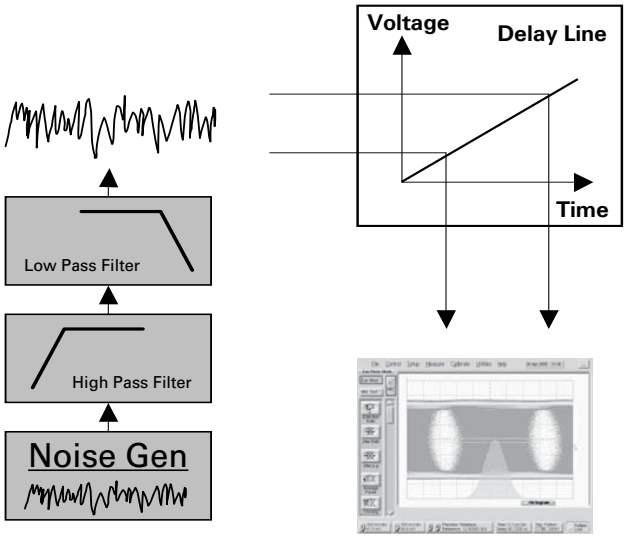


Figure 32: RJ calibration

Bounded Uncorrelated Jitter (BUJ)

This type of jitter is created by applying a filtered PRBS to the delay line, as shown in figure 33. Using a PRBS guarantees that it is bounded. Essential is the filtering, only a carefully chosen combination of PRBS polynomial, frequency and selected filter gives calibrated results. The CEI standard invented this type of jitter. Here the combination of polynomial, frequency and filtering is fixed.

According to the CEI-02.0 standard:

"The jitter control signal for generating High Probability Jitter should be filtered using at least a first order low pass filter with a corner frequency between 1/20 - 1/10 of the baud rate of the PRBS generator to ensure that high frequency components are removed. The distribution of the jitter after the filter must be reasonably even, symmetrical, and large spikes should be avoided. The order of the PRBS polynomial may be between 7 and 11, inclusive, to allow flexibility in meeting this objective. The rate of the PRBS generator should be between 1/10 - 1/3 of the data rate of the DUT being tested, and their rates must be not harmonically related. The upper -3 dB frequency of the filtered HPJ should be at least 1/100 of the data rate of the DUT being tested to represent transmitter jitter that is above the tracking frequencies of the DUT's CDR. Calibration of HPJ must be done with a golden PLL in place. Once these objectives are achieved, there is no need to vary these settings; any combination of settings that meets all the objectives is satisfactory."

The N4903A provides CEI compliant calibrated presets.

Apart from these presets the N4903A provides a Gaussian setting based on a PRBS 2^{31}-1 generated at 2 GHz and filtered with 100 MHz. This combination gives a smooth spectral distribution, similar that shown in figure 35. Such a spectrum creates a jitter distribution close to Gaussian, as shown in figure 34. Such a distribution can be calibrated by measuring the peak to peak level of the signal that drives the delay line. Custom settings of polynomial, frequency and filtering are possible but do not result in calibrated jitter. The histograms are not Gaussian, so it is recommended to double check the results if you alter these parameters extensively.

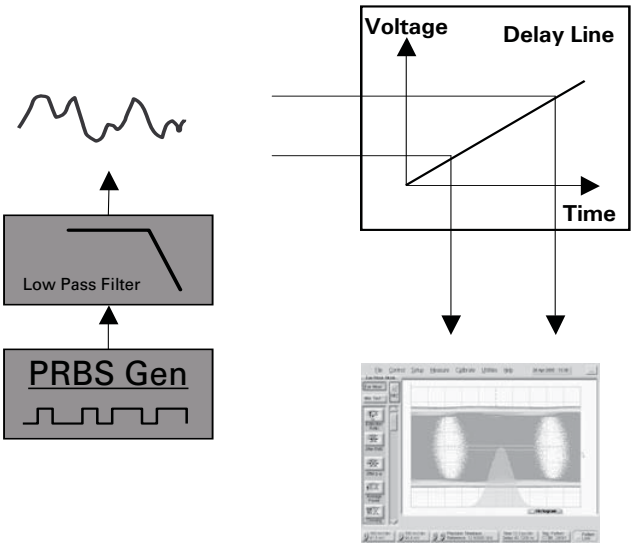


Figure 33: BUJ calibration

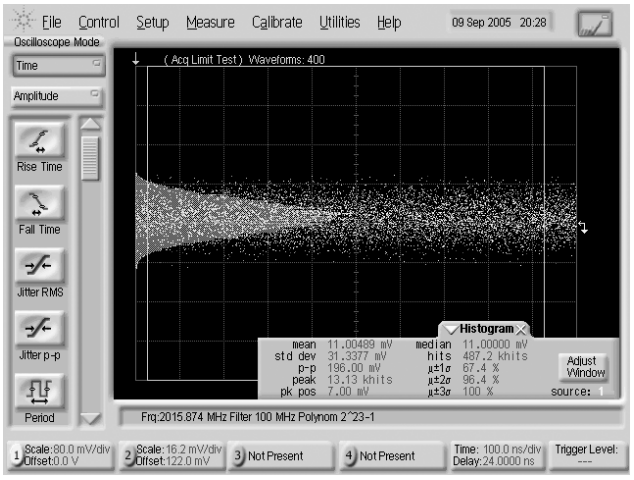


Figure 34: BUJ histogram for frequency 2015.874 MHz, PRBS 2^{23}-1, filter 100 MHz

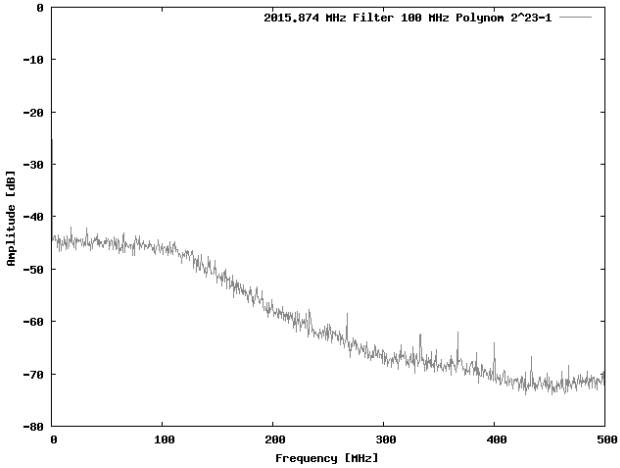


Figure 35: Spectrum of the input voltage at frequency 2015.874 MHz, PRBS 2^{23} -1, filter 100 MHz

Jitter laboratory setup

This laboratory compares the jitter measurement results against the various jitter components created.

For this the following readings are compared against the expected jitter setup:

- The reading of the horizontal eye-opening provided by the Auto Alignment
- The eye width reading from the eye diagram measurement
- The RJ, DJ and TJ reading from the output timing measurement

The equipment for this jitter laboratory is set up as follows:

The output from the Agilent N4903A data generator is connected differentially to the interference module port P1. The complement output of the module port P2 is terminated with 50 Ohms, the normal output connects via a 3 dB attenuator to a power divider (11636B). One side of the power divider is connected to the N4903A analyzer normal data input; the complement input is terminated with 50 Ohms. The other side of the power divider can connect to any other equipment for comparing the results, such as the DCA-J. The N4903A clock outputs are fed to the clock input of the N4903A analyzer and to the clock or trigger input of a comparing device.

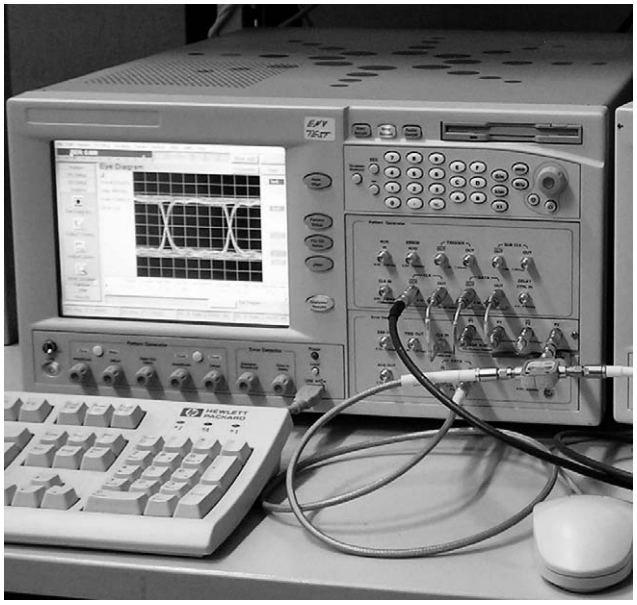


Figure 36: Jitter laboratory equipment setup

Good practice hints:

- Use the same output by power splitting, do not use out and complement out
- Use cables of same type and length to connect the power divider to the J-BERT analyzer input and the input of the comparing device. The 3dB attenu ator improves the back-termination

In the examples shown here, the BERT data generation is at the data rate of 2.5 Gb/s and 10 Gb/s. The pattern used is the PRBS polynomial 2^7-1. The levels of the generator are set to +/- 600 mV. The J-BERT analyzer is used in external clock mode. The following parameters settings are changed from the defaults: The BER Threshold in Auto Alignment is set for 1e-3. The transition time measurements in the eye diagram routine is set for 20/80%. The number of bits in the output timing is set for 1e8 bits and the resolution is set to 1 ps (at 2.5 Gb/s) and .5 ps (at 10 Gb/s). The BER Threshold is set for 1e-4 and the minimum BER for RJ/DJ Separation is set for 1e-8. This ensures enough measurement points for the RJ/DJ separation, while excluding the DJ from the RJ extrapolation.

The pictures opposite show the initial measurements without any jitter added. To compare the readings of Auto Align, eye diagram and TJ, consider the BER threshold parameter. For the Auto Align this is BER = 1e-3, so Auto Align sees 6x the rms value of any random jitter. The eye diagram uses BER = 1e-6, so it sees 10x the rms value. The TJ of the output timing measurement uses BER = 1e-12 or 14x the rms value is included in the reading.

Findings

Though there is no jitter added, there is a slight amount of intrinsic ISI introduced by the interference channel (6 ps at 2.5 Gb/s, 10 ps at 10 Gb/s). The reported readings match well with the expectations, except for the DJ figures from the output timing measurement. These readings are just half of the ISI.

No jitter at Data Rate: 2.5 Gb/s

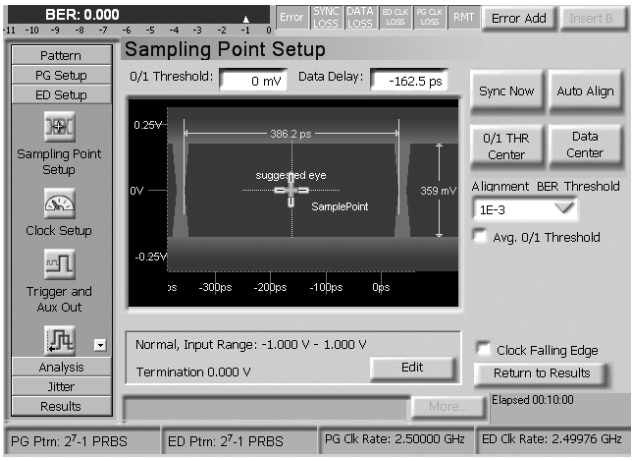


Figure 37: Agilent N4903A auto alignment

No jitter at Data Rate: 10 Gb/s

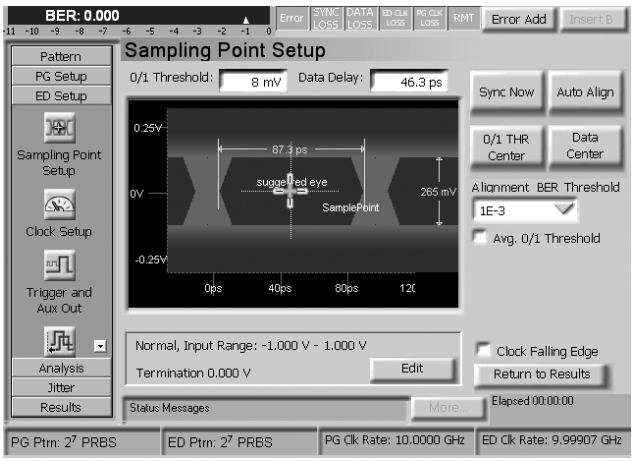


Figure 37b: Agilent N4903A auto alignment

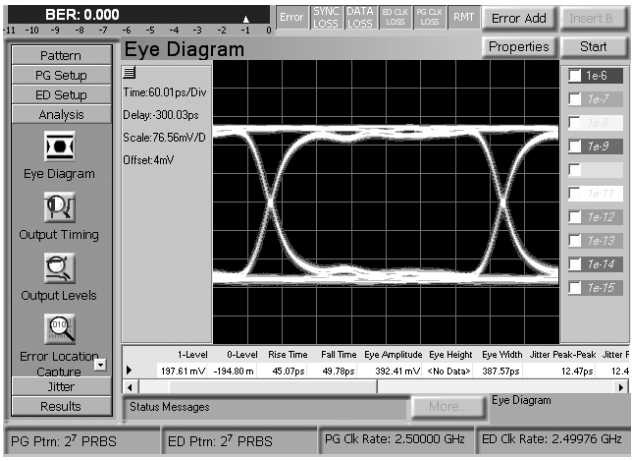


Figure 38: Agilent N4903A eye diagram

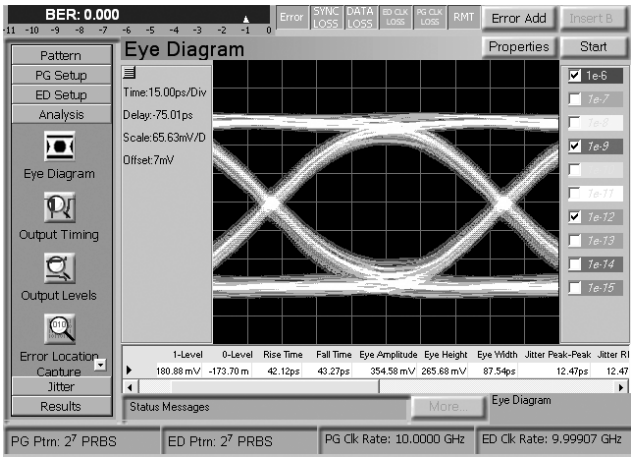


Figure 38b: Agilent N4903A eye diagram

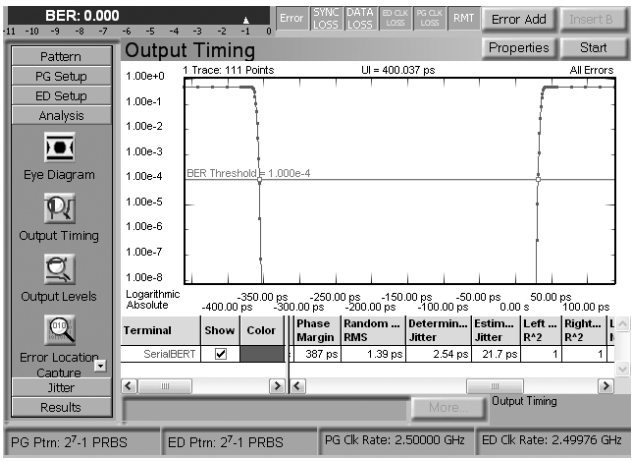


Figure 39: Agilent N4903A BERT scan measurement

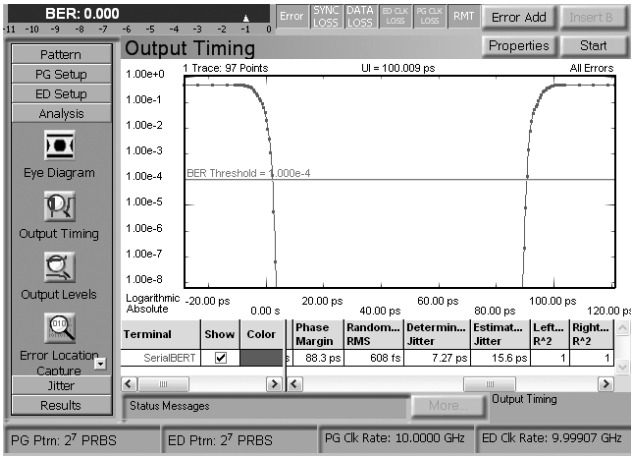


Figure 39b: Agilent N4903A BERT scan measurement

Data Rate: 2.5 Gb/s

ISI (inter-symbol interference), 2.5 Gb/s

The ISI jitter setup on N4903A is done by selecting a trace of specified length. For this example we chose trace #5 with 28“ (see figure 43). Figure 22 of N4903A data sheet (5989-2899EN) [5] specifies typical ISI for various data rates and patterns. This provides the reference for expectations, see the table below. So the reference is an ISI of .24 UI or 96 ps.

Findings

The results agree with the expectations for the Auto Align and the eye width reading in the eye diagram. The output timing measurement shows parts of the ISI reflected in the RJ value. The total jitter is reported accurately.

Datarate	1.25 Gb/s			2.5 Gb/s		
ISI trace length [inch]	PRBS 2^7-1	PRBS 2^{15} - 1	CJPAT	PRBS 2^7-1	PRBS 2^{15} - 1	CJPAT
3.5"	0.007	0.017	0.016	0.016	0.022	0.014
9"	0.026	0.034	0.037	0.039	0.066	0.039
16"	0.045	0.068	0.051	~~0.103~~	0.138	0.106
20"	0.058	0.088	0.062	0.152	0.184	0.123
24"	0.081	0.109	0.103	0.182	0.260	0.171
28"	0.098	0.141	0.147	0.241	0.334	0.238
32"	0.128	0.153	0.120	0.289	0.395	0.295
36"	0.156	0.188	0.168	0.375	0.493	0.390
40"	0.172	0.228	0.199	0.458	0.626	0.423
44"	0.199	0.262	0.247	0.571		

Table 1

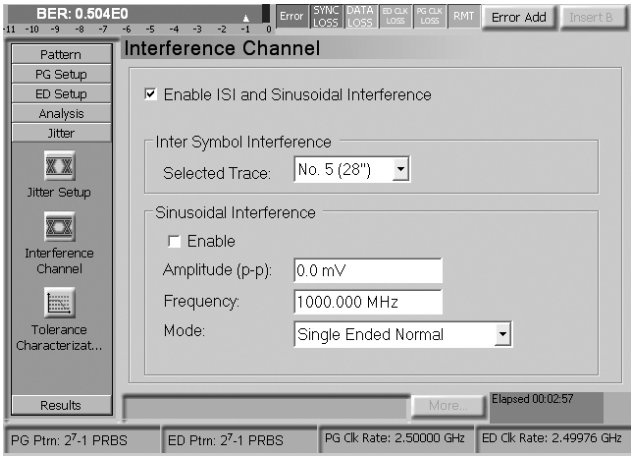


Figure 43: ISI jitter setup on the Agilent N4903A

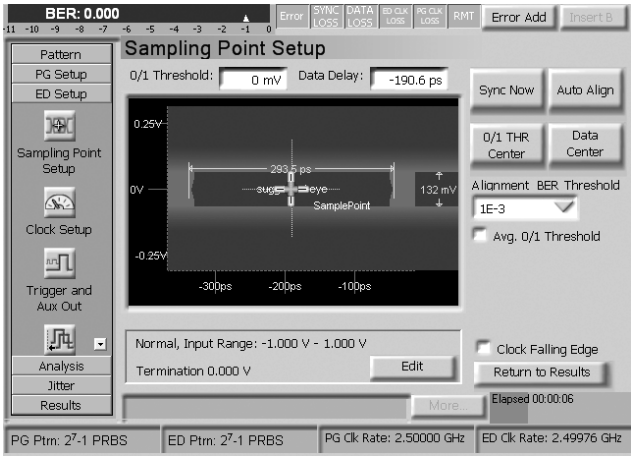


Figure 44: Agilent N4903A auto alignment

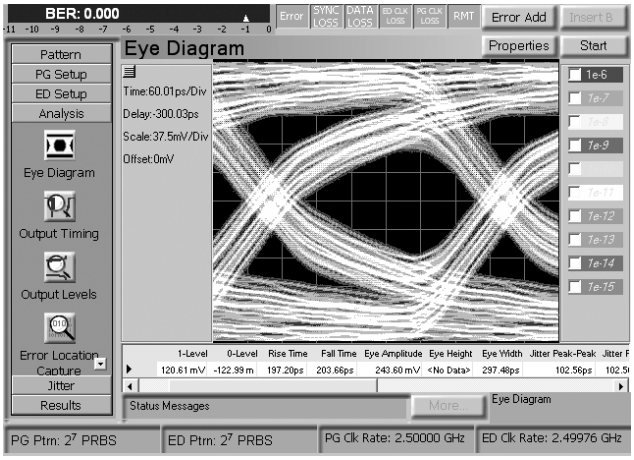


Figure 45: Agilent N4903A eye diagram

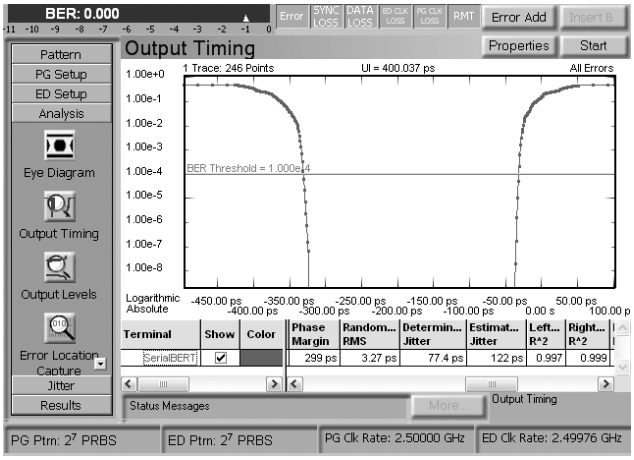


Figure 46: Agilent N4903A BERT scan measurement

Data Rate: 10 Gb/s

ISI (inter-symbol interference), 10 Gb/s

For this ISI jitter we chose trace #1 with 9“. This corresponds to .33 UI or 33 ps jitter according the table in the data sheet.

Findings

The results agree with the expectations for the Auto Align and the eye width reading in the eye diagram. The RJ/DJ separation shows the DJ too small, while the total jitter is reported accurately again.

Datarate	11 Gb/s		
ISI trace length [inch]	PRBS 2^7-1	PRBS $2^{15}-1$	CJPAT
3.5"	0.099	0.146	0.131
9"	0.329	0.504	0.405
16"			
20"			
24"			
28"			
32"			
36"			
40"			
44"			

Table 2

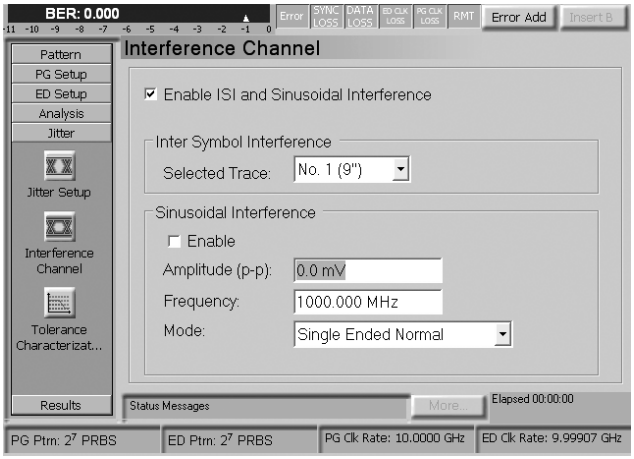


Figure 43b: ISI jitter setup on the Agilent N4903A

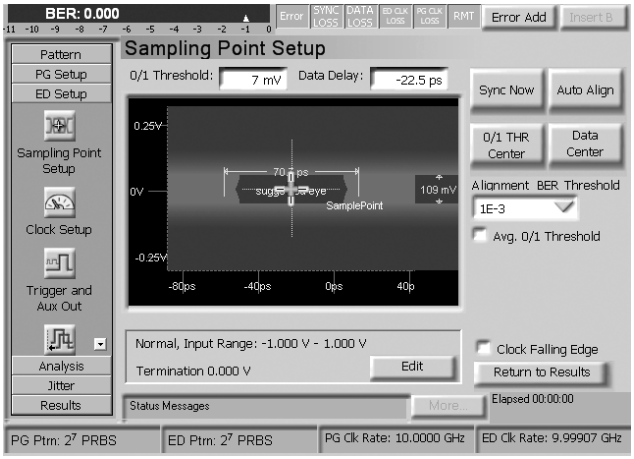


Figure 44b: Agilent N4903A auto alignment

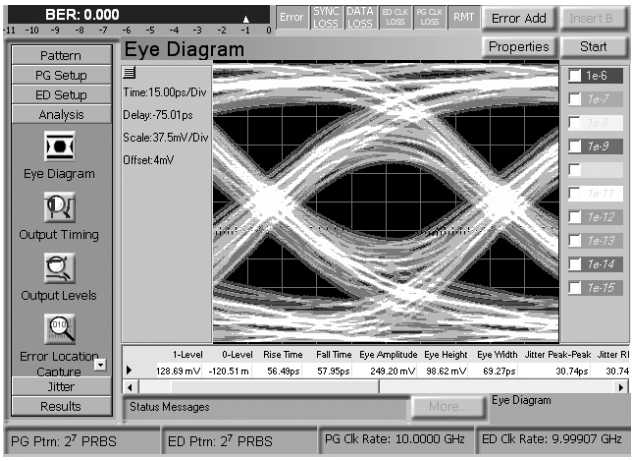


Figure 45b: Agilent N4903A eye diagram

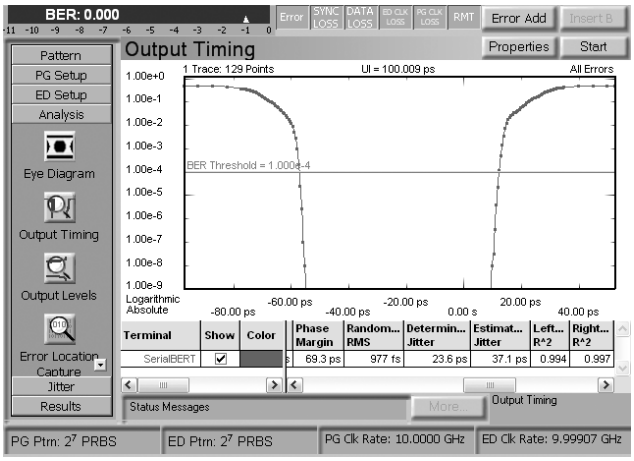


Figure 46b: Agilent N4903A BERT scan measurement

Data Rate: 2.5 Gb/s

SJ (sinusoidal jitter), 2.5 Gb/s

Sinusoidal jitter is created by modulating the clock source of the N4903A generator. In this setup, we set the sinusoidal jitter for .5 UI or 200 ps at a jitter frequency of 5 MHz, as shown in figure 50.

Findings

The results agree with the expectations for the Auto Align, the eye width reading in the eye diagram and the RJ, DJ and TJ readings of the output timing measurement.

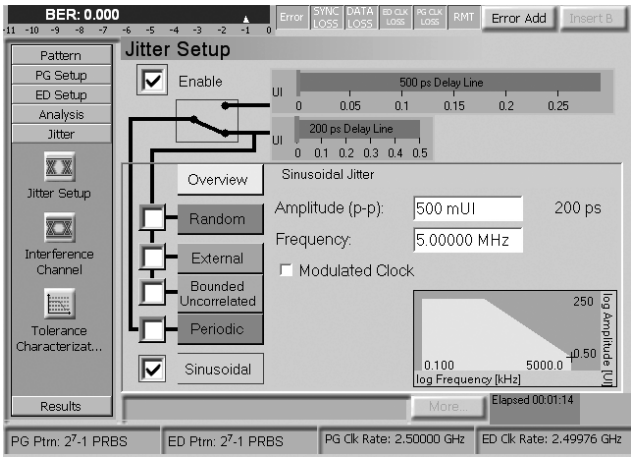


Figure 50: Sinusoidal jitter setup on the Agilent N4903A

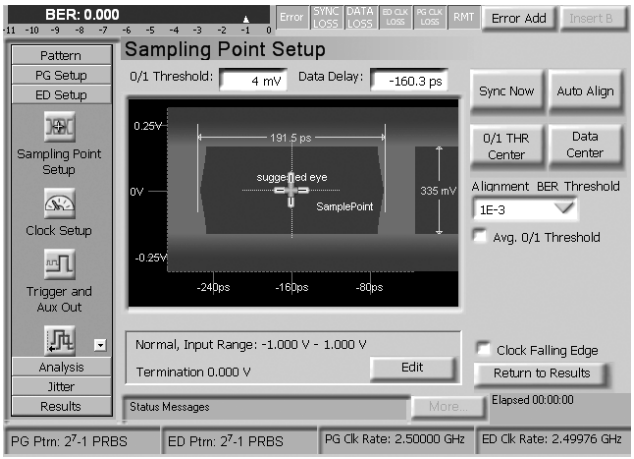


Figure 51: Agilent N4903A auto alignment

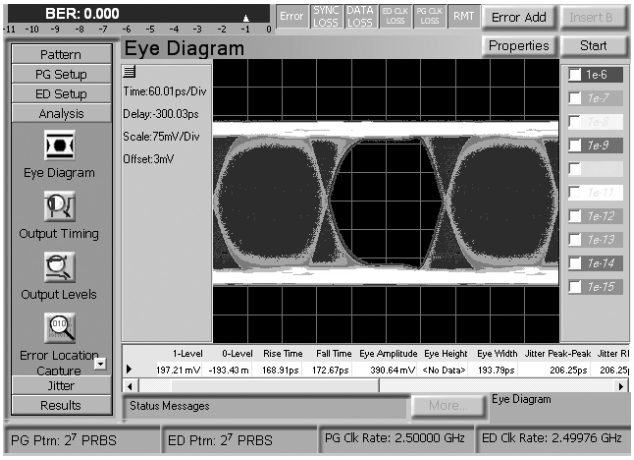


Figure 52: Agilent N4903A eye diagram

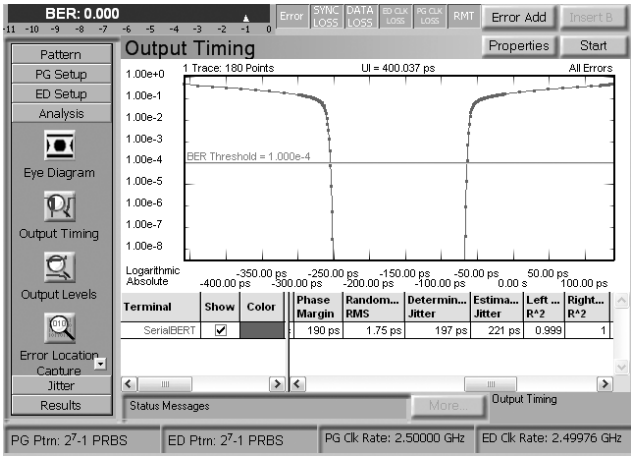


Figure 53: Agilent N4903A BERT scan measurement

Data Rate: 10 Gb/s

SJ (sinusoidal jitter), 10 Gb/s

In this setup, we set the sinusoidal jitter for .5 UI or 50 ps at a jitter frequency of 5 MHz, as shown in figure 50b.

Findings

The results agree with the expectations for the Auto Align, the eye width reading in the eye diagram and the RJ, DJ and TJ readings of the output timing measurement.

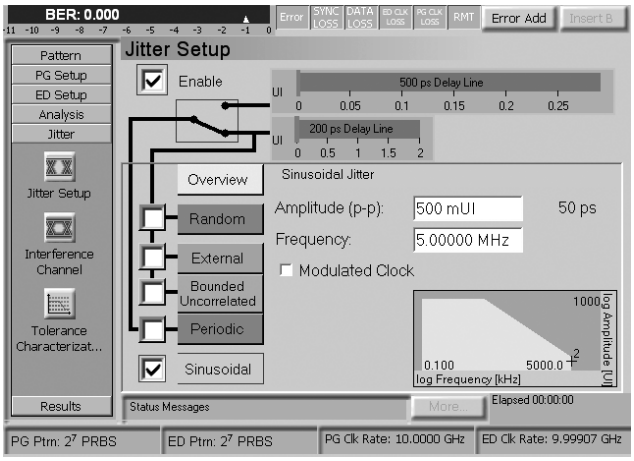


Figure 50b: Sinusoidal jitter setup on the Agilent N4903A

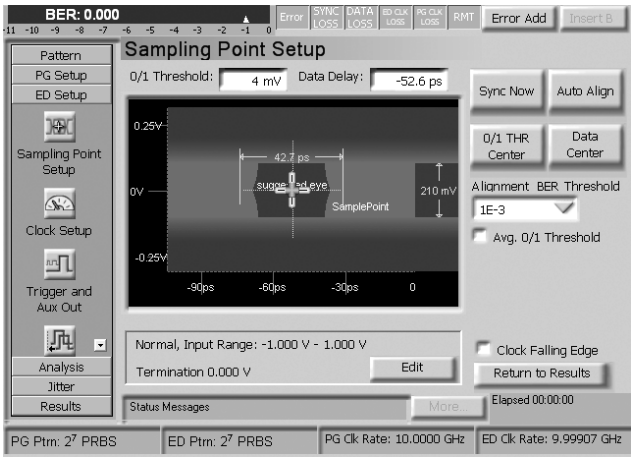


Figure 51b: Agilent N4903A auto alignment

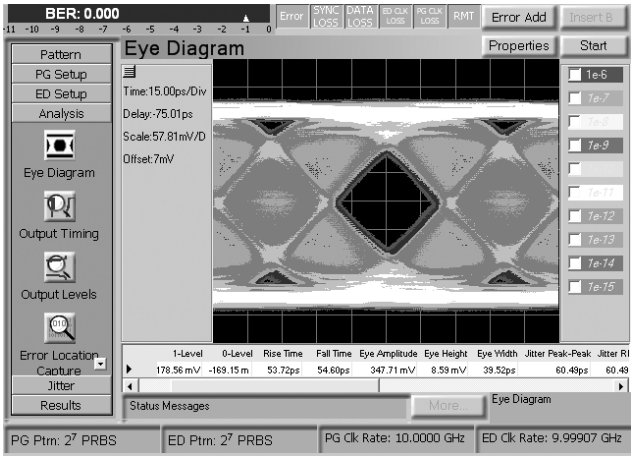


Figure 52b: Agilent N4903A eye diagram

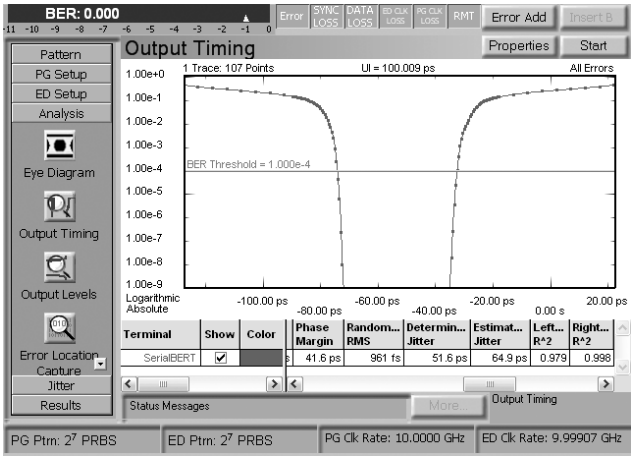


Figure 53b: Agilent N4903A BERT scan measurement

Data Rate: 2.5 Gb/s

PJ (periodic jitter), 2.5 Gb/s

Periodic jitter is induced by selecting the periodic button and specifying jitter amplitude, frequency and waveform. In this case, we selected .125 UI or 50 ps at a jitter frequency of 50 MHz and a sinusoidal waveform, as shown in figure 57.

Findings

The results agree with the expectations for the Auto Align, the eye width reading in the eye diagram and the RJ, DJ and TJ readings of the output timing measurement.

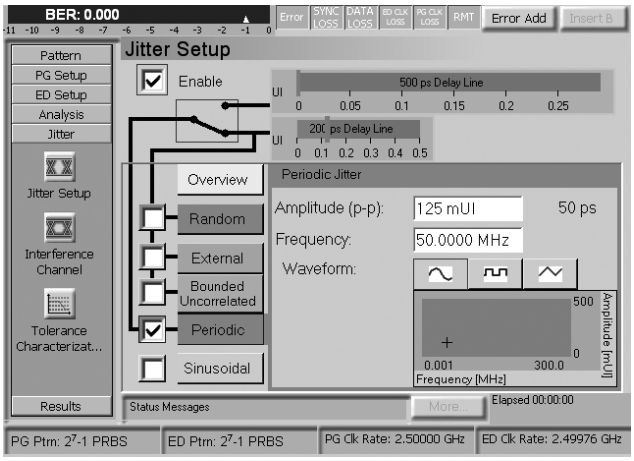


Figure 57: Periodic jitter setup on the Agilent N4903A

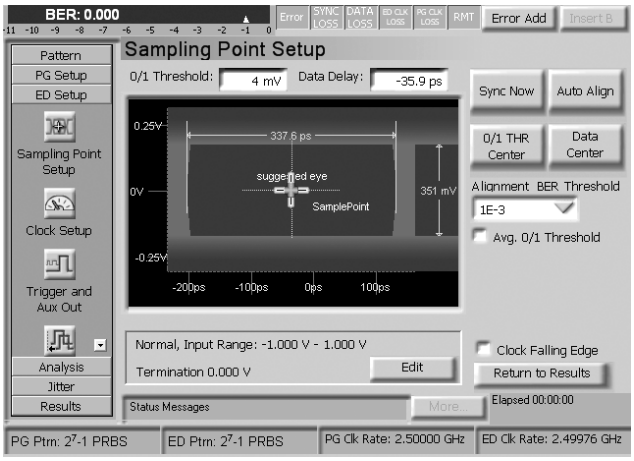


Figure 58: Agilent N4903A auto alignment

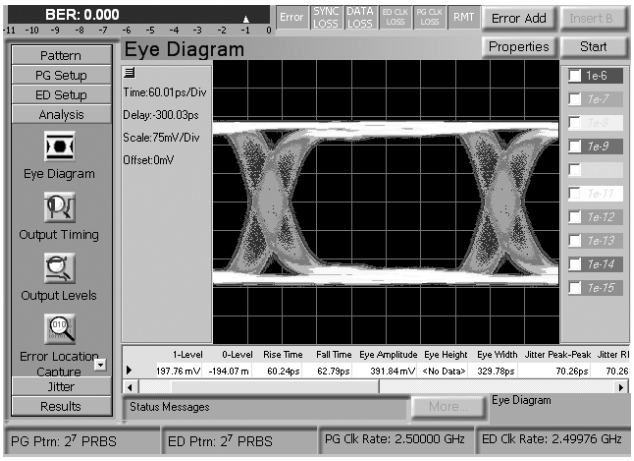


Figure 59: Agilent N4903A eye diagram

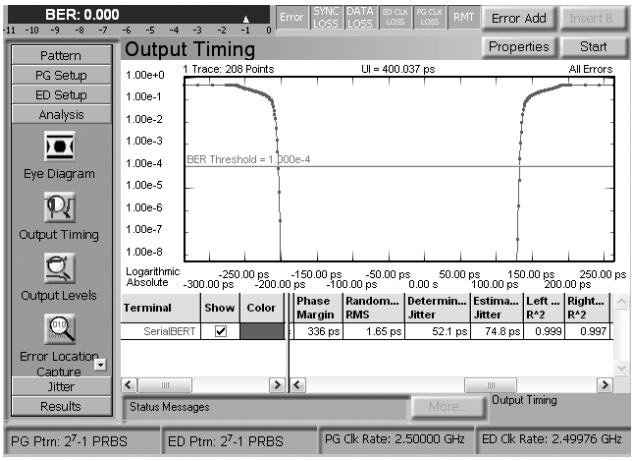


Figure 60: Agilent N4903A BERT scan measurement

Data Rate: 10 Gb/s

PJ (periodic jitter), 10 Gb/s

In this case, we selected .125 UI or 12.5 ps at a jitter frequency of 50 MHz and a sinusoidal waveform, as shown in figure 57b.

Findings

The results agree with the expectations for the Auto Align, the eye width reading in the eye diagram and the RJ, DJ and TJ readings of the output timing measurement.

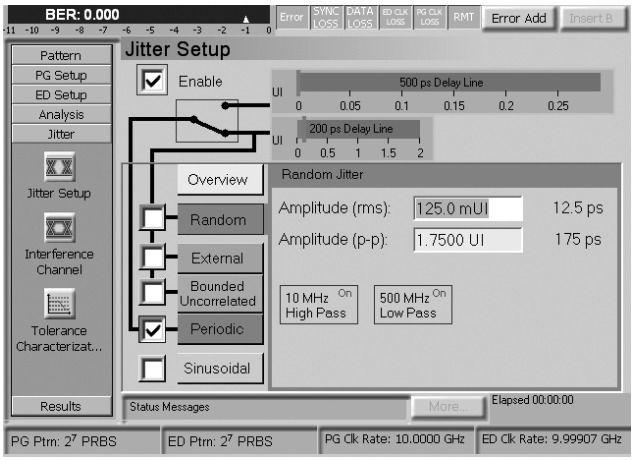


Figure 57b: Periodic jitter setup on the Agilent N4903A

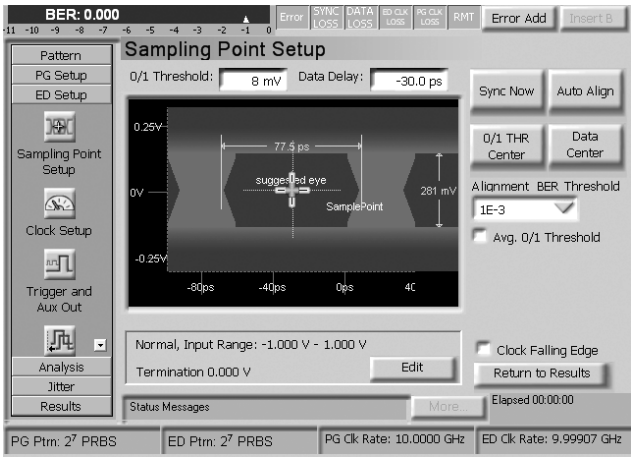


Figure 58b: Agilent N4903A auto alignment

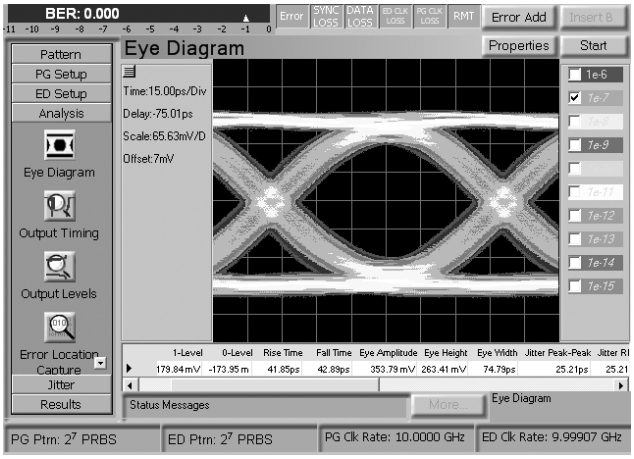


Figure 59b: Agilent N4903A eye diagram

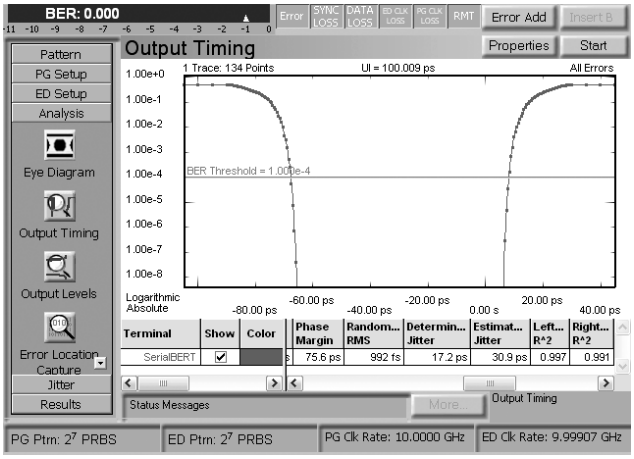


Figure 60b: Agilent N4903A BERT scan measurement

Data Rate: 2.5 Gb/s

RJ (random jitter), 2.5 Gb/s

Random jitter is controlled by the Random button. In this case, we set 7.2 ps rms or 100 ps pp. In theory, random jitter is infinite, so a pp value cannot be given, but practical noise sources are always bounded. The crest factor specifies the pp/rms ratio. Good, practical noise sources, such as the N4903A noise source, provide a crest factor of 14. A crest factor of 14 is equivalent of 7.2 ps rms which equals 100 ps pp jitter.

Findings

All results match well with expectations.

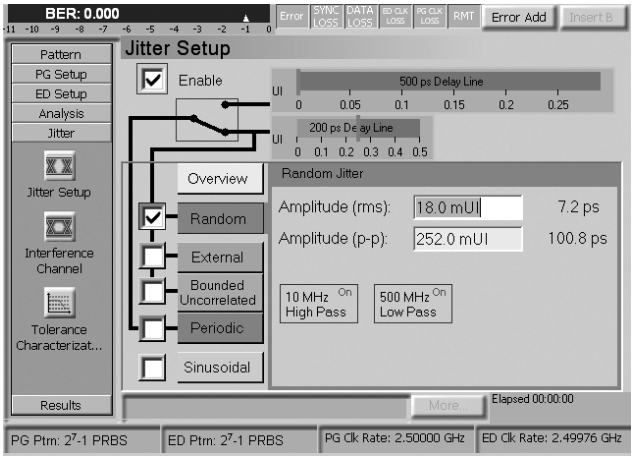


Figure 64: Random jitter Setup on the Agilent N4903A

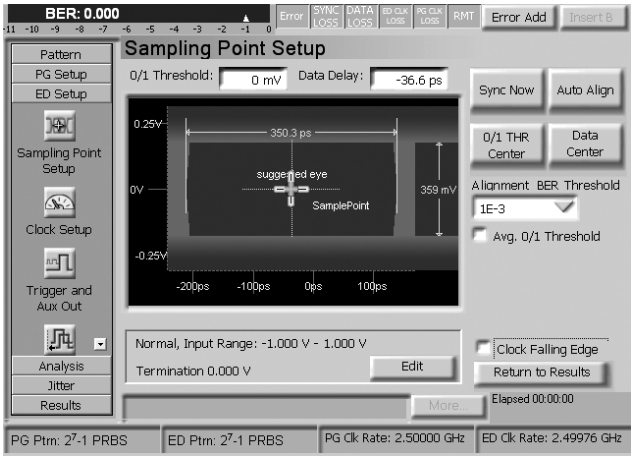


Figure 65: Agilent N4903A auto alignment

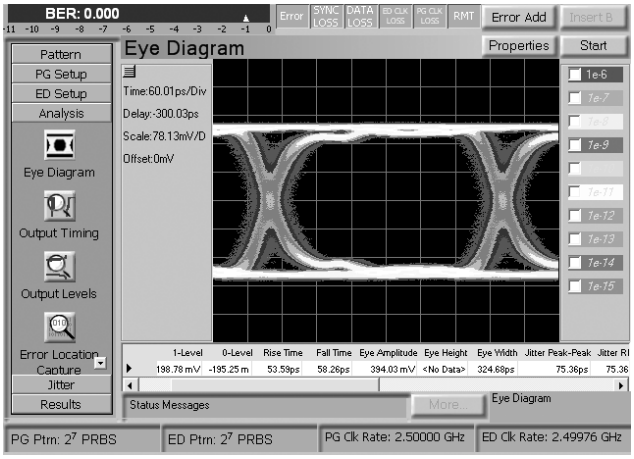


Figure 66: Agilent N4903A eye diagram

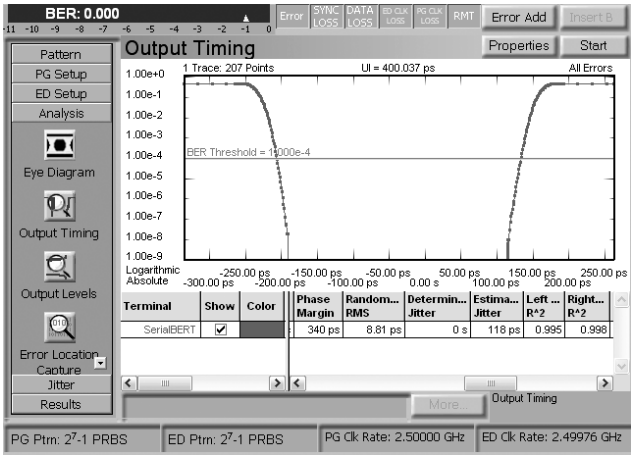


Figure 67: Agilent N4903A BERT scan measurement

Data Rate: 10 Gb/s

RJ (random jitter), 10 Gb/s

In this case, we set 1.8 ps rms or 25 ps pp. As the Auto Align is set for BER 1e -3, the reading there includes only 6x rms, not the total jitter. The eye diagram is configured for 1e-6, so a jitter of 10x rms is seen. The RJ/DJ separation sees the total amount of random jitter.

Findings

All results match well with expectations.

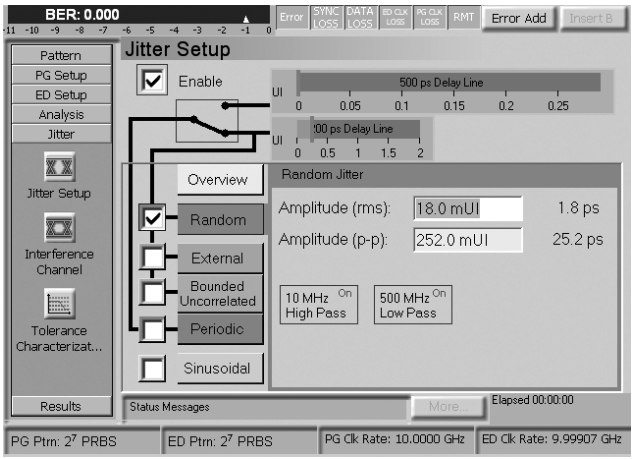


Figure 64b: Random jitter setup on the Agilent N4903A

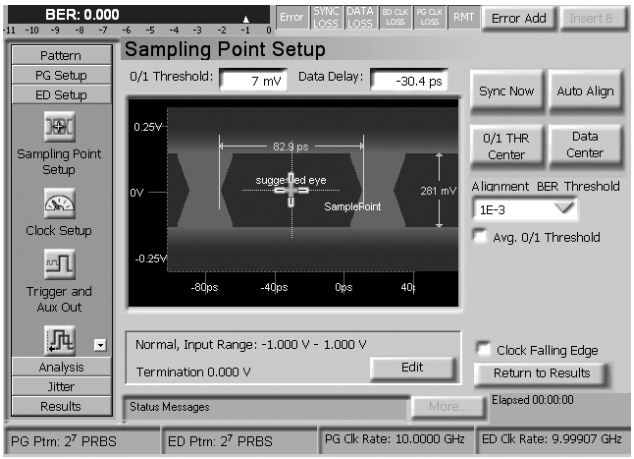


Figure 65b: Agilent N4903A auto alignment

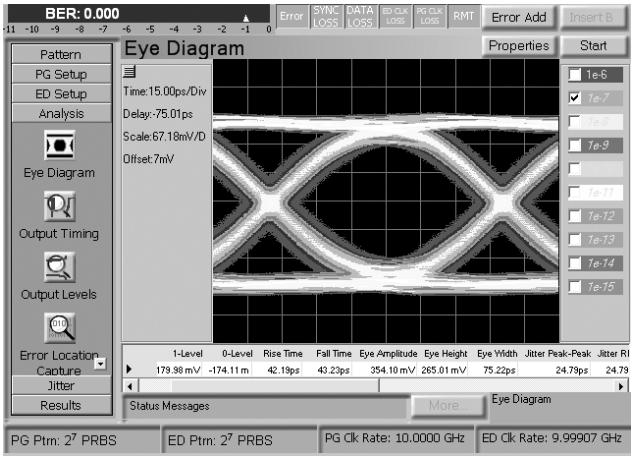


Figure 66b: Agilent N4903A eye diagram

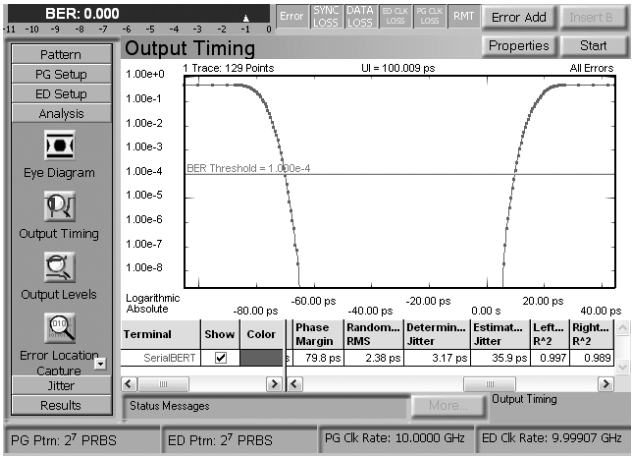


Figure 67b: Agilent N4903A BERT scan measurement

Data Rate: 2.5 Gb/s

BUJ (bounded uncorrelated jitter), 2.5 Gb/s
BUJ is generated by enabling the bounded uncorrelated. The parameters are the amplitude and the setting. The Gaussian setting sets the PRBS polynomial, the PRBS generation frequency and the filtering to achieve a bounded Gaussian distribution. Adjusting the PRBS polynomial, PRBS data rate and filtering can cause a non-bounded Gaussian distribution, so it is not recommended to change the Gaussian defaults. The jitter amplitude is set for 50 ps pp.

Findings
The results of the Auto Align and eye diagram are acceptable. The RJ/DJ separation is incorrect because the BUJ is not limited at 1e-4, so the RJ is over-extrapolated and consequently the DJ is under-extrapolated. The figure for TJ matches expectations.

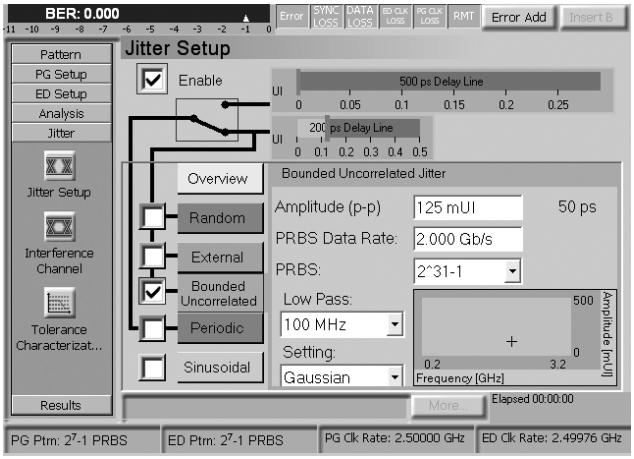


Figure 71: Bounded uncorrelated jitter setup on the Agilent N4903A

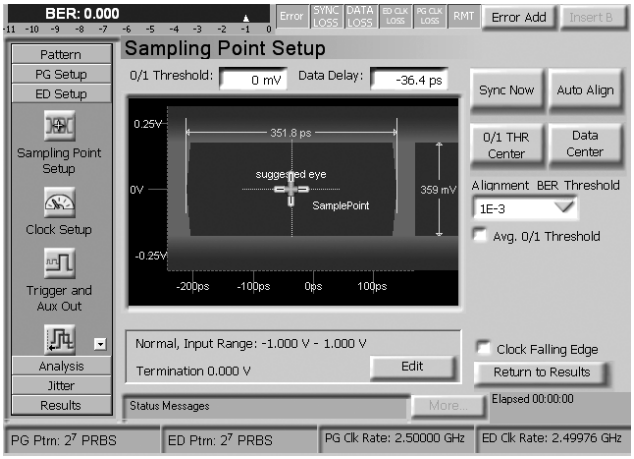


Figure 72: Agilent N4903A auto alignment

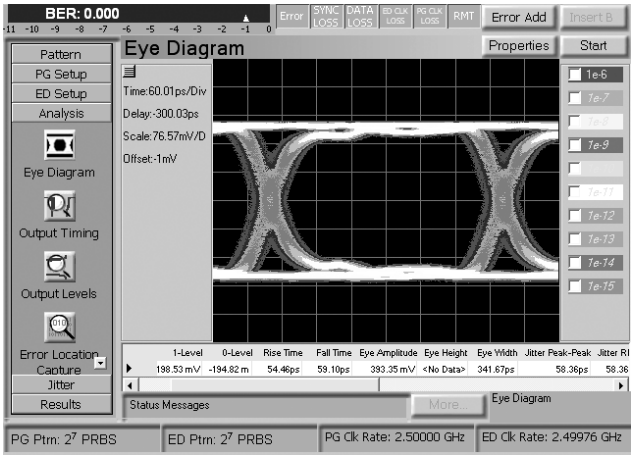


Figure 73: Agilent N4903A eye diagram

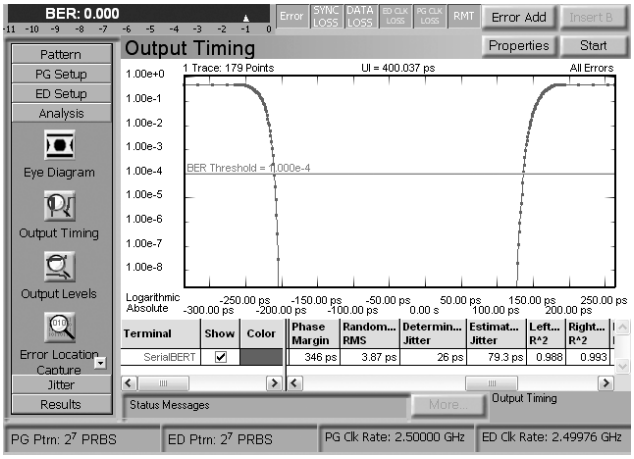


Figure 74: Agilent N4903A BERT scan measurement

Data Rate: 10 Gb/s

BUJ (bounded uncorrelated jitter), 10 Gb/s
The setup here uses a jitter amplitude of 12.5 ps pp.

Findings
The readings of Auto Align and eye diagram are acceptable. The RJ/DJ separation is incorrect because the BUJ is not limited at 1e-4, so the RJ is over-extrapolated and consequently the DJ is under-extrapolated. The TJ result is as expected.

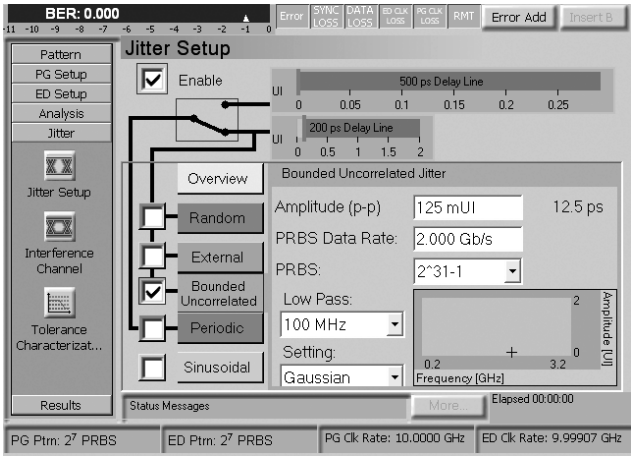


Figure 71b: Bounded uncorrelated jitter setup on the Agilent N4903A

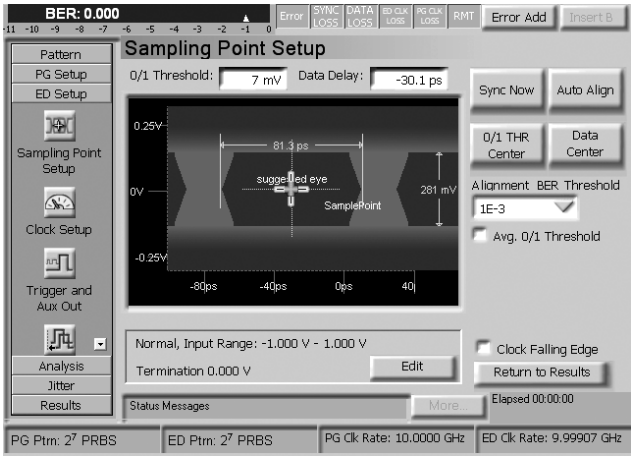


Figure 72b: Agilent N4903A auto alignment

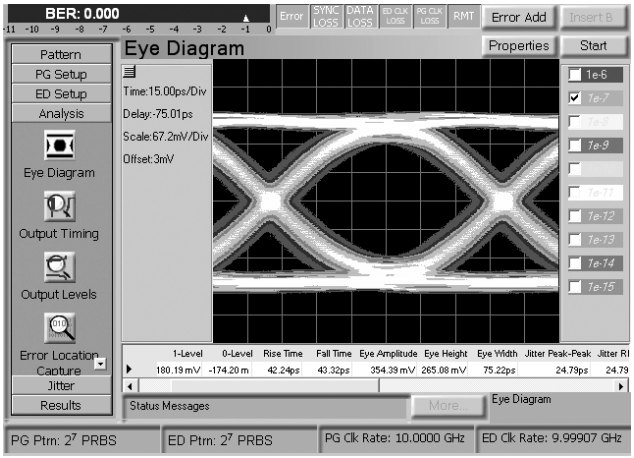


Figure 73b: Agilent N4903A eye diagram

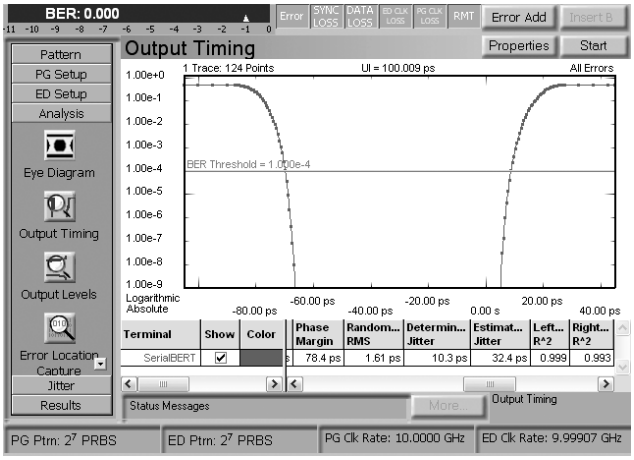


Figure 74b: Agilent N4903A BERT scan measurement

Data Rate: 2.5 Gb/s

Noise (amplitude noise), 2.5 Gb/s

Amplitude noise also causes timing jitter as the modulated level changes the starting point for the transition. The faster the transition, the less the jitter. This setup uses 150 mV noise which creates a timing jitter of .125 UI or 50 ps. This includes 15 ps ISI generated by using trace #1.

Findings

The results agree with the expectations for the Auto Align and the eye width reading in the eye diagram. The RJ/DJ separation shows that part of the noise is reflected in the RJ value, while the total jitter is as expected.

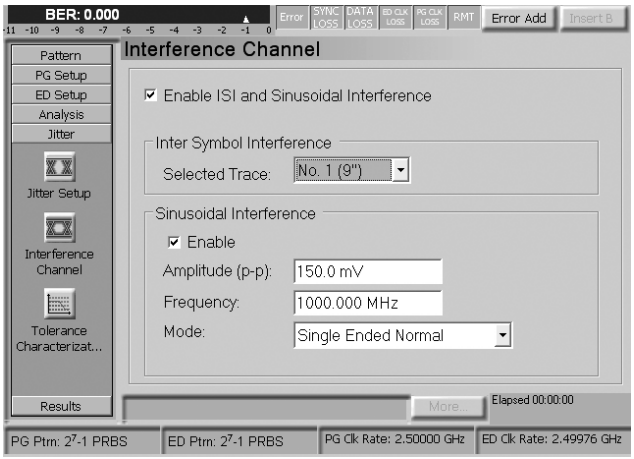


Figure 78: Amplitude noise setup on the Agilent N4903A

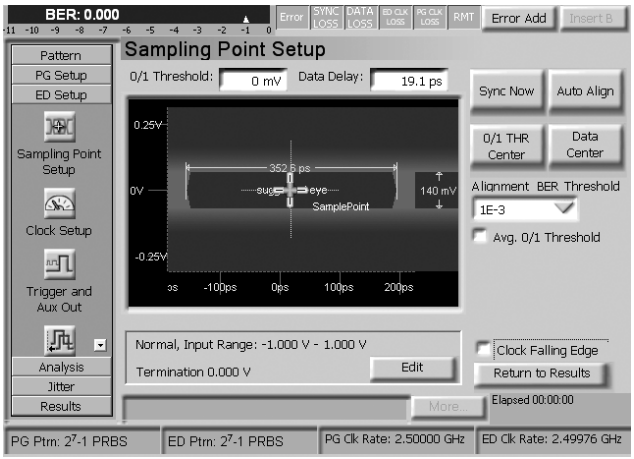


Figure 79: Agilent N4903A auto alignment

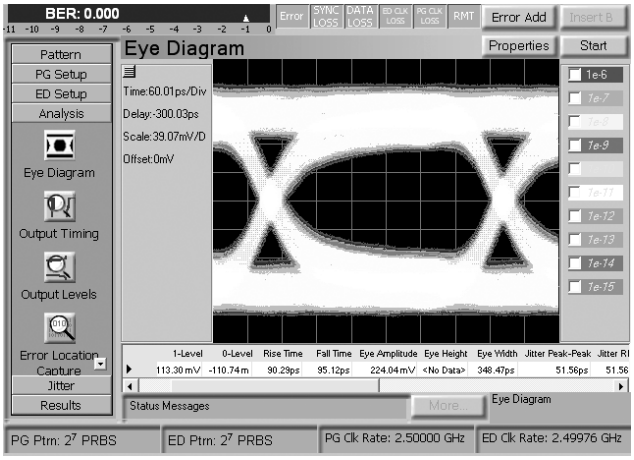


Figure 80: Agilent N4903A eye diagram

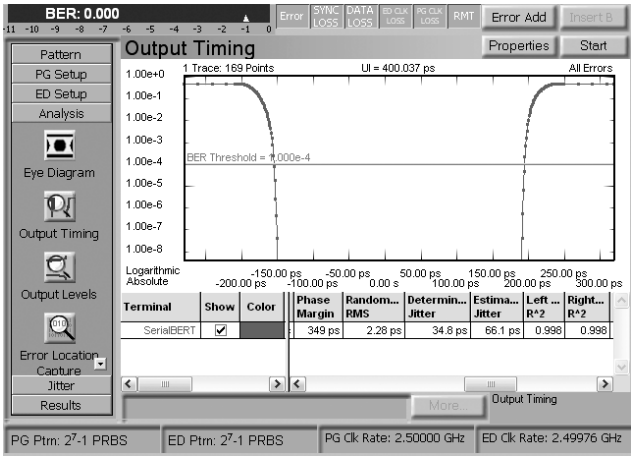


Figure 81: Agilent N4903A BERT scan measurement

Data Rate: 10 Gb/s

Noise (amplitude noise), 10 Gb/s

This setup uses 50 mV amplitude noise, which creates a timing jitter of .42 UI or 42 ps. This includes 30 ps ISI caused by trace #1.

Findings

The results agree with the expectations for the Auto Align and the eye width reading in the eye diagram. The RJ/DJ separation shows that part of the SI/noise is reflected in the RJ value, while the total jitter is as expected.

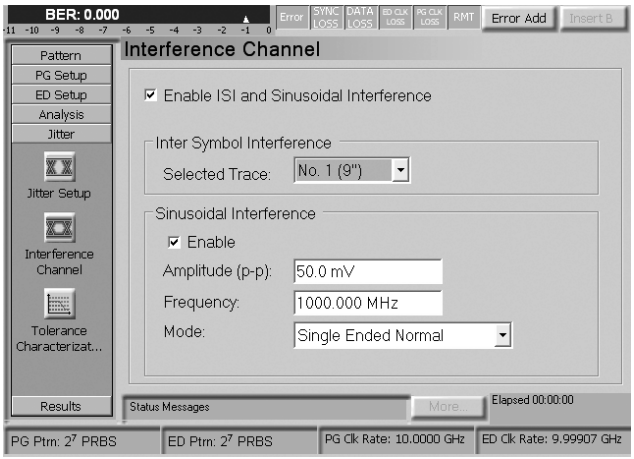


Figure 78b: Amplitude noise setup on the Agilent N4903A

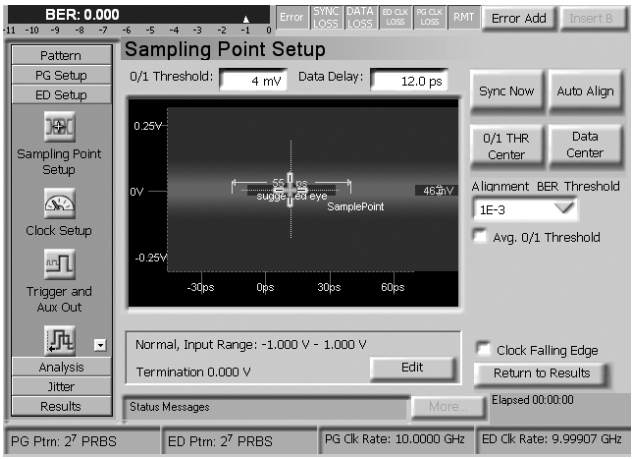


Figure 79b: Agilent N4903A auto alignment

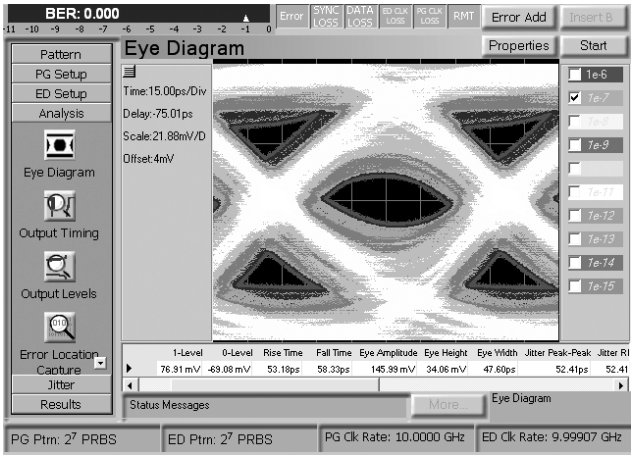


Figure 80b: Agilent N4903A eye diagram

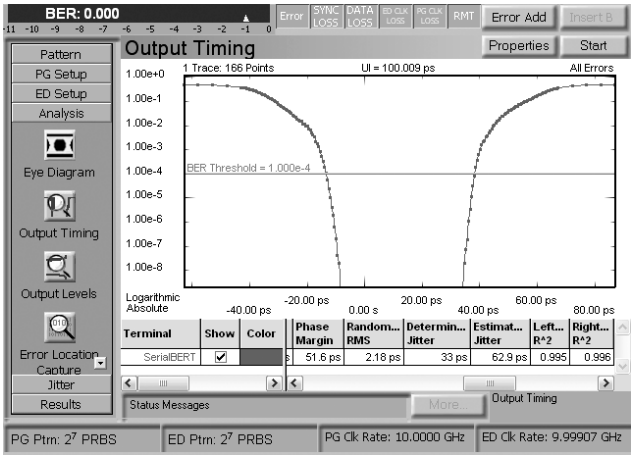


Figure 81b: Agilent N4903A BERT scan measurement

Data Rate: 2.5 Gb/s

Stressed eye, 2.5 Gb/s

This setup combines three jitter components:

- 10% Random Jitter (40 ps pp – 2.9 ps rms)
- 15% ISI (trace #3)
- 10% Noise (100mV)

It is recommended to set up the signal in two steps: First enable ISI and add noise to close the eye by the needed amount. Second add the RJ. The total jitter is .35 UI or 140 ps pp.

Findings

The results agree with the expectations for the Auto Align and the eye width reading of the eye diagram. The RJ/DJ separation over-extrapolates the RJ value, while the total jitter is as expected.

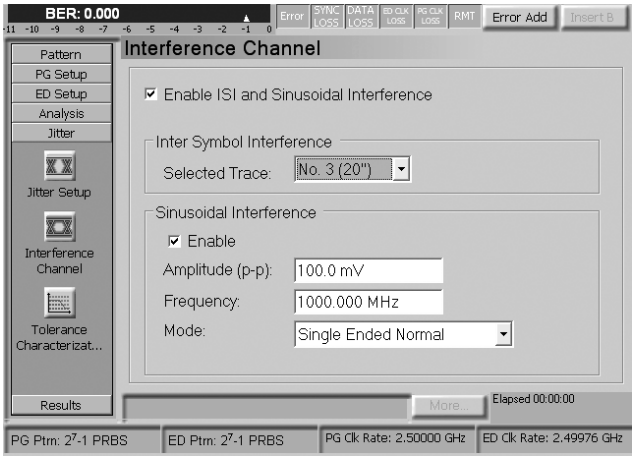


Figure 85: Stressed eye setup, step 1, on the Agilent N4903A

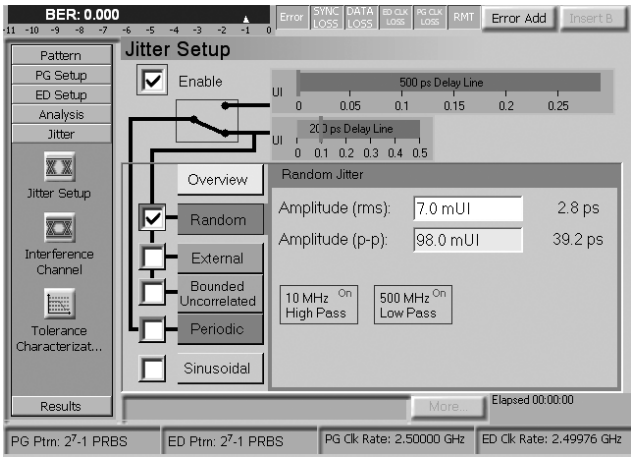


Figure 86: Stressed eye setup, step 2, on the Agilent N4903A

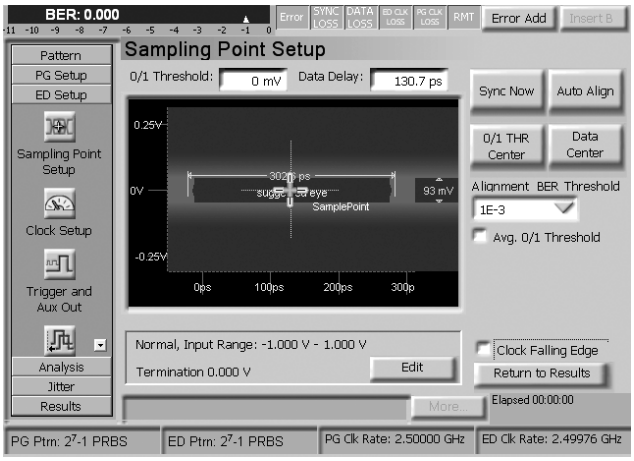


Figure 87: Agilent N4903A auto alignment

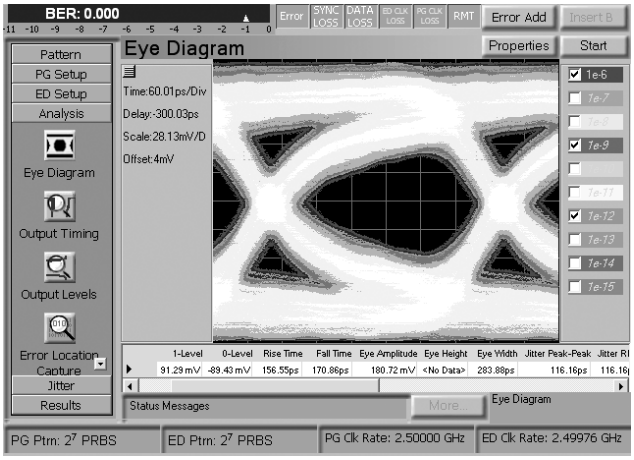


Figure 88: Agilent N4903A eye diagram

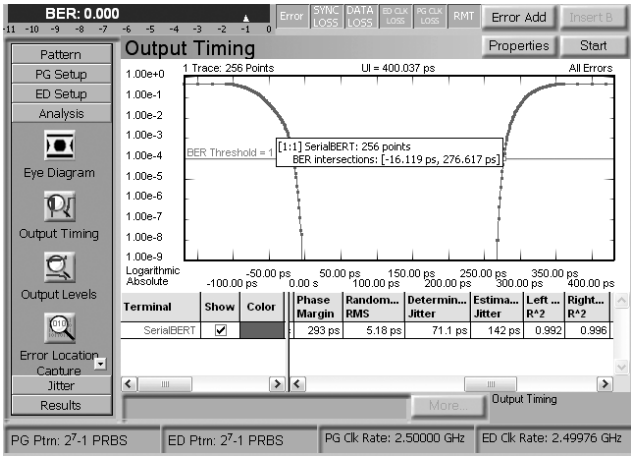


Figure 89: Agilent N4903A BERT scan measurement

Data Rate: 10 Gb/s

Stressed eye, 10 Gb/s

This setup combines three jitter types:

- 10% Random Jitter (10 ps pp)
- 30% ISI (trace #1)
- 5% Noise (50mV)

It is recommended to set up the signal in two steps: First enable ISI and add noise to close the eye by the needed amount. Second add the RJ. The total jitter is .35 UI or 35 ps pp

Findings

The results agree with the expectations for the Auto Align and the eye width reading of the eye diagram. The RJ/DJ separation over-extrapolates the RJ value, while the total jitter is as expected.

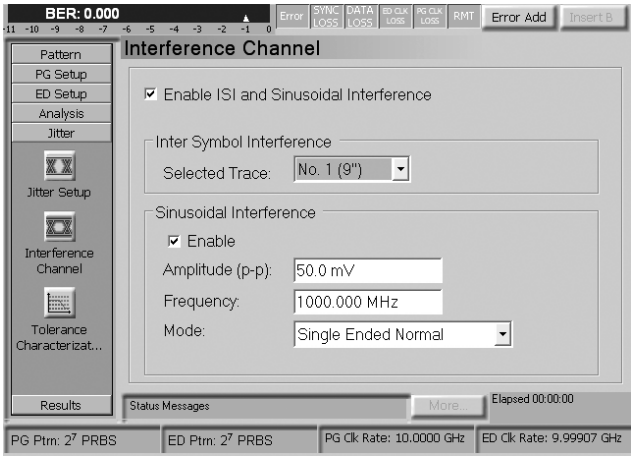


Figure 85b: Stressed eye setup, step 1, on the Agilent N4903A

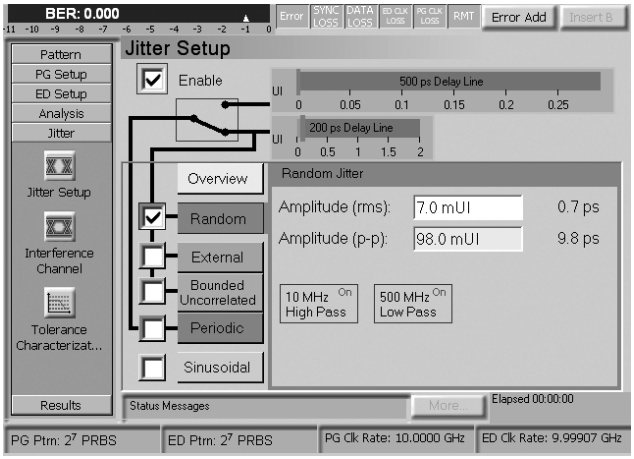


Figure 86b: Stressed eye setup, step 2, on the Agilent N4903A

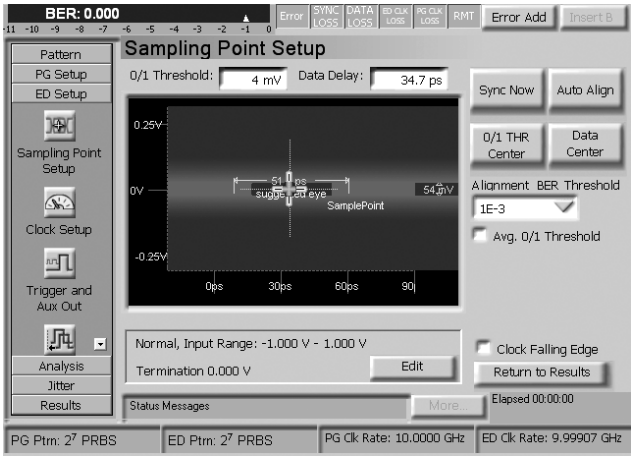


Figure 87b: Agilent N4903A auto alignment

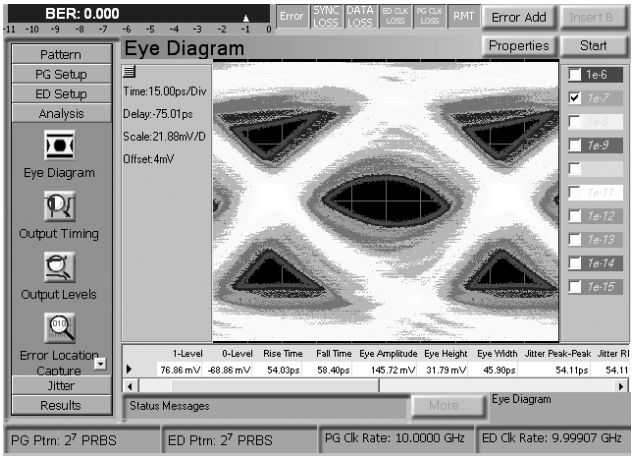


Figure 88b: Agilent N4903A eye diagram

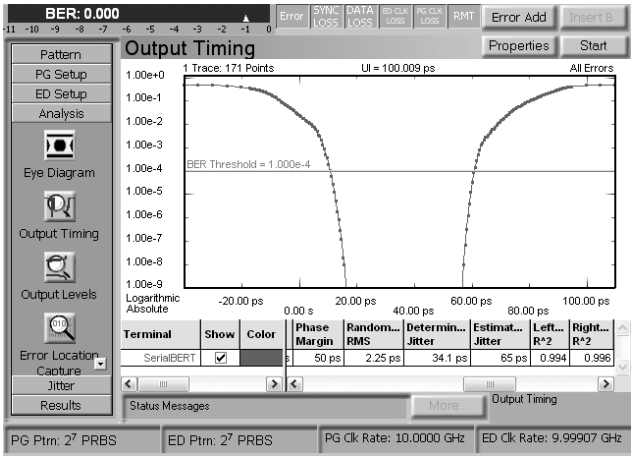


Figure 89b: Agilent N4903A BERT scan measurement

References:
[1] PCI Express® 2.0 Base Specification
[2] IEEE P802.3ae
[3] FB-DIMM High Speed Differential PTP Link Specification
[4] Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O, OIF-CEI-02.0
[5] J-BERT N4903A High-Performance Serial BERT Data Sheet

Related Literature	Publication Number
J-BERT N4903A High-Performance Serial BERT Brochure	**5989-3882EN**
Bit Recovery Mode for characterizing idle and framed data traffic Application Note	**5989-3796EN**
Second Generation PCI EXPRESS® Testing with the N4903A High-Performance Serial BERT Application Note	**5989-4087EN**
N4906B Serial BERT 3 and 12.5 Gb/s Data Sheet	**5989-2406EN**
Mastering Jitter in Serial Gigabit Designs Poster	**5989-4823EN**
Agilent Physical Layer Test Brochure	**5988-9514EN**
ParBERT 81250 Product Overview	**5968-9188E**
86100 Infiniium DCA-J Data Sheet	**5989-0278EN**
Infiniium 80000 Series Oscilloscopes Data Sheet	**5989-1487ENUS**
Fast Total Jitter Solution Application Note	**5989-3151EN**
Jitter Analysis: The dual-dirac model, RJ/DJ and Q-scale White Paper	**5989-3206EN**

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