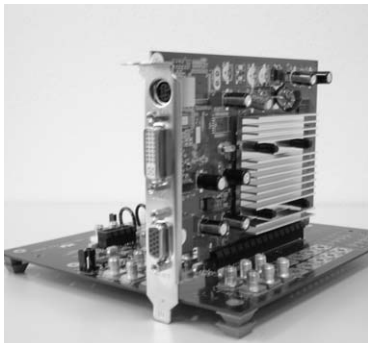
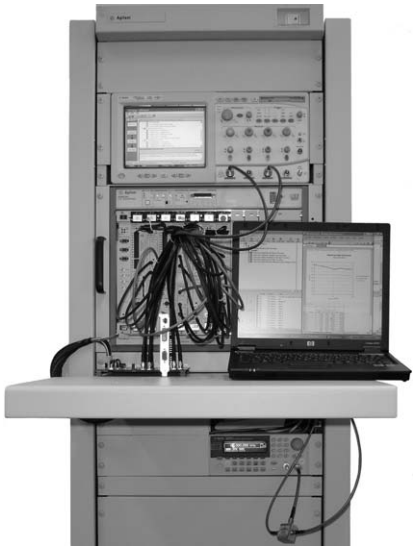
Automated PCI Express Receiver Compliance Test and Characterization with the Agilent N5990A Software Platform

Product Note





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Introduction

Industry standard committees, such as the PCI-SIG®, the PCI special interest group, define tests, which products that want to support the standard must pass. These compliance tests ensure interoperability and are mandatory to achieve the official certification. Typically, compliance tests comprise transmitter, receiver and cable tests.

Compliance tests often cover static or low-speed as well as high-speed parameters. For digital high-speed buses, with data rates of 1 GHz or higher, the receiver jitter tolerance test is the most important high-speed test (Fig. 1).

Some compliance tests only deliver a pass/fail result. To evaluate a DUT fully, for example to check the device's margins, you need to conduct characterization tests, by systematically varying test parameters with user-selectable step width and parameter ranges. For a summary about the specific challenges of digital high-speed testing, see for example reference [1].

During R&D cycles you often perform pre-compliance tests and characterizations manually. Systematic design validation tests and tests provided by authorized test centers or compliance test labs are usually automated. Automated compliance tests and characterization require high test-throughput, repeatability and convenient control as well as advanced data management.

Agilent Technologies' N5990A Test Automation Software Platform facilitates automated compliance tests and characterization. It leverages the investment in physical layer test equipment for use with multiple high-speed bus standards by providing a generic test structure and user interface.

The software platform provides a high level of test integration and throughput, as well as ease-of-use. The N5990A's receiver test options offer dedicated receiver tests for popular and emerging digital buses. These libraries complement Agilent's portfolio of transmitter test software applications, such as N5393A for PCI Express®.

N5990A combines the performance of advanced test instruments with the convenience of PC control. It makes electrical testing of devices, such as PCI Express receivers, quicker, more thorough, and less expensive than manual testing. Example target devices are PCI Express bridges, network adapters, DSP, TV and data acquisition cards as well as evaluation or development boards.

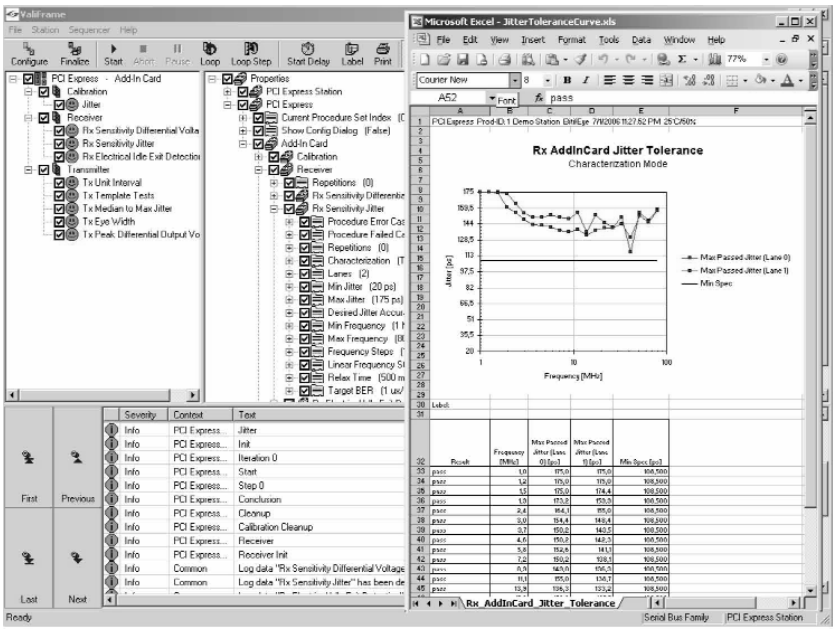

Figure 1: Receiver jitter tolerance test.

Automated Compliance Tests with N5990A

The N5990A Test Software Automation Platform provides compliance tests for multiple high-speed digital bus standards, and supports a wide range of standard instruments (Fig. 2). It complements electrical transmitter compliance tests running on oscilloscopes with receiver compliance tests running on stimulus instruments such as pattern generators or bit error ratio testers (BERTs).

This product note discusses the example of PCI Express compliance tests. Transmitter tests are conducted with the N5393A software on an oscilloscope as described in [2]. N5990A's option 201 exclusively provides remote control for the transmitter tests and loads the test results onto the PC.

N5990A's option 101 automates testing PCI Express receivers as discussed in the following. To accomodate any requirements beyond the standard tests, for example with regard to DUT conditioning or the generation of specific test plans, contact Agilent or the partner BitifEye Digital Test Solutions. (http://www.bitifeye.com)

This example uses a multi-lane add-in graphics card, as shown on the cover page, as a DUT. To conduct simultaneous measurements on multiple lanes, the 81250A ParBERT is used as the hardware front-end.

The most important test is the receiver jitter tolerance test. For PCI Express 1.0a, it is part of the receiver sensitivity test, defined in 4.1.21 of the PCI Express Architecture PHY Electrical Test Considerations (Rev. 1.0). The differential voltage test is part of the receiver sensitivity test too.

A configuration example for automated PCI Express receiver sensitivity tests is shown in Fig. 3. It assumes no switch matrix is available and consists of two 3.3 Gb/s generators with jitter insertion and two analyzers for the parallel jitter tolerance test on lane 0 and 1. On lane 2, it conducts the differential voltage test using two 2.7 Gb/s generators.

Two more 2.7 Gb/s generators provide the master clock for synchronizing the ParBERT generators and analyzers, and the 100 MHz PCI Express reference clock.

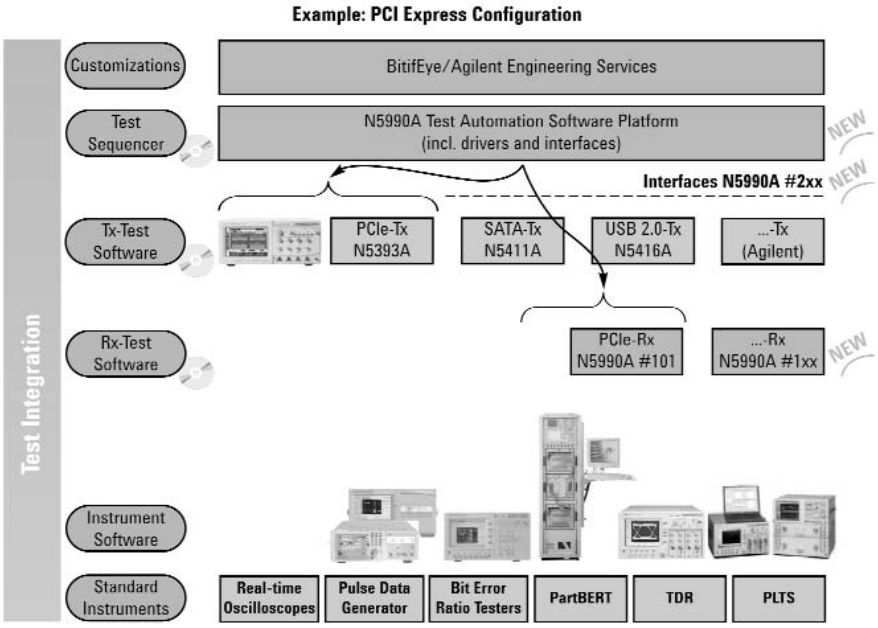

Figure 2: N5990A test platform.

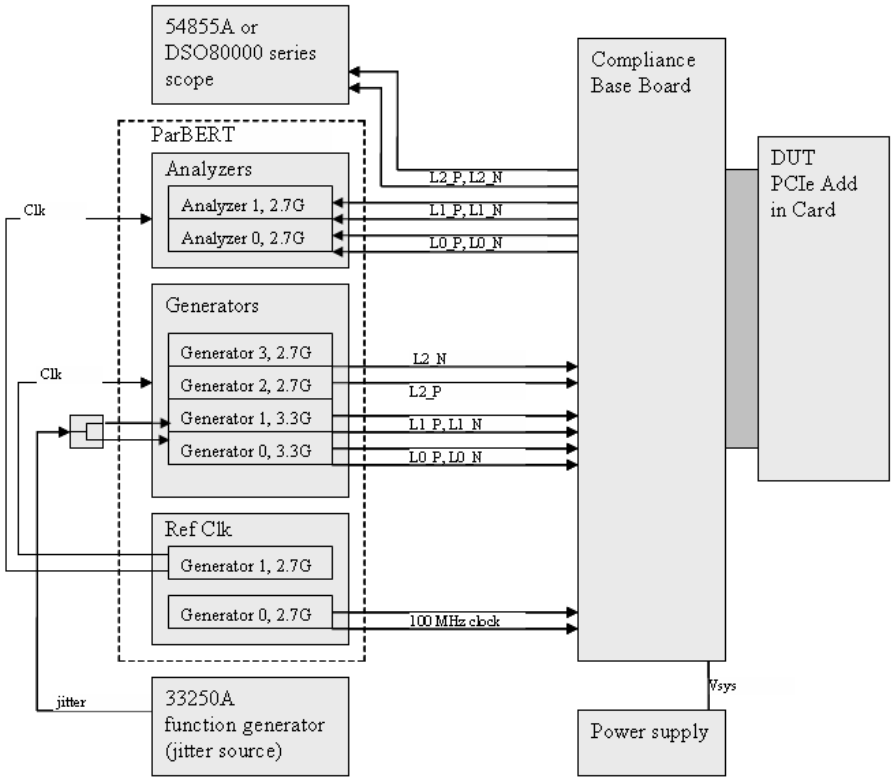

Figure 3: ParBERT configuration for multi-lane PCI Express add-in card receiver physical layer compliance tests.

The DUT add-in card is seated in a compliance baseboard (see Fig. 4), available from the PCI-SIG.

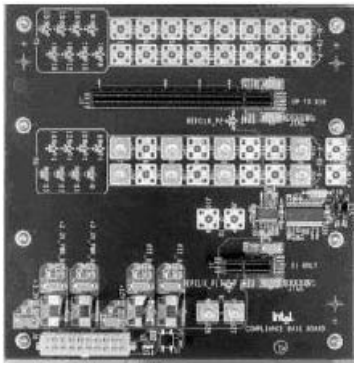

Figure 4: Compliance base board (CBB) for testing add-in cards.

After connecting the test hardware, you select the receiver sensitivity tests in the N5990A main menu (Fig. 5). The N5990A's characterization mode gives expert users full control over a wide range of test parameters and provides detailed status information.

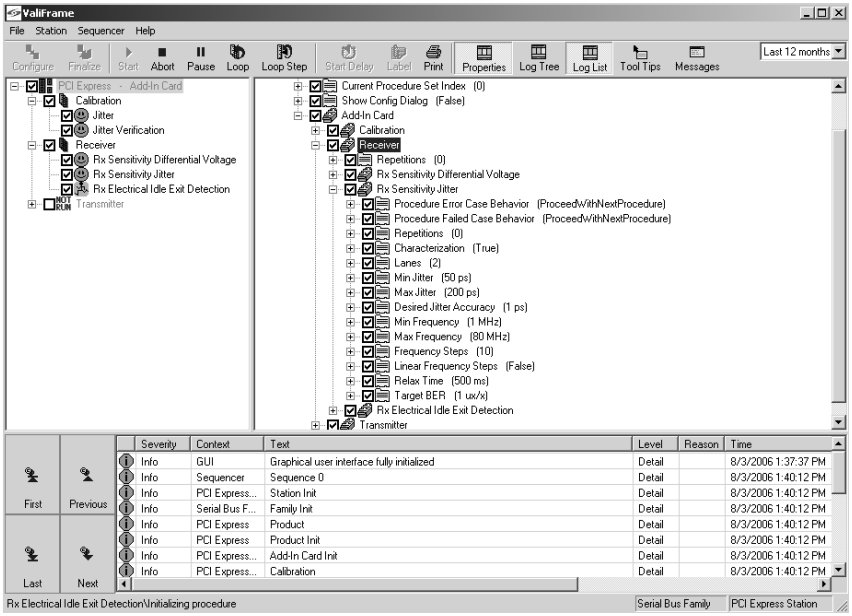

Figure 5: N5990A main menu (characterization mode).

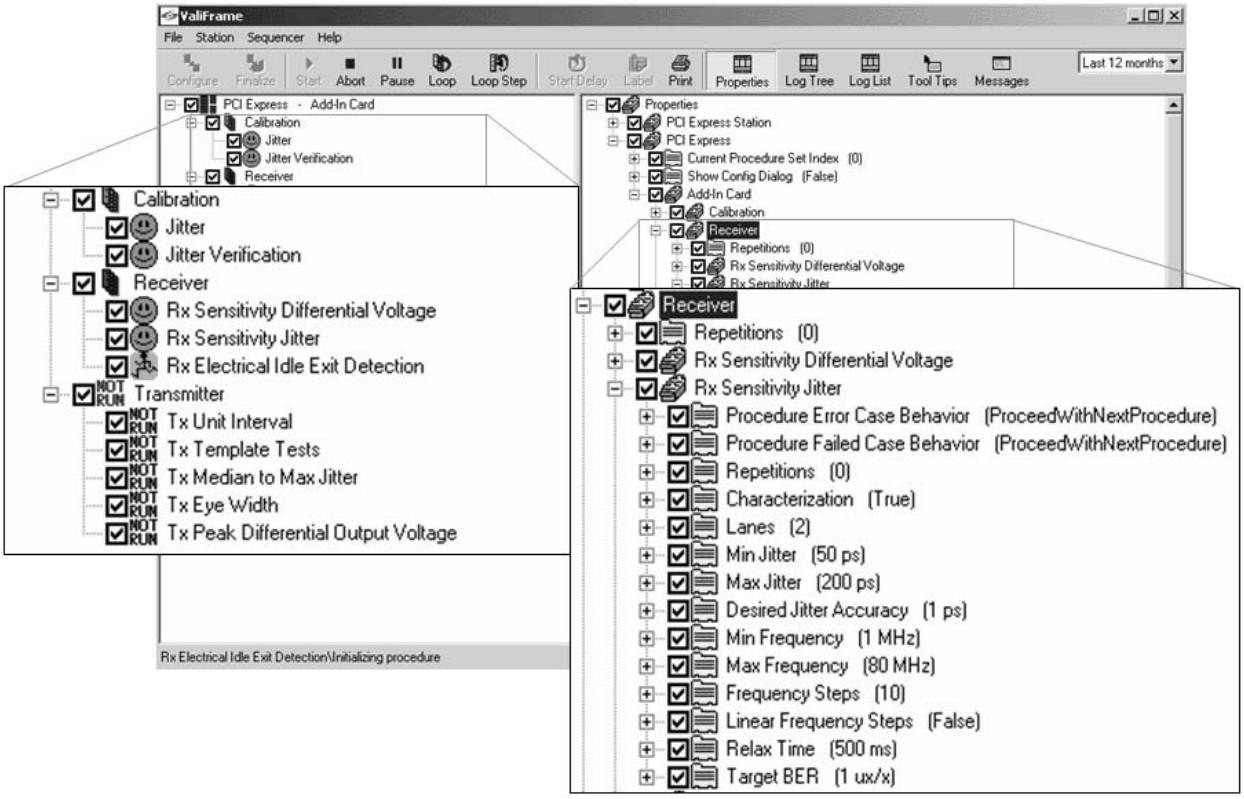

Figure 6: Jitter tolerance test parameter selections.

The differential voltage test sets the DUT to loopback mode, using the link training and status state machine. It sends a specified number of TS2 and TS1 ordered sets with asserted loopback-bit to each lane with a receiver connected to its output. It then applies the compliance pattern and measures bit error ratio (BER). The voltage is systematically decreased until it reaches the target BER, in practice between 10^{-6} and 10^{-12}.

The N5990A jitter tolerance test sets the DUT to loopback mode too. It also applies the compliance test pattern to the DUT. The DUT loops the pattern back to the BER analyzer. Sinusoidal jitter applied to the test pattern is increased gradually until the analyzer detects the user-selectable target BER. The test is repeated for a user-defined range of jitter frequencies.

Figures 6 and 7 show the user-selectable parameters, such as frequency range and step width that are available in characterization mode, as well as how to modify these parameters.

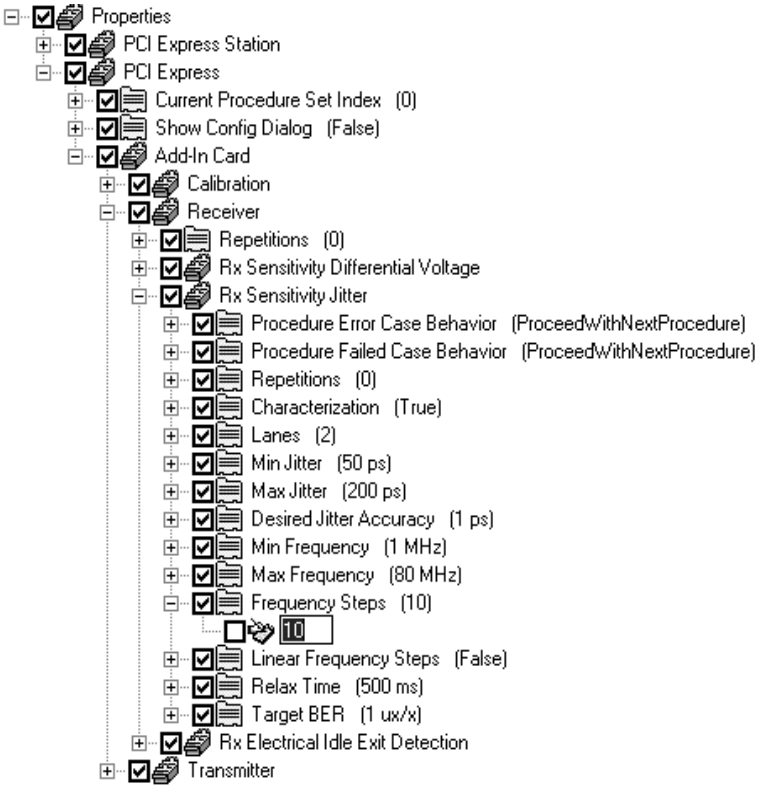

Figure 7: Parameter input.

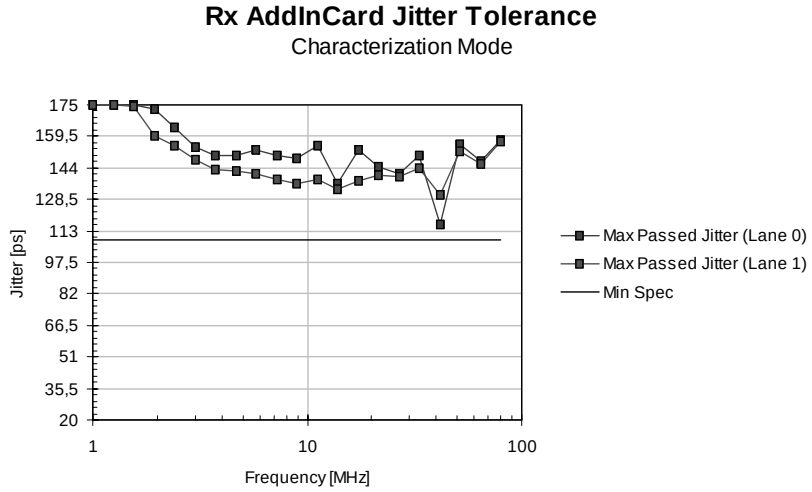

Figure 8: Dual-lane PCI Express receiver jitter tolerance test results.

The range of the jitter frequency depends on the jitter source. For example, these are between 100 kHz and 80 MHz if you are using a standard function generator, such as the Agilent 33250A. If you use a signal generator, such as the Agilent E4438C, the range extends from 100 kHz to 300 MHz.

The sinusoidal jitter amplitude ranges from 0 to 400 ps pp.

With the parameter selections shown above, you can conduct a dual-channel jitter tolerance test in a few minutes (subject to the stability of the DUT). A typical result is given in Fig. 8. The notches measured close to 40 MHz do not yet violate the threshold. However, in this case, we would recommend checking how this behavior varies with different DUTs.

Conclusion

Automated PCI Express transmitter compliance tests can now be matched and complemented conveniently with receiver tests.

References:

[1]: Schmitt, A., 9. Jan. 2005 *Testing serial gigahertz-speed buses*, EDN: http://www.edn.com/article/CA6250020.html

[2]: *PCI Express Transmitter Electrical Validation and Compliance Testing,* Agilent Technologies Application Note 1496, 5989-1275EN

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Related Literature	Publication Number
Test Automation Software Platform N5990A Data Sheet	**5989-5483EN**
Second Generation PCI EXPRESS with the J-BERT N4903A Application Note	**5989-4087EN**
Jitter Fundamentals: Jitter Tolerance Testing with 81250 ParBERT Application Note	**5989-0223EN**
Next Generation I/O Bus PCI-Express BER Test Solution Application Note	**5989-2690EN**
Physical Layer Testing of Passive Optical Network (PON) Modules Application Note	**5989-3298EN**
Jitter Fundamentals: ParBERT 81250 Jitter Injection and Analysis Capabilities Application Note	**5988-9756EN**

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