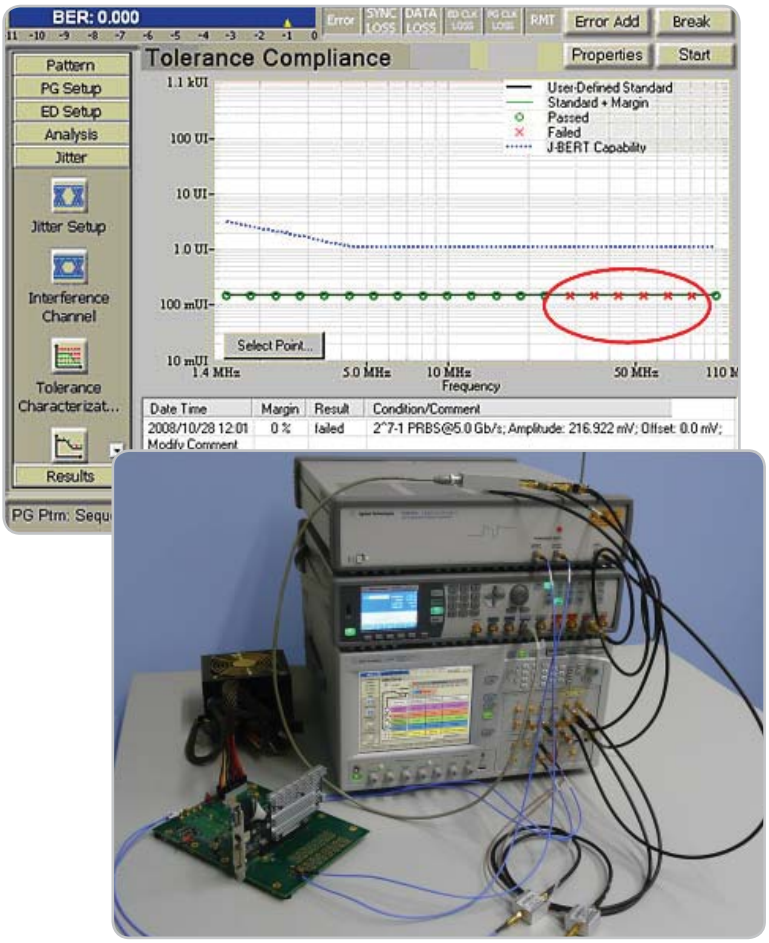
PCI Express® Revision 2.0 Receiver Testing

With J-BERT N4903A and 81150A Pulse Function Arbitrary Generator

Application Note

Agilent's PCIe™ 2.0 receiver test solution is the most flexible jitter tolerance test setup for today's and next generation needs:

- Use your standard J-BERT with Agilent N4916A and 81150A as an external noise source and as dedicated filters allowing PCI Express rev 2.0 compliant spectral RJ injection
- Compliant RX test signal with J-BERT's built-in jitter sources for PJ, ISI, SSC, common and differential mode noise
- Preparing DUTs for test and setting into loop back mode easily with J-BERT's flexible pattern sequencer
- Automated compliance tests with N5990A test automation software
- Accurate and sample-rich transmitter tests of total jitter and eye diagrams



Agilent Technologies

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1. Introduction

Data rates in the digital communication arena have crossed 10 Gb/s since long. Nowadays, computer buses and interfaces are on their way towards this speed class. PCI Express as an example, which is used as interface bus between CPU, bridge chips and the related peripherals (see Figure 1) is aiming at 8 Gb/s with its third generation.

Making such systems work reliably requires careful design of the related standards and thorough testing of the components that comprise these systems, i.e. ASICs, motherboards and add-in cards.

This document describes in-depth, how to verify current PCI Express rev. 2.0 5 Gb/s add-in cards with respect to the relevant CEM standard using the PCI-SIG® provided compliance base board and an Agilent J-BERT N4903A high-performance serial BERT. A step-by-step procedure is given for calibration of the required test signal and the compliance test itself; measurements beyond the pure RX-compliance tests are introduced at the end of this document. If this topic is your only interest, just read section 4 “Compliant test for add-in cards”, starting on page 13.

Figure 2 shows how PCIe Express “CEM-” relates to the “base-” specification and for which DUTs (chips, add-in cards and mother boards) which specification in which flavor (data clocked or common reference clock) is applicable.

Some theoretical background information highlighting the differences between the two clocking schemes (the so-called topologies) and the rationals for some specifications and test methods are described in the section entitled “Details of the PCI Express specification”.

To start with, a generic introduction to RX-jitter tolerance test and the related challenges is provided as well.

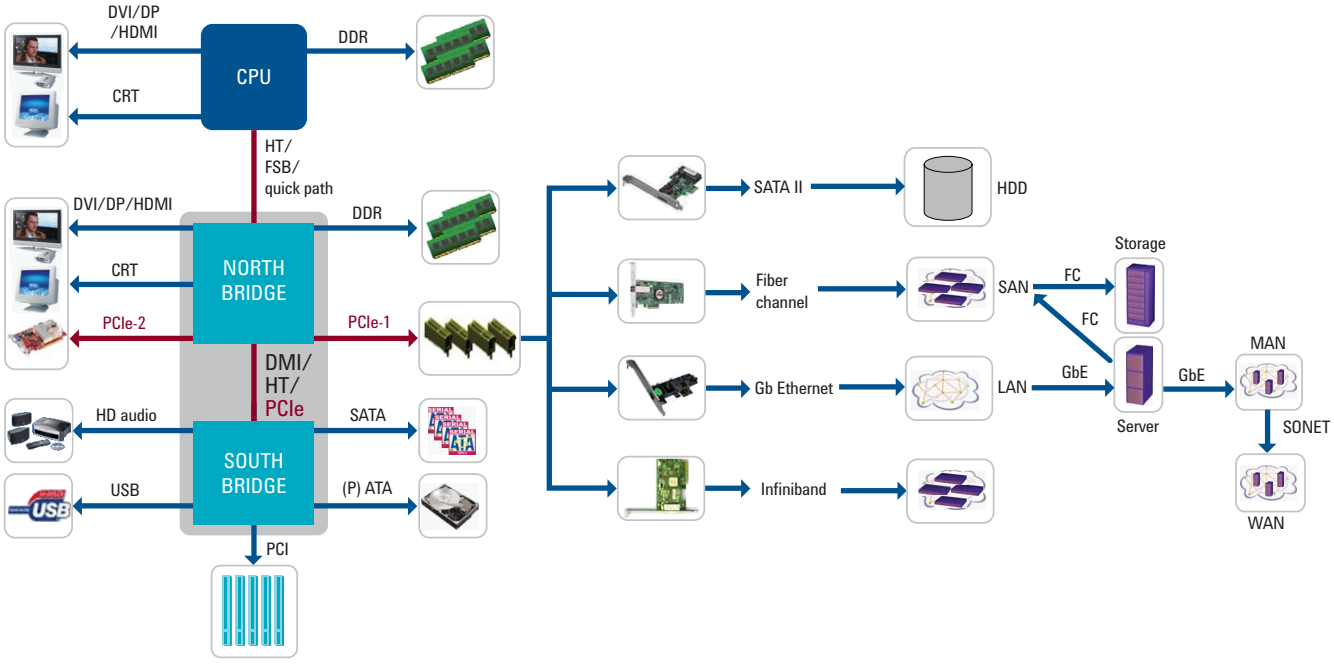


Figure 1. Generic computer block diagram

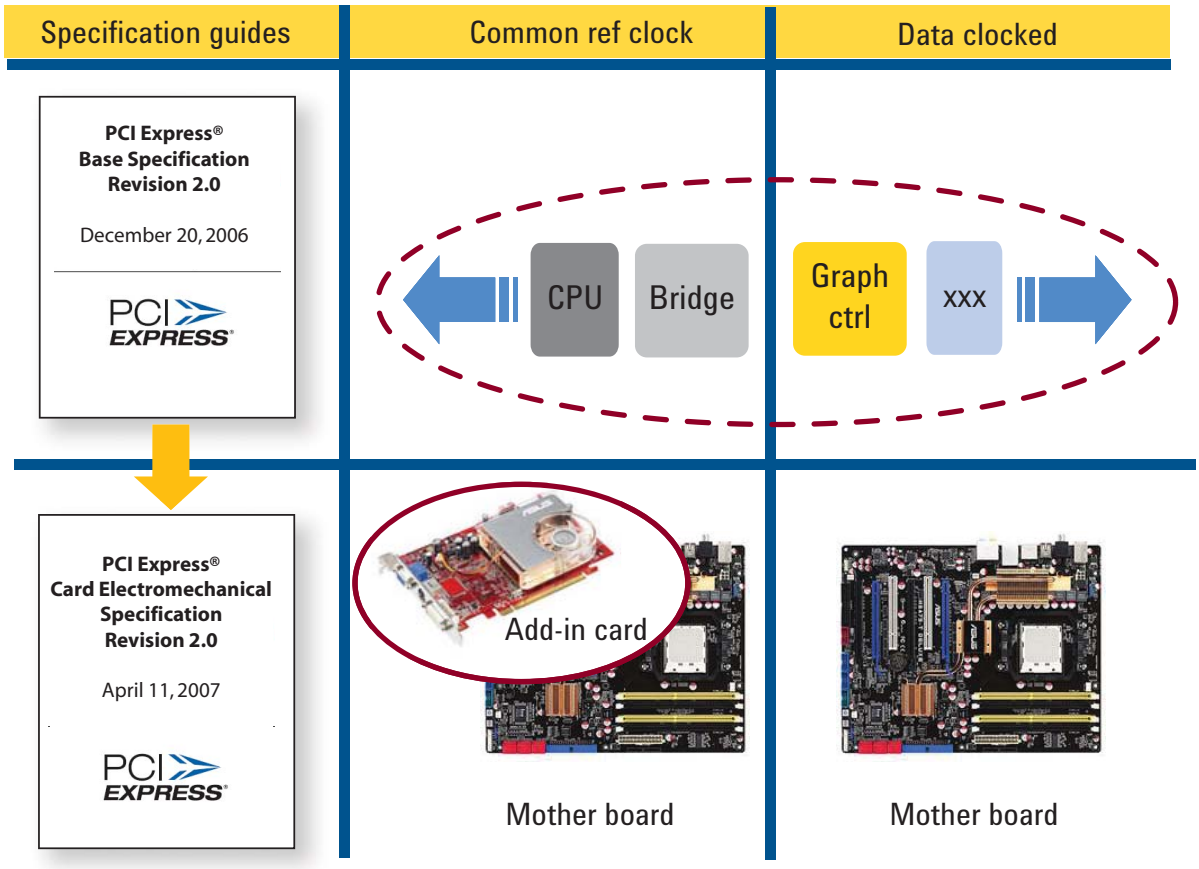


Figure 2. Relation between the different PCI Express specifications and the DUTs; topics to be discussed throughout this application note are circled above

2. Introduction to RX Jitter-Tolerance Test

Or why does RX-test seem so complicated in comparison to TX-test?

TX test is straight forward

In a digital transmission system the TX has to generate digital output signals with certain signal integrity. It may be that some parameters (amplitude, de-emphasis levels) are required to be adjustable. TX performance can directly be characterized or checked e.g. with an oscilloscope. Very often the TX generates test patterns by itself eliminating the need for a suitable pattern generator. The procedure is straightforward and identical for characterization and compliance test.

RX jitter tolerance test is recommended

The RX test is a bit more complicated, due to the DUT's task within a digital transmission system: the extraction of the digital content from its input signal with a specified, very low bit error ratio (BER); the difficulty of this task is, that the signal is heavily deteriorated after it left the (non-ideal) TX and propagated through a channel with low pass filter characteristic (see screen shots as of Figure 3).

The main building blocks of an RX, depicted in Figure 3 as well, are an (optional) equalizer, a differential limiting amp, a clock recovery (CR), a sample FF and a de-mux. The equalizer (EQ) can revert some of the channel effects that caused ISI and the clock recovery (CR) can track jitter within its bandwidth (BW) (why it is sometimes called jitter filter) to optimize the sampling point timing.

Therefore, judging alone from the RX-input eye-diagram, i.e. from signal amplitude (eye-height) and minimum pulse width (eye-width) and relating them to the classical RX performance determining properties such as limiting amp's sensitivity or sampling FF's t_{setup} + t_{hold}, whether the RX can properly perform its task, is impossible.

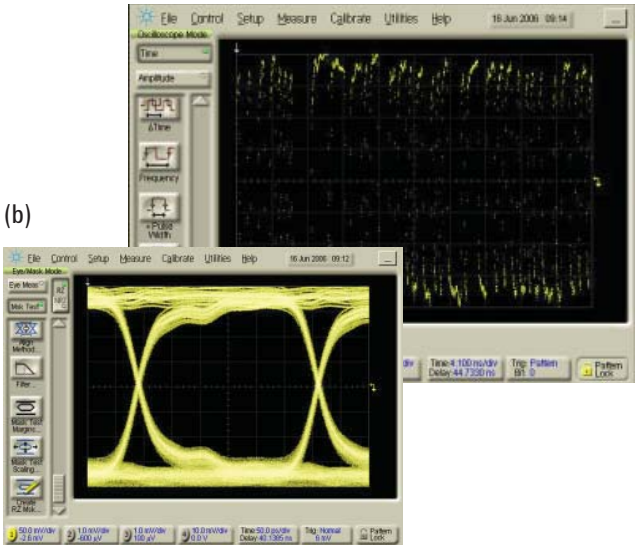
Properties of the RX jitter tolerance test

Usually a test is designed as a combination of a black-box and a white box test, such that (a) realistic conditions are emulated regardless of the RX's architecture and (b) certain properties of the test (-signal) deliberately stress specific building blocks of the DUT.

For example,

- Minimum levels are selected to stress the limiting amplifier's sensitivity
- Patterns with an isolated "1" or "0" are selected to stress the limiting amps's BW (minimum pulse-width acceptance)
- Certain patterns are selected to stress the CR's capability to deal with long sequences of consecutive identical bits (CID)
- Low frequency (in-band) jitter is selected to check the CR's tracking capability

(b)



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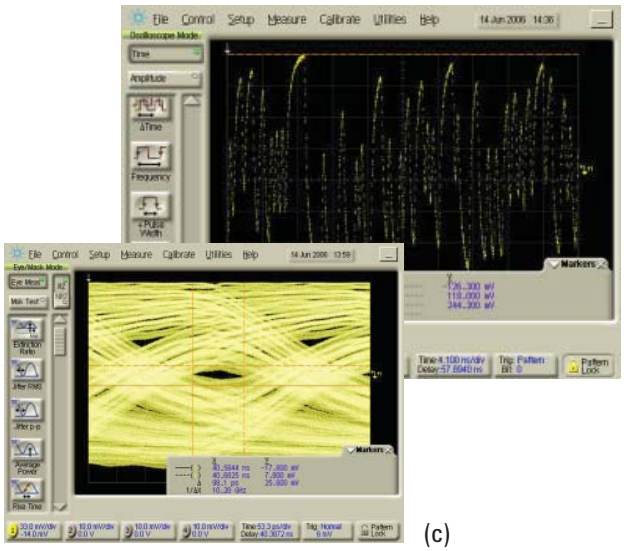


(a)

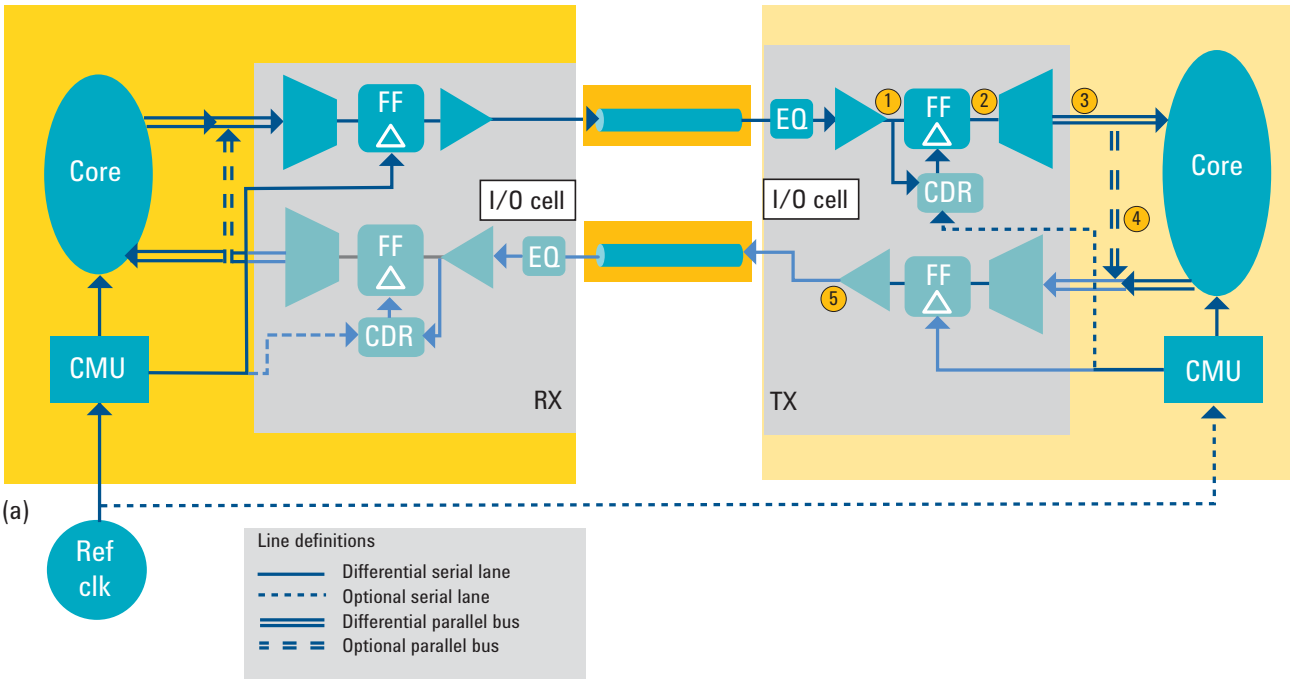


Figure 3. (a) Block diagram of TX and RX of a digital transmission system and related signals: (b) TX-output and (c) RX-input

Two-port testing required

Taking all this into account reveals that in order to test (check or characterize) the RX's capability of converting signals from the analog to the digital domain requires some sort of connection to both ports of the RX with suitable measurement gear.

The input port must be stimulated with a properly deteriorated signal, which requires a sophisticated generator. If not built-in or factory provided, calibration of impairments (jitter) can become quite complicated and tedious.

The output port (point [2] or [3] of Figure 3a) is usually not accessible: received bits need to be looped back [4] through the TX [5] for external error counting with a BERT's ED and this mode needs to be initiated through the RX-input by a certain bit sequence.

Test automation desired

The check to determine if a certain deterioration was tolerated with sufficiently low BER is already lengthy. The characterization of the RX's performance is not a straightforward procedure, rather a time consuming iterative process. This process consists of the following steps:

- Stimulate with a certain amount of jitter, measure the BER
- Depending upon the result (above or below the BER-limit) increase or decrease the amount of jitter
- Measure BER again and so on

To summarize the above: Enough obstacles to make the RX test the most unloved and commonly avoided task throughout the industry and to request help from instrument vendors - that's what this document is about!

3. Details of the PCI Express Specification and Its Flavors

The base standard for PCI Express specifies TX and RX performance taking channel effects into account such that a system in mission-mode will function properly. The system could consist of a CPU- and a bridge-chip both located on a mother board (the "channel") or a bridge chip and e.g. a graphic controller located on an add-in card (here the channel consists of PC-board-traces and a connector).
In order to make compliance testing easier and reproducible the PCI-SIG came up with the CEM standard, a derivative of the base standard, and a set of tools, e.g. the compliance base board (CBB) and the compliance load board (CLB), as described in this document.

The base standard, two clock topologies and the RX-specifications

The base specification can directly be applied to RX and TX of an ASIC, which for testing purposes resides on a more or less ideal test fixture where influences of the testing environment have been reduced to a minimum and the remainders are de-embedded.
To realize such a test environment requires a lot of effort and is usually only done by semiconductor vendors.

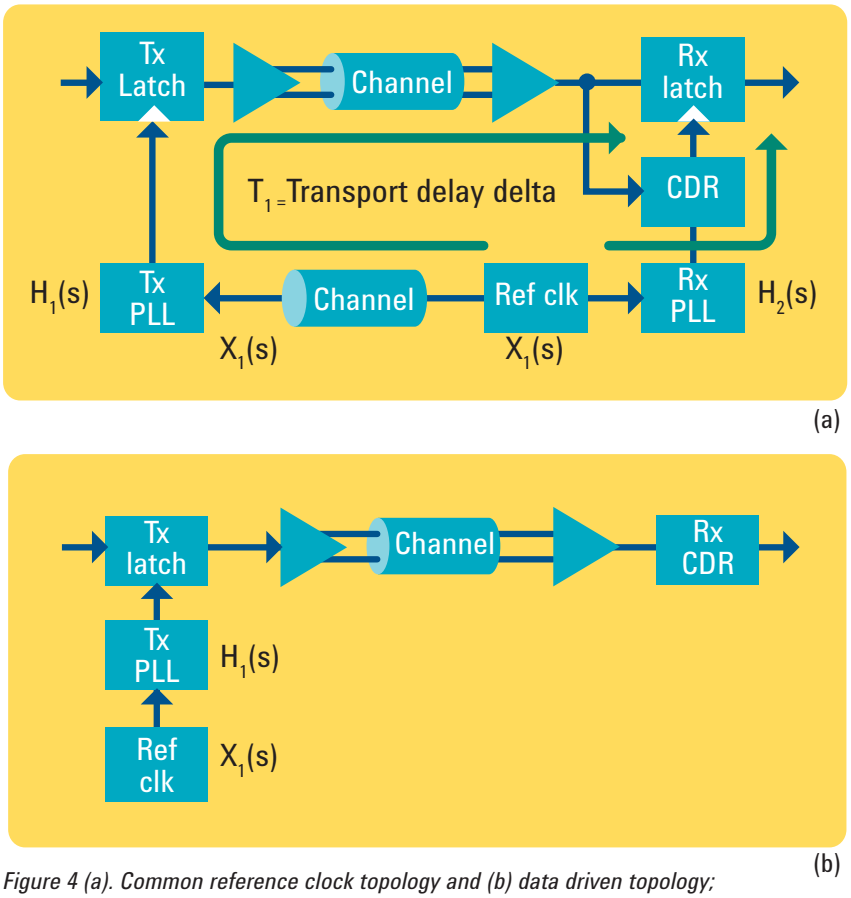


Figure 4 (a). Common reference clock topology and (b) data driven topology; The information in this graphic was obtained from [1], Figures 4-49 and 4-51

Two clock topologies

A PCI Express system can be realized with two different clocking modes or topologies, the common (reference) clock and the data driven topology as depicted in Figure 4 below.

The RX for the data driven topology is realized with a full PLL-CDR as it is known from communication systems, the sample timing is determined by the parameters of the PLL. The test is done with full SSC on data, same as in mission mode.

In the common clock topology, the RX samples the incoming data with respect to the multiplied reference clock; it uses a DLL-circuit for proper phase adjust with smaller adjust range than that of the PLL-CDR, which is not required, due to:

- The relatively small difference in the transport delay of the two paths from the reference oscillator through the TX and the channel and to the RX sampling-FF (see Figure 4a) and
- PLL or DLL circuits involved

Testing with different SSCs

The uncertainty in this path delay and the permitted range and the possible permutations of the TX-CMU-PLL and the RX-PLL (DLL) would lead to an impractical number of test scenarios.

Therefore a different approach has been chosen for the test:

- The reference clock is kept clean (without SSC) and
- The worst case phase difference resulting from the scenarios described above is added as "residual SSC" phase modulation (PM) on top of other jitter components of the RX data-input test signal.

The data driven architecture, however, uses full SSC frequency modulation (FM).

RJ with spectral distribution

These different scenarios and topologies also lead to a peculiarity of the PCIe RX test specification, i.e. the RJ with its spectral distribution.

Assuming that the major portion of the random jitter RJ has its origin in the phase noise of the reference oscillator, then those portions that fall within the bandwidth of the TX-CMU-PLL, will also be present on the TX-data. The RX, however, can follow these portions according to the bandwidth of its PLL or DLL (depending on topology). Stressing this capability is achieved by a RJ-spectrum with a higher LF-portion which is slightly different between the two topologies.

The complete jitter cocktail

The detailed specifications for the two topologies are listed in Table 1. Figure 5 shows how the complete jitter cocktail is composed for the common data clock topology. It not only shows the timing impairments (jitter cocktail) but the voltage impairments, the differential or common mode "noise" (DM/CM xtalk) as well.

Figure 5 also visualizes the test load, and where the test points for calibration of the test signal are located, and how and where the DUT-RX shall be connected. In the case of reference clock topology, the low frequency DJ equals the residual SSC described above.

For the data driven topology, this jitter component would be realized by the full SSC frequency modulation on the RX test signal, while the connection between clock and DUT-RX would not be required (see Figure 5).

Parameter	Description	Common ref clock	Data clocked
TRX_SSC	0 - 1.5 MHz DJ	75 ps_{pp} (residual SSC)	20 ns_{pp} (full SSC)
TRX_HF_DJ_DD	> 1.5 MHz DJ (including channel effects)	88 ps_{pp}	88 ps_{pp}
TRX_RF_RMS	0.01 – 1.5 MHz RJ	4.2 ps_{rms}	8.0 ps_{rms}
TRX_HF_RMS	> 1.5 MHz RJ	3.4 ps_{rms}	4.2 ps_{rms}

Table 1. RX specifications for common ref clock and data driven topology

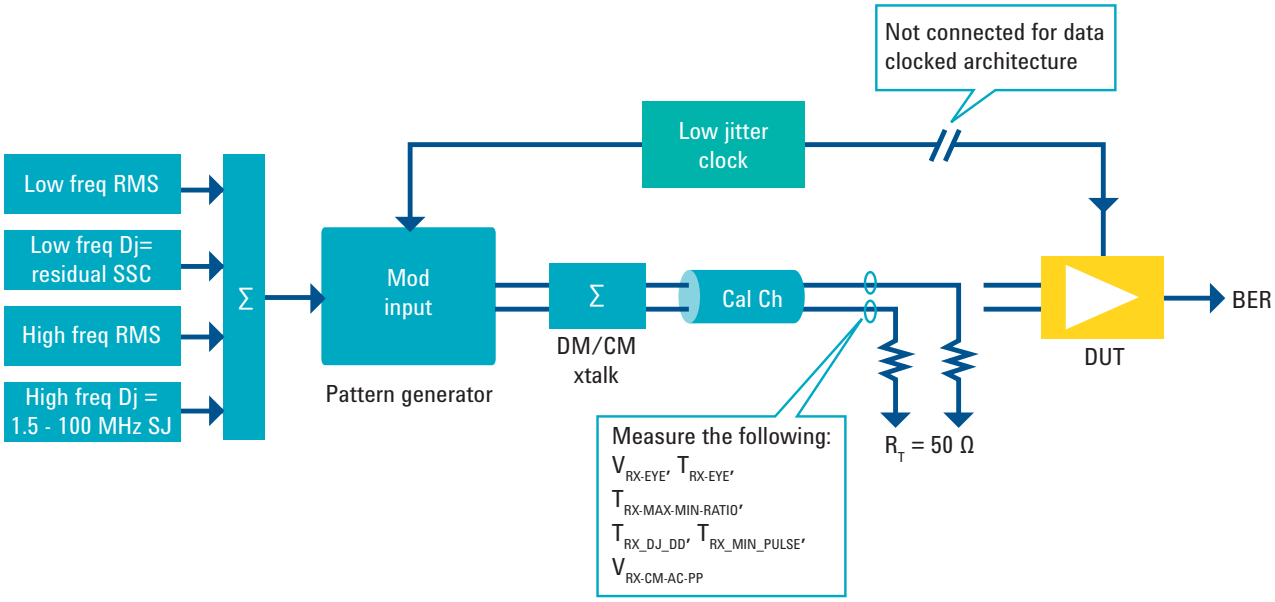


Figure 5. Complete jitter cocktail for common data clock topology; the information in this graphic was obtained from [1], Figures 4-35 and 4-36

How to realize the PCI Express jitter cocktail

With the Agilent Technologies J-BERT N4903A and 81150A pulse/function/arbitrary/noise generator

The test signal for an RX-test according to the PCI Express base spec can be realized as depicted in Figure 6 and listed in Table 2.

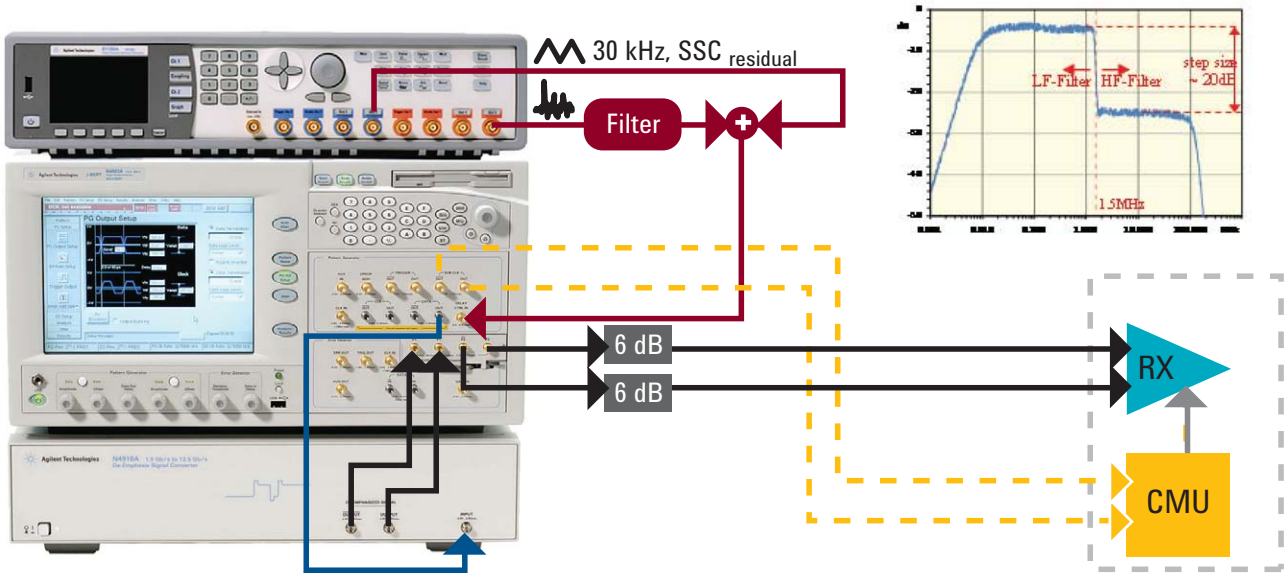


Figure 6. Test set-up for PCI Express base specification, common clock topology

Type of deterioration	Common clock topology	Data driven topology
RJ	With 81150, noise voltage with selectable crest factor, plus appropriate filter 15431A	
SSC	Residual, phase modulation with 81150, triangular voltage, 33 KHz	Full SSC frequency modulation, J-BERT with built-in SSC capability (Option 011)
DJ	Composed of J-BERT built-in PJ and ISI trace (Option J20)	
Noise voltages	Internally (Option J20)	

Table 2. Association of signal impairment with generating instrument feature

RJ:

The set up consists of the Agilent J-BERT N4903A and the 81150. The latter, together with a dedicated filter per topology, generates the modulation voltage for J-BERT realizing the desired RJ-spectrum.

SSC:

In the case of the common clock topology, the 2nd channel of the 81150 is used to produce the "residual SSC", while for the data driven architecture the internal SSC frequency modulation capability of J-BERT is utilized.

DJ (ISI+PJ):

The PCI Express base specification does not specify a certain amount of DDJ or ISI in terms of UI or ps or a certain PC-board trace by means of length or S_{21}. Instead the limited bandwidth of this "calibration channel" is specified in terms of amplitude ratio between the longest run of consecutive identical bits (CID, here: max = 5 bits due to 8 B/10 B coding) and a single bit as visualized in Figure 7 (a, b). Furthermore an impedance or return loss specification (-20 dB) is given as depicted in Figure 7 (c).

Transient behavior

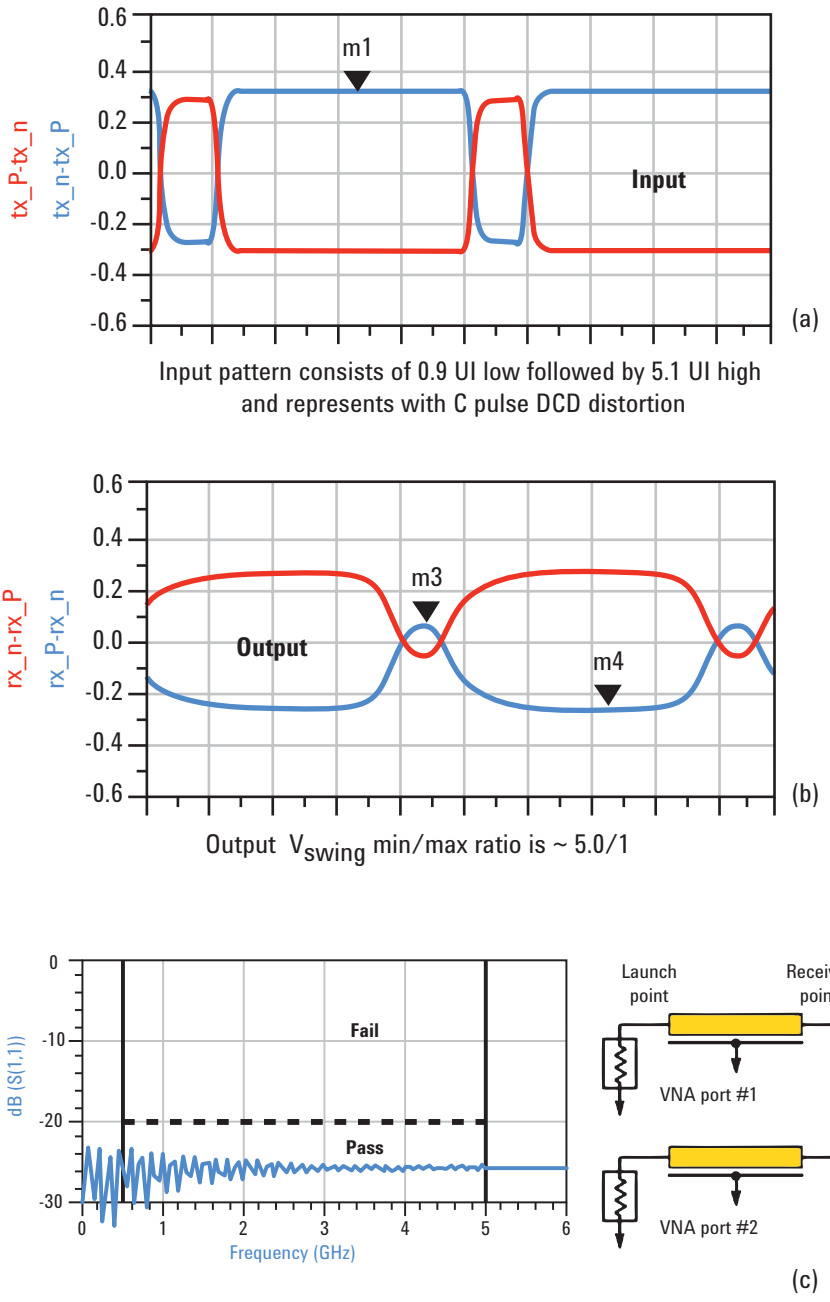


Figure 7 (a, b). ISI calibration channel specified through resulting shrinkage of a single bit vs. the longest CID (5 bits) and (c) impedance or return loss; the information in this graphic was obtained from reference 3, page 53 (a and b) and from reference 1, Figure 4-39 (c)

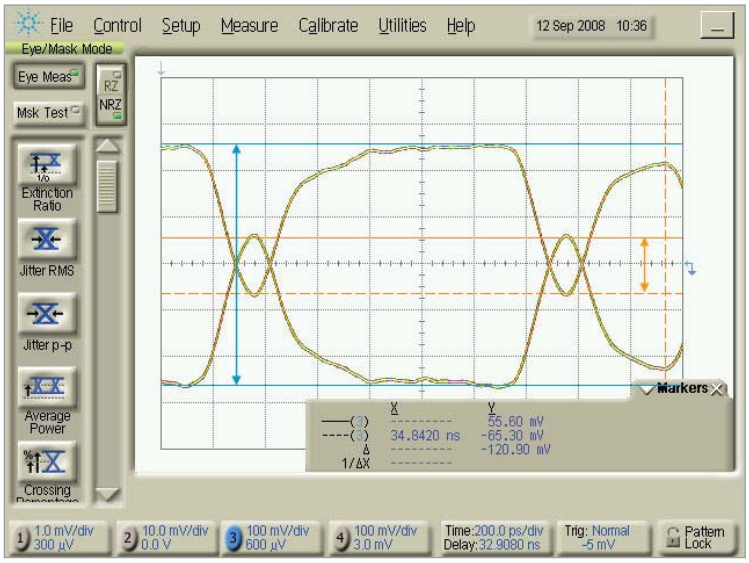
Trace #2 of J-BERT's Option 020 fulfills the desired properties in terms of pulse amplitude reduction and passes the return loss specification utilizing a 6 dB attenuator for "isolation" (see Figure 8).

According to the spec, two test cases need to be addressed:

1. With specified ISI-channel (comment: nearly no additional PJ required to achieve desired DJ of 88 ps (see Figure 8 (b))
2. Without any channel but PJ only

The calibration steps in detail

A detailed calibration procedure according to the PCI Express base spec is not provided here, as this document focuses on add-in cards. However, both specifications are similar, so that the procedure described below can be applied to the base specification correspondingly.



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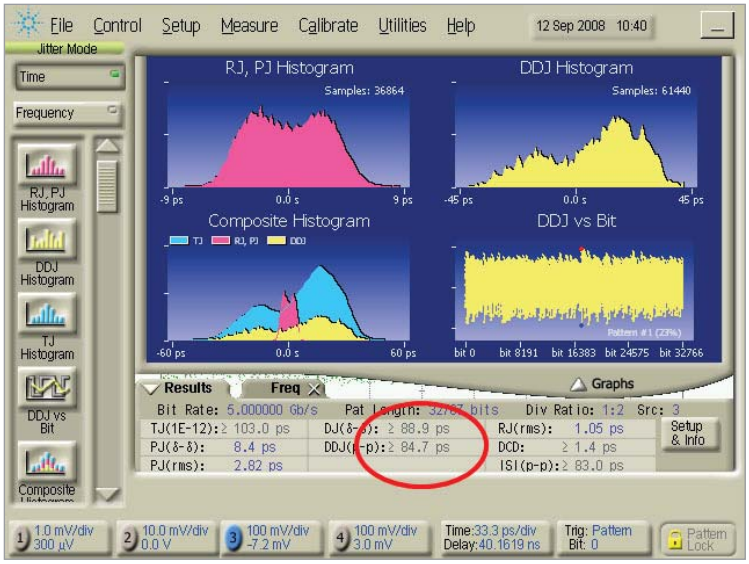

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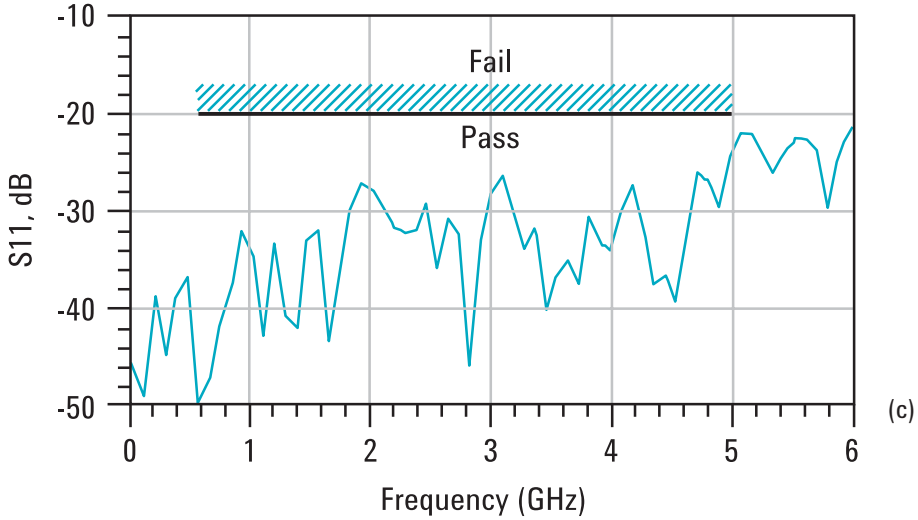


(c)

Figure 8 (a). Amplitudes of single 1 (0) are about 20% of those of longest CID (5 bits duration), (b) ISI measurement of PRBS 2^{15} - 1 through J-BERT Option J020 trace # 2, (c) return loss measurement of trace

The CEM spec and the compliance test for add-in cards

Why this additional specification?

The intension for this spec with respect to electrical-layer testing was, to

a) Unburden, e.g. add-in card manufacturers from compiling the base specification into applicable values for their cards and
b) Guarantee interoperability between motherboards and add-in cards of different manufacturers.

The compliance base board provides a close-to-real test environment with PC-board traces and a real connector, where at least a portion of the DJ, i.e. enough ISI is already generated by the test bed and the add-in card under test. Therefore no additional ISI needs to be generated, it is no more necessary to route the signal through J-BERT opt 020 traces as depicted in Figure 6.

However, the pulse performance is degraded by the CBB and the connector, such that transition bits do not reach the full amplitude compared to non-transition bits. In a real system, this effect would at least be partially compensated by the link-partner TX, providing a certain amount of de-emphasis. Consequently, this capability is now required by the test equipment. That is why the N4916A, de-emphasis signal converter, is necessary – allowing adjustment of transition and non-transition bits to the specified values.

The amount of DJ still to be generated is lower compared to the base specification. However a "dual-tone" test has been specified, consisting of a constant "tone" > 100 MHz and another tone in the range of 1.5 to 100 MHz, which needs to be swept.

RJ and residual SSC are unchanged vs. the base spec. The common mode "noise voltage injection" was removed as well from the stress cocktail. The details of the spec are summarized in Table 3.

Parameter	Base specification		CEM specification	
	Chip test		Add-in card	Motherboard
	Data driven	Common ref clock	Common ref clock	Common ref clock
V_{RXA}	100 mV	120 mV	300 mV	260 mV
V_{RXA_d}	No		300 mV	
ISI / calibration channel	5:1 pulse amplitude compression		No	
SSC 33 kHz reference clock	20 000 (FM) ps_{pp}	75, residual (PM) ps_{pp}	75, residual (PM) ps_{pp}	No
1.5 to 100 MHz RMS jitter	4.2 ps_{rms}	3.4 ps_{rms}	3.4 ps_{rms}	1.4 ps_{rms}
< 1.5 MHz RMS jitter	8.0 ps_{rms}	4.2 ps_{rms}	4.2 ps_{rms}	3.0 ps_{rms}
1.5-100 MHz DJ	88 ps_{pp} (pure SJ or SJ+ISI)		30 ps_{pp}	
>100MHz DJ	No		27 ps_{pp}	
Common mode cross talk	300 mV		No	

Table 3. Complete RX jitter tolerance and sensitivity test specifications for all four cases; the information in this table was obtained from reference 2, Figure 4-13

4. Compliance Test for Add-In Cards

According to the CEM–specification

Test specifications are listed in Table 3. The complete procedure for the compliance test is provided below. It consists of 4 major steps, i.e. the preparation of the compliance-base-board, the electrical connection, the calibration of the test signal and the test itself.

Preparing the test

The compliance base board

A few peculiarities of this board are listed and resulting actions necessary for a meaningful RX-test described as follows.

- Remove all resistors for Lane 0 on the RX side, R1, R2, R12 and R13 (R1 and R2 connect RX lane 0 with a toggle circuit used to switch between data rates in Compliance mode for TX-test – this circuit heavily interferes with the injected data for RX test – however, after removing R1 and R2 the CCB can no more be used for 5 GB/s TX tests)
- Remove resistors R20 and R19 of Lane 0 on the TX side
- Important: all lanes require a 50 Ω termination, either through test equipment, through board resistors or through terminations at the connectors – alternatively, unused lanes can be "taped" within the DUT PCIe connector or a multi- to single-lane adapter board can be used.
- Make sure the resistors R78 and R87 are loaded otherwise external reference clock cannot be injected. Remove R4, R5, R84 and R86.
- Connect a standard computer supply to the CBB and if required to the DUT add-in card as well; it can be advantageous to use a lab power supply instead to avoid uncontrolled power supply cross-talk distortions.

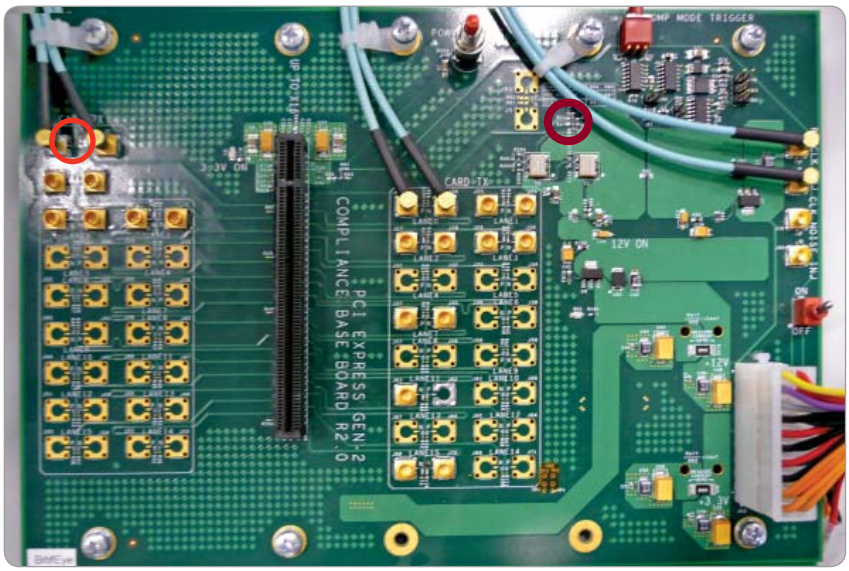


Figure 9. Compliance base board (CCB) – circles mark the mentioned modifications

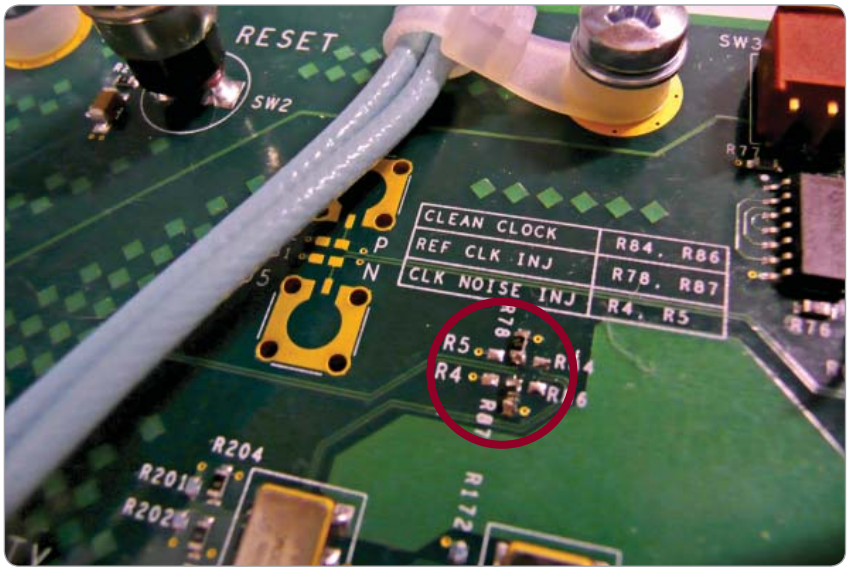


Figure 10. Detail of compliance base board

The test set-up (cabling)

Figure 11 visualizes the necessary connections between J-BERT/81150/N4916A and the compliance base board (CBB). A list of required instruments, options and accessories can be found in the appendix at the end of this document.

Jitter generation by instrument

This list identifies which instrument generates which jitter component.

- 88150 Ch2: RMS Jitter RJ < 1.5 MHz + 1.5-100 MHz (RJ_{LF} + RJ_{HF})
- J-BERT: 33 kHz ref clock residual ($SSC_{residual}$)
- J-BERT: DJ > 100 MHz (HF sinusoidal jitter (SJ))
- 81150 Ch1: DJ 1.5 – 100 MHz (swept sinusoidal jitter (SJ_{sweep}))

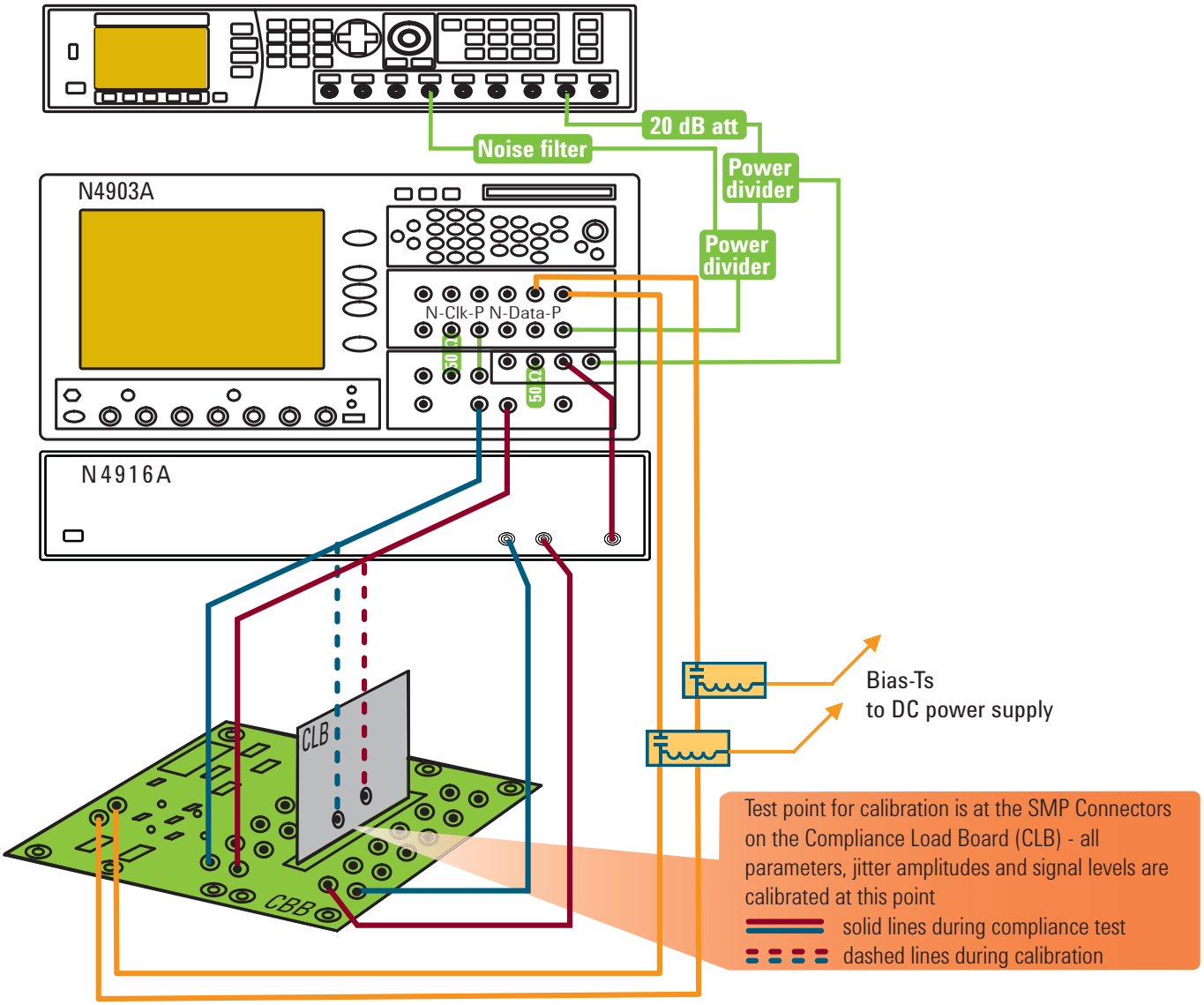


Figure 11. Schematic connection diagram between J-BERT and CBB

The calibration steps in detail

Jitter components, which are directly generated with J-BERT are already factory calibrated. It would not be necessary to repeat this calibration, but it is listed here for completeness and for increased confidence.

Furthermore, output levels of the 81150 are factory calibrated, J-BERT's external jitter input has a typical conversion gain of 400 ps/V. Combining these two characteristics delivers good starting points for amplitude settings on external sources for those jitter components not generated by J-BERT internally.

All manual calibrations described step-by-step, are automated when using the "test automation software," N5990A Option 101.

Default settings

The calibration of each component is described in detail below; the commonalities of all steps are listed up-front:

- Connect the J-BERT with the 81150A, the N4916A, the accessories, and the CBB/CLB, as shown in Figure 11.
- Set the power supply voltage for the Bias – Ts to approximately 300 mV

Instrument default settings

- J-BERT preparations: load the compliance profile (see appendix) to a suitable location onto the J-BERT C-disk.
- J-BERT settings
  - Data rate 5 Gbit/s, set up the depicted sequence with the appropriate test patterns and start the sequence manually (Figure 12)
  - Set the data output amplitude to V_{data} = 150 mV and the clock output to 250 mV
  - Enable jitter, external jitter, PJ and sinusoidal interference (SI):
  - for PJ: triangular waveform, frequency 33 kHz and 0UI amplitude
  - for SI: mode = normal, frequency = 240 MHz, amplitude = 0 mV
  - Set error detector (ED) to differential mode and external clocking
  - Under timing measurement, properties, set resolution to 0.001 UI

- 81150A settings
  - Ch1 function = sine, sweep, start frq = 1.5 MHz, stop frq 100 MHz, amplitude amp = 50 mV, offset = 0 V
  - Ch2 function = noise, cf = 7.0, amplitude = 50 mV_{pp}, offset = 0 V.

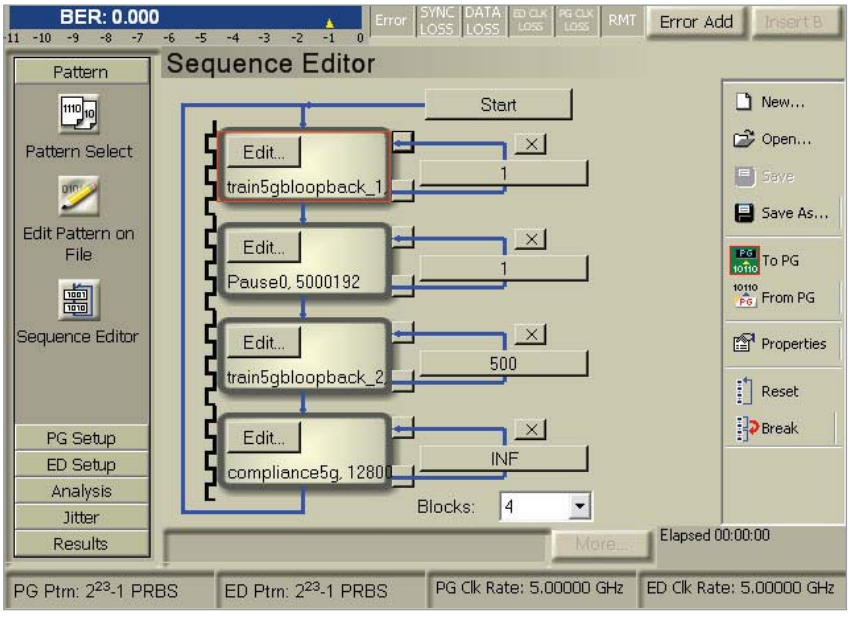


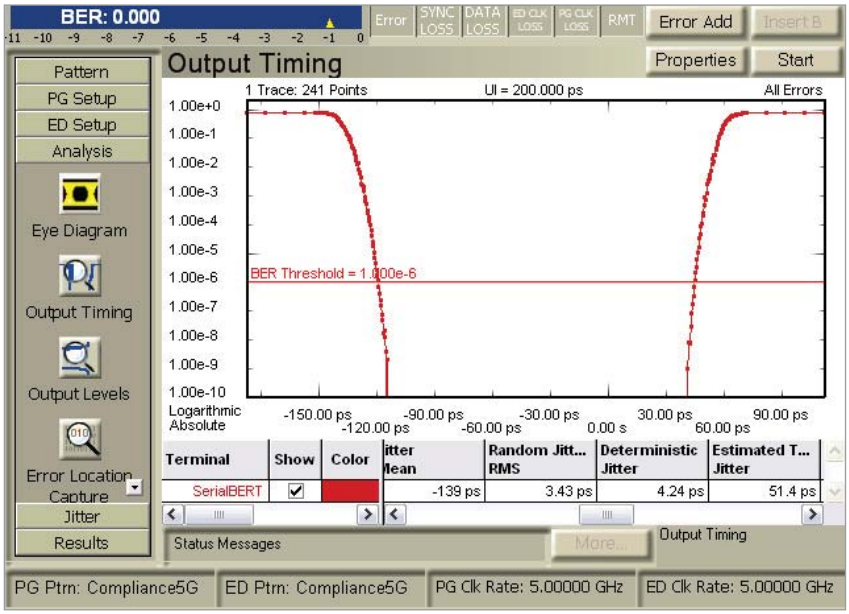
Figure 12. J-BERT test sequence and patterns for calibration and test

RJ

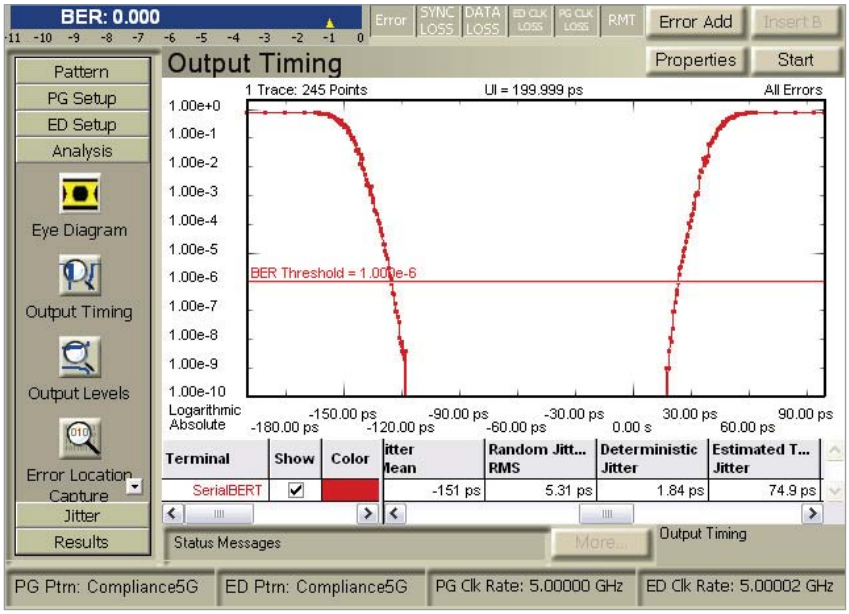
- Start with the instruments' default settings
- The white noise voltage generated by the 81150 is filtered such that the appropriate spectrum, i.e. the ratio of LF to HF noise is automatically achieved (please see Figure 6, upper right). Therefore it is only necessary to do one adjust for the proper amount of the combined jitter.
- $(RJ_{LF} + RJ_{HF}) = \sqrt{(4.2\ ps^2 + 3.4\ ps^2)} = 5.4\ ps_{rms} = 75.5\ ps_{pp}$ (for a crest factor of 7, equiv. to BER 10^{-12}).

81150A settings

- Ch2 amplitude = 3.5 V_{pp}, offset = 0 V.
- J-BERT: Press <Auto align >
- Choose <Analysis> and select <Output timing measurement> properties: 10^{10} bits, BER-threshold = 10^{-6}, BER-threshold for estimated jitter = 10^{-12}
- Start measurement and note estimated total TJ value
- If $TJ_{pp} \neq 75.5\ p \pm 2.5$ ps adjust 811150 Ch2 amp and repeat output timing measurement
- Note Ch2 amplitude



(a)



(b)

Figure 13 (a). RJ measurements with J-BERT timing measurement: $RJ_{HF} = 3.4\ ps_{rms}$ with ED set to CDR (F_c approximately 2 MHz) and, (b) $RJ_{HF}+RJ_{LF} = 5.4\ ps_{rms}$ with ED set to ext clock mode

SSC residual calibration

- Start with the instruments' default settings
- J-BERT: Set PJ amplitude to approximately 75 ps (0.375 UI)
- Press <Auto align> on J-BERT
- Choose <Analysis> and select <Output timing measurement> properties: 10^{10} bits, BER-threshold = 10^{-6}, BER-threshold for estimated jitter = 10^{-12} Start measurement and note DJ value
- If $DJ_{pp} \neq 75.0$ ps ± 2.5 ps adjust PJ amplitude and repeat output timing measurement
- Note PJ amp

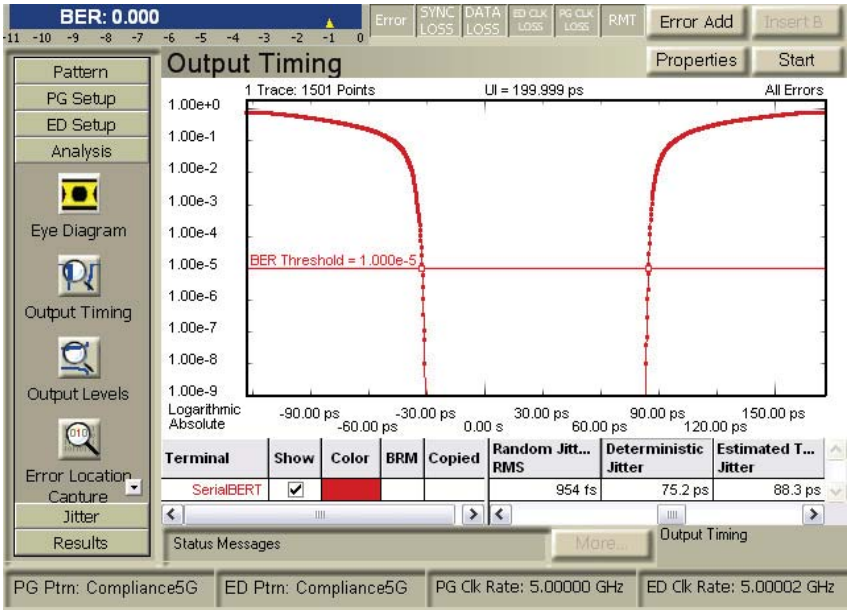


Figure 14. Residual SSC measured with output timing measurement showing DJ = 75.2 ps_{pp}

SJ calibration (1.5 – 100 MHz)

- Start with the instruments' default settings
- 81150A Settings: Ch2 amp = 2.7 V
- Press <Auto align> on J-BERT
- Choose <Analysis> and select <Output timing measurement> properties: 10^9 bits, BER-threshold = 10^{-5}, BER-threshold for estimated jitter = 10^{-12}
- Start measurement and note DJ value
- If $DJ_{pp} \neq 30.0$ ps ±2.0 ps adjust 81150A Ch2 amplitude and repeat output timing measurement
- Note Ch1 amp

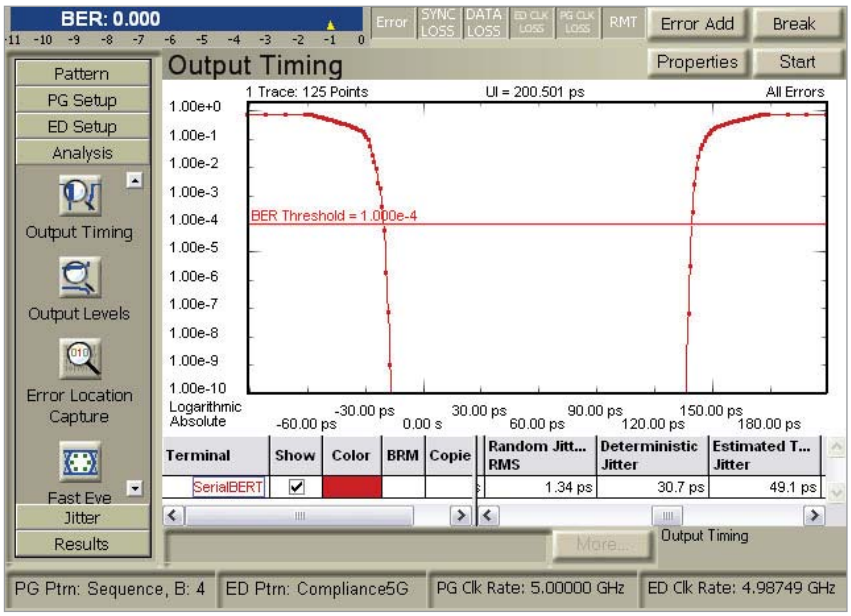


Figure 15. Swept sinusoidal jitter measured with output timing measurement showing DJ = 30.7 ps_{pp}

HF SJ calibration

- Start with the instruments' default settings
- J-BERT: Set sinusoidal interference (SI) to 210 mV
- Press <Auto align> on J-BERT
- Choose Analysis and select <Output timing measurement> Properties: 10^9 bits, BER-threshold = 10^{-5}, BER-threshold for estimated jitter = 10^{-12}
  - Start measurement and note DJ value
  - If $DJ_{pp} \neq 27.0$ ps ± 2.0 ps adjust SI and repeat output timing measurement
  - Note SI voltage

Differential voltage calibration

The differential voltage and the de-emphasis levels can be calibrated using any suitable oscilloscope or, as shown here, using J-BERT's measurement capabilities, in this case the eye-diagram measurement. However, the specified jitter cocktail completely closes the eye:

$RJ + SSC_{res} + SJ_{HF} + SJ_{swept}$ = 75.5 ps + 75 ps + 27 ps + 30 ps = 207.5 ps = 1.04 UI.

Therefore, the measurement is not performed with respect to a stable clock but with the ED's built-in CR.

- Start with the instruments' default settings
- Choose <Analysis> and select <Eye diagram>
- Adjust de-emphasis level such that eye diagram on the screen of the BERT only shows one high and one low level (see Figure 17); restart measurement after each change of de-emphasis-level)
- Set 81150 Ch1 and Ch2 amplitudes to noted values
- Set J-BERT PJ and SI to noted values
- On J-BERT, set ED clocking to CDR and select loop bandwidth 1.5 MHz, transition density 50% and peaking 0 dB.
- If eye-height ≠ 300 mV ± 5.0 mV adjust data output amplitude and repeat eye diagram measurement
- Note data output amplitude voltage

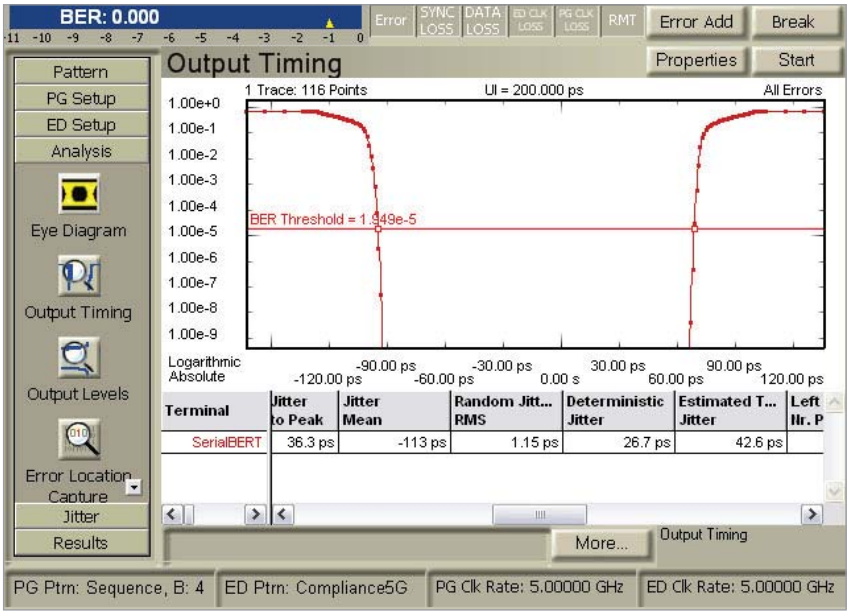


Figure 16. High frequency sinusoidal jitter measured with output timing measurement showing DJ= 26.7 ps_{pp}

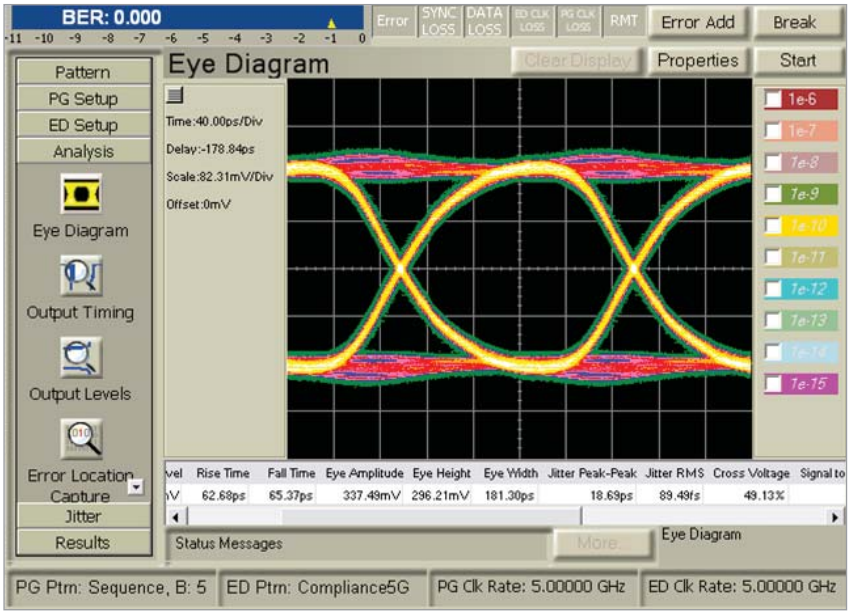


Figure 17. Eye diagram of the calibrated test signal measured with PCIe compliant CDR showing a differential eye height of 297 mV

The compliance test itself

- Insert a DUT add-in card into the PCI connector, either with a “lane 0–only” interposer board or cover all unused lanes with tape
- Connect all instruments as shown in Figure 11
- Start with the instruments’ default settings
- Set data output amplitude to 250 mV
- Stop J-BERT by pressing <Reset> button in sequence window (Figure 12)
- Turn on the CBB power supply
- Start J-BERT by pressing <Start> button in sequence window (Figure 12)
- Press <Auto align> on J-BERT
- Note that BER = 0 now
- Reduce data output amplitude and set jitter settings to the values determined during the calibration procedure above
- Make a BER measurement with a BER target of 10^{-12} and a confidence level (CL) of 95%. Compliance is achieved when no errors occur for approximately $3*10^{12}$ bits or 10 minutes (for a data rate of 5 Gb/s)

J-BERT’s accumulated results screen nicely supports this compliance measurement, as it logs BER for a predefined amount of bits or measurement time; as visualized in Figure 18, the DUT passed this compliance test. However, if it failed, you might want to have more information allowing some root cause analysis. This task is described in the next chapter.

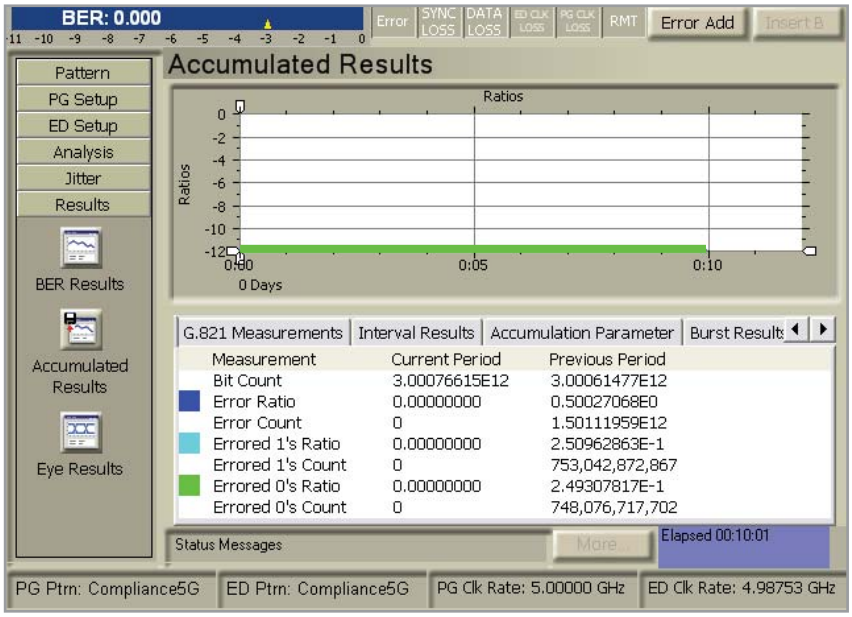


Figure 18. No errors occurred over a period of 10 minutes, as indicated by the green line; the DUT passed compliance criterion of BER < 10^{12} with CL = 95%

5. Additional Tests Beyond Pure RX-Compliance

Provided the compliance test failed and you want to know e.g. which jitter frequency made the RX fail or how much jitter at any frequency it tolerates you may want to perform the two measurements listed below.

Swept SJ RX compliance test

First attempt to gather more detailed information is performing a "tolerance compliance" measurement, to find out which jitter frequencies caused the failure. Therefore it is necessary to swap the instruments which generate the SJ_{swept} and the SSC_{res}, i.e. 81150 and J-BERT.

- Start with the instruments' default settings
- J-BERT, set PJ to sinusoidal waveform
- 81150, Ch1, turn sweep off, set to triangle waveform, freq 33 kHz, symmetry = 50%, and amplitude to 2.7 V (please exchange the 20 dB attenuator with a 10 dB attenuation)
- Calibrate the amplitude of the residual SSC similar to the procedure given in the previous chapter.

Now you can perform a compliance measurement with constant jitter amplitude of 30 ps (0.15 UI) between 1.5 MHz and 100 MHz, choosing <Compliance sweep> under the J-BERT <Jitter> tab selecting the related profile from the file you have stored on the C-disk before the beginning of the tests (see appendix).

A characterization down to BER = 10^{-12} for every jitter frequency is probably impractical in terms of total measurement time (each frequency would have to be measured for 10 minutes provided no errors occur!). So the "target BER" on the properties page should be set to 10^{-9} or 10^{-10}.

The measurement is performed analogous to the description given in the previous chapter. The result of this measurement is shown in Figure 19, revealing problems in the 20 – 80 MHz jitter frequency range (red crosses instead of green circles).

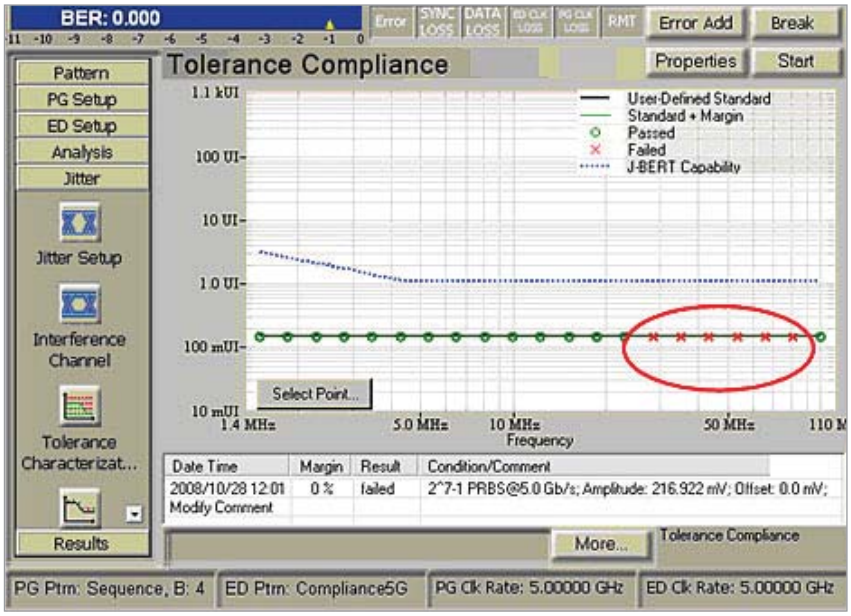


Figure 19. Compliance measurement on add-in card receiver sweeping from 1.5 MHz to 100 MHz

Full characterization measurement of RX

Even more insight into the RX's jitter tolerance can be gained using J-BERT's jitter tolerance characterization measurement, which automatically determines the maximum tolerable amount of SJ per preprogrammed frequency, as depicted in Figure 20. The six red crosses of Figure 19 translate to the measurement points circled in Figure 20.

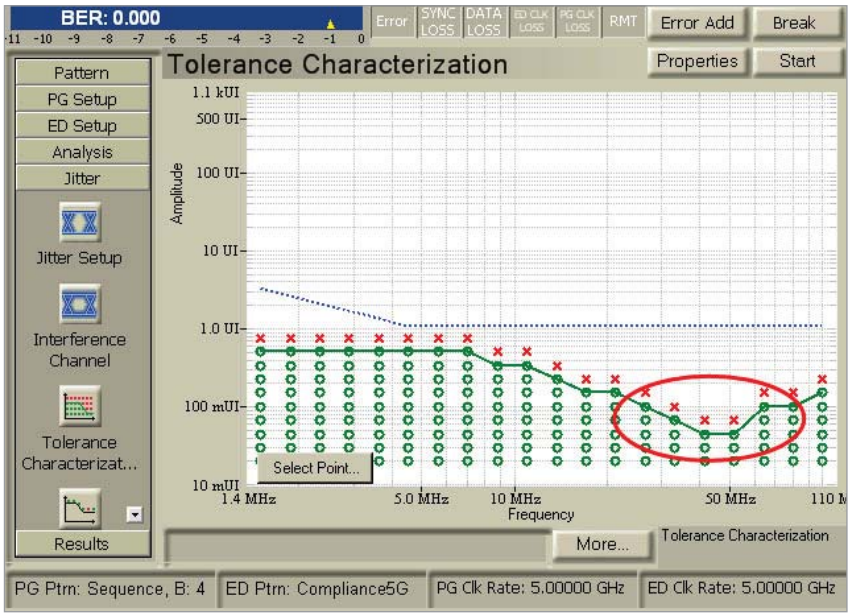


Figure 20. Full RX-jitter tolerance characterization

6. Summary and conclusions

The different versions of the PCI Express standard and their application to the different DUT types have been discussed. A test according to the base standard applicable for ASICs has been described. A step by step procedure for the compliance test of add-in cards has also been provided; it consisted of the preparation of the compliance-base-board, the connection diagram, the calibration of the test signal and the test itself. An example for a RX characterization measurement has also been provided.

The conclusion is that with a small set of accessories (see appendix) and supporting instruments, the Agilent J-BERT N4903A masters this test completely.

7. Appendix

Shopping list

- (1) Agilent N4903A, J-BERT 7 Gb/s (C07) Option J10, J11, J20, SW rev 4.9.2 and higher
- (1) Agilent N4916A de-emphasis signal converter
- (1) Agilent 81150A, Option 020
- (1) Agilent 15431A, PCI Express generation 2 filter for 81150A
- (2) Agilent 11636B, power divider, DC to 26.5 GHz
- (1) BNC ≥ SMA(f)
- (2) Agilent N4912A, termination 2.4 mm (m), 50 Ω
- (2) Bias-T
- (1) Agilent E3150-61602, BNC cable
- (1) Agilent 15442A 4x SMA (m) to SMA (m)
- (1) Agilent 8493(A) C-020, attenuator 3.5 mm (m) to 3.5 mm (f), 20 dB, dc to (12.4) 26.5 GHz
- (1) Agilent 8493(A) C-010, attenuator 3.5 mm (m) to 3.5 mm (f), 10 dB, dc to (12.4) 26.5 GHz
- (1) Agilent N4915A-003, 2.4 mm to SMA semi-rigid cable for N490x clock out to clock in
- (5) Agilent N4911A-002, adapters 3.5 mm (f) to 2.4 mm (m), dc to 26.5 GHz
- (2) Agilent SMA 3.5 mm (m) to 3.5 mm (m) matched cable pair, ± 5 ps , 1 m
- (6) Agilent E4809-61603, SMP-SMA cables
- (1) PCI SIG compliance base board CBB, rev 2.0
- (1) PC power-supply
- (1) DC-power supply (for bias voltage)
- (1) DUT with 1-lane adapter card
- Optional: (1) N5990A-101

Related literature

[1] *PCI Express Base Specification* Revision 2.0 December 20, 2006

[2] *PCI Express Card Electromechanical Specification* Revision 2.0 April 11, 2007

[3] Presentation from PCI-SIG entitled, *"PCI Express 2.0 Electrical specification"* Jeff Morris (Intel) and Gerry Talbot (AMD) Co-chairs EWG

Test Automation Software Platform N5990A Data Sheet
Pub number: 5989-5483EN

Agilent J-BERT N4903A High-Performance Serial BERT Data Sheet
Pub number: 5989-2899EN

Filter Set for 81150A -- Generates Random Jitter Profile for Testing PCI Express Data Sheet
Pub number: 5989-9826EN

Agilent 81150A Pulse Function Arbitrary Noise Generator Data Sheet
Pub number: 5989-6433EN

Upgrade to PCI Express 2.0 Receiver Test Brochure
Pub number: 5989-9937EN

Agilent N4903A High-Performance Serial BERT Brochure
Pub number: 5989-3882EN

N81150A Getting Started Guide

N81150-91010 Quick Start Guide

Characterizing Clock Jitter through Phase Noise Measurements Speeds Up Your Design, White Paper
Pub number: 5989-9849EN

Compliance patterns

Suitable compliance patterns are integrated in J-BERT SW rev 4.9.2 and higher. The sweep profile according to Figure 18 can be downloaded from www.agilent.com/find/PCIe_receiver_test

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Product specifications and descriptions in this document subject to change without notice.

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www.agilent.com/find/J-BERT
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