

# Configuring Signal and Load Switching Using Agilent TestExec SL

Application Note

### **Overview**

Switching is essential and critical to functional testing. As the design of unit under test (UUT) gets more complex nowadays, the test pin counts and resulting number of switching channels required have increased significantly. Therefore, the need for features which can help manage the switching in a test system has become even more crucial for test sequencer tools, such as the Agilent TestExec SL software.

This application note describes how simple it is for users of the TestExec SL software to configure and set up the switching using its Switch Manager feature. A few examples will be discussed in details, for example, performing direct current (DC) measurements via signal switching and connecting simulated loads via load switching.



### Switching Topology Overview

Switching topology is the combination of physical and logical descriptions of switching configuration and interconnections between resources and the UUT. It defines the switchable paths for the three layers of topology in a complete test system – *System*, *Fixture* and *UUT* (see Figure 1).

Prior to defining the topology files, users have to plan their hardware resources accordingly. A fixture worksheet is usually created to show the resource allocation for the test system (see Table 1). From the worksheet, users will identify the connections from each DUT pin to respective switching channels, either pin matrix card, load card, or both, and then convert them into topology files using the topology editor.



Figure 1. System block diagram showing system, fixture and UUT layers

Table 1. Fixture worksheet allocating DUT pins to pin matrix card rows and load channels

DUT nin #	Signal name	Aliases	Pin matrix	Load card
23	Ser1 In	Ser1 In	15	
20	Sor? In	Sor? In	14	
24			14	
25	Ser2 Out	Ser2_Out	13	-
26	Ser1 Out	Ser1_Out	12	-
35	+12V	+12V_Supply	2	2
37	DUT Ground	DUT_Gnd	1	1
(SLU)	Current Sense +	Current Sense +	3	-
(SLU)	Current Sense –	Current Sense –	4	-

### System Layers

System layers contain all switching node definitions within a test system up to the interface. It includes the modules (e.g. DMM, power supply, load card, pin matrix card, etc.) and wires (for example, 'dmm:Hi' is connected to 'matrix1-Instr1') which defines the wiring connections between modules in the system. Aliases are sometimes added to define alternate names for switching nodes but usually the default names themselves are already selfexplanatory.

#### Example 1.

Defining	the system layer using Topology Editor
Step 1	Click File > New
Step 2	Select Topology Layer, and then click OK.
Step 3	Select System Layer, and then click OK.
Step 4	Click <b>Modules</b> , then type 'dmm' in Name space. Description is optional but recommended.
Step 5	Select DLL Module
Step 6	Click $\mbox{\bf Browse}$ and browse the 'hwhdmm.dll' from the correct directory.
Step 7	Configure other Parameter Block properties according to the actual setting.
Step 8	Click Update
Step 9	Repeat steps 4 - 8 for other pins. Change the DLL accordingly in step 5.

1. The hardware handler for DMM - 'hwhdmm.dll' - can be found in default directory 'C:\Program Files\Agilent\TS-5400 System Software\Bin' under TS-5400 Application Software package. Other hardware handlers for supported instruments also saved in this folder.

Aliases Wires Modules Cloadunit0 Cloadunit0 Cloadcard1 Cloadcard1 dmm:Hi dmm:Lu	Name: dmm	dmm		
	Description: AG34411A 22	Multimeter at GPIB address	Update Help	
	O DLL Module O CO     Prefic	IM Automation Module O.N	ET Module	
Amm HiConce	ACCOUNTS AND			
ndmm:HiSense dmm:LoSense	Library: hwhdmm.dll	C	Browse	
🗈 dmm:HiSense 🖻 dmm:LoSense	Libraty: hwhdmm.dll Parameter Block:		Browse	
🖻 dmm:HiSense 🖻 dmm:LoSense	Library: hwhdmm.dll Parameter Block: Name	Value	Browse	
ि dmm:HiSense हि dmm:LoSense	Libray: hwhdmm.dll Parameter Block: Name     single: [Device ID]	Value ag34411a	Browse	
B dmm:HiSense B dmm:LoSense	Librag: hwhdmm.dll Parameter Block: Name is: Bell/Device ID is: Bell Instrument Desc	Value ag34411a siptor GPIB0-22-INSTR	Browse	
₿dmm:HiSense ₿dmm:LoSense	Libray: hwindmin di Parameter Block: Name # Bel: Device ID # Bel: Instrument Desc # IEE: Cage or Board #	Value ag34411a riptor GPI80-22:INSTR t 0	Browse	
₿dmm:HiSense ₪dmm:LoSense	Libray: hwhdana.dl Parameter Block: Name # Infel Device ID # Infel Device ID # Infel Device ID # INFEL Cage or Board # # INFEL Cage or Board #	Value ag34411a siptor GPIB0:22:INSTR 0 11	Browse	

Figure 2. Topology Editor – system layer

### System Layers

Alternatively, you can define the system save layer using System Configuration Editor (SCE)<sup>2</sup>. This application software is created to simplify the process of creating the system layer topology file. It has a predefined list of supported instruments. In order to create the topology file, you can choose the desired instruments from the list and add them to the system topology file. Otherwise, if you have the instruments connected to the controller, then you can also select Detected on system, whereupon it will show a list of detected instruments.

#### Example 2.

Defining	the system layer using System Configuration Editor (SCE)
Step 1	Launch SCE software from the icon (usually on the desktop).
Step 2	Select Detected on system (optional).
Step 3	Select the instrument to be added, then click Add.
Step 4	Configure the properties in the Configure Module pop-up dialog box and then click <b>OK</b> .
Step 5	Repeat steps 3 and 4 until all desired instruments are added to the topology file.
Step 6	Click <b>Save</b> and save the system topology file at desired directory path.



Figure 3. System Configuration Editor (SCE)

 SCE is one of the software grouped under the TS-5400 Application Software package. Beginning with release 5.1.1, the SCE was expanded to operate on all topology layers (system.ust, fixture.ust and uut.ust). Additionally, the import feature was added in release 5.1.1 to import wires and aliases from a '.csv' file while the export feature was added in release 6.0.0 to export the wires and aliases to a '.csv' file.

### **Fixture Layer**

The fixture itself is a module. Therefore, most of the time, the fixture layer only contains the wires that defines the wiring connections between system layer and UUT layer. *Wires* are used to define any permanent connections between switching nodes. For example, we can set 'Ser1\_In' node in the fixture later is connected to 'Row 15' of the pin matrix card number 1 in the system layer (see Figure 4).

#### Example 3.

Defining	the fixture layer using Topology Editor
Step 1	Click File > New
Step 2	Select Topology Layer, and then click OK
Step 3	Select Fixture Layer, and then click OK
Step 4	Select <b>Wires</b> , then type 'Ser1_In' in Name space. Description and Keywords are optional but recommended.
Step 5	Select Reference Layer = system, and Reference Node = matrix1:Row15
Step 6	Click Update
Step 7	Repeat steps 4 - 6 for other pins. Change the reference node accordingly in step 5.

Note: Make sure the TestExec SL is linked to the correct system.ust file before creating the new fixture.ust file. Otherwise, the reference layer will not show the right list of nodes.

Wires	Name:	Ser1_	In	Update
Current Sense + Ser2_In Ser2_Out	Description:		0.0	Help
Ser1_Out	Keywords:			1
Current Sense -	Connections			10
	Bef Laver	1	Ref Node	
Modules	system		matrix1.Row15	New Conn
				Delete Con
				Move Up
				Move Dove
	Reference La	yer.	Reference Node:	
	system	*	matrix1:Row15	Update Con
	Filter:		ABus1	1
			40	

Figure 4. Topology Editor – fixture layer

### **UUT Layer**

UUT itself is also a module but it usually does not contain wiring connections. Instead, we define *aliases* to symbolize the UUT pins in a UUT layer. *Aliases* are defined to give the pin an alternate logical name which is more meaningful. For instance, we can set +12 V aliased as pin 35 of the UUT (see Figure 5). Every pin must be defined in the topology file so that TestExec SL is able to recognize the switching nodes.

#### Example 4.

Defining	the UUT Layer using Topology Editor
Step 1	Click File > New
Step 2	Select Topology Layer, and then click OK.
Step 3	Select <b>UUT Layer</b> , and then click <b>OK</b> .
Step 4	Click <b>Aliases</b> , then type '+12V' in Name space. Description and Keywords are optional but recommended.
Step 5	Select Reference Layer = fixture, and Reference Node = +12V_Supply
Step 6	Click Update
Step 7	Repeat steps 4 - 6 for other pins. Change the reference node accordingly in step 5.

Note: Make sure the TestExec SL is linked to the correct system.ust file before creating the new fixture.ust file. Otherwise, the reference layer will not show the right list of nodes.



Figure 5. Topology Editor – UUT layer

## **UUT Layer**

After completing the topology files, you have to specify their directory paths in TestExec SL. This is necessary in order to allow Switching Path Editor to recognize the hardware configuration and control the switching paths during a test.

### Example 5.

Specifying the switching topology layers for a testplan		
Step 1	Click Options > Testplan Options	
Step 2	Select Topology Files	
Step 3	Specify the directory path of the files for system, fixture and uut layers.	
Step 4	Click <b>OK</b> and back to the testplan.	

	Tennies Celluis		
estplan Sequence: Main	Variants	Testplan Options	
		Execution Reporting Profiler Topology Files Sequences 1	Search Paths Throughput Multiplier
		System life name:	
		Instern MysSLUDerro uit	Browse
		C-Documents and Settings/sweegoh1/Desktop/Min/SLUDemo/system_ministu	idemo.ust
		Fidure file name:	-
		C-VDocuments and Settings/sweegoh1/vDesktop/MiniSLUDemo/Vixture_ministur	demo.ust
		uut. MinSLUDemo.ust	Browse
		C:\Documents and Settings/tweegoh1Vbrisk.tep\MinSLUDenroVaxLinenish.den Preferences C:\Miy1xSL:Files\1reit System1\Preferences.upt	no. ust

Figure 6. Specifying the switching topology layers for a testplan

### Signal Switching via Pin Matrix Card

A pin matrix card is a collection of high speed reed relays in a matrix form used to link the instrumentations to all measurement nodes at a UUT. Typically, you can divide a matrix card into instrument matrix and measurement matrix sections. Both the matrixes are linked via four *analog buses* (Abus1-4), thus instruments that are attached to the matrix card can flexibly access any measurement nodes at a UUT.

With TestExec SL Switch Manager feature, the switching configuration has been made really easy by simply linking the logical names in a switching path. Take a continuity test for instance; in order to measure the resistance across two points at a UUT, we need to probe the digital multimeter (DMM) high and low pins to the two points in parallel and then make a measurement (see Example 6). In TestExec SL, subsequent to inserting a switching action in a test, Switching Path Editor will guide you through to specify the switching path by listing all the adjacent nodes.

#### Example 6.

Measu	ing the resistance
Step 1	Click <b>Insert &gt; Testgroup</b> , then type 'Continuity Test' in the Testgroup Name space
Step 2	Click <b>Insert &gt; Test</b> , then type 'Check Serial1 Short' in the Test Name space
Step 3	Click Insert Switching, double-click Add Path in the Parameter space, then add the following switching paths. Path1 - dmm:Hi   Abus1   Ser1_In Path2 - dmm:Lo   Abus2   Ser1_Out Path3 - dmm:HiSense   Abus3   Ser1_In Path4 - dmm:LoSense   Abus4   Ser1_Out This switching action closes the relay paths from DMM to UUT via Abus1-4 of pin matrix card. Four connections are required for four-wire resistance measurement.
Step 4	Insert 'PinProtBypass' <sup>3</sup> action. This action will bypass the 200 Ohm protection resistor on the Agilent E8792A pin matrix card.
Step 5	Insert 'dmmMeas4WResEx' <sup>3</sup> action, set ExpectedReading = 1 Ohms. This action will trigger the Agilent 34411A DMM to make a four-wire resistance measurement.
Step 6	Click <b>Limits</b> , set 'Kind of Limits' to 'Min/Max', set min = 0 Ohms and max = 2 Ohms.

 The TS-5400 Application Software package also comes with a set of predefined hardware actions which can be found in default directory 'C:\Program Files\Agilent\TS-5400 System Software\actions'.



Figure 7. Specifying the switching paths in a test

# Signal Switching via Pin Matrix Card



Figure 8. Block diagram showing the switching path connections via pin matrix card

Another common example of signal switching is to measure DC voltage using a DMM. Like the resistance test, if we were to measure the voltage at any UUT pin with respect to ground, then we have to probe the DMM high and low pins to the pin and its reference ground (see Example 7).

Other than a DMM, you can also add other instruments (for example, arbitrary function generator, frequency counter, communication card, etc.) to the instrument matrix. Agilent E8792A pin matrix card equipped with 16 matrix rows for instrument inputs and 32 rows for measurement points.

Example 7	
Measu	ring the voltage
Step 1	Click <b>Insert &gt; Test</b> , then type 'Check +12V Supply Voltage' in the Test Name space.
Step 2	Click <b>Insert Switching</b> , double-click <b>Add Path</b> in the Parameter space, then add the following switching paths. Path1 - <b>dmm:Hi   Abus1   +12V_Supply</b> Path2 - <b>dmm:Lo   Abus2   DUT_Grn</b> This switching action closes the relay paths from DMM to UUT via Abus1-2 of pin matrix card. The '+12V_Supply' and 'DUT_Gnd' are node names for UUT pins.
Step 3	Insert 'dmmMeasureDCV' <sup>3</sup> action, set AccuracySpeed = 1 and ExpectedReading = 12 Volts. This action will trigger the Agilent 34411A DMM to make a DC voltage measurement.
Step 4	Click <b>Limits</b> , set 'Kind of Limits' to 'Nominal Tolerance', set nominal = 12 Volts and tolerance = 0.2 Volts.
3 The TS	5400 Application Software package also comes with a set of prodefined hardware

 The TS-5400 Application Software package also comes with a set of predefined hardware actions which can be found in default directory 'C:\Program Files\Agilent\TS-5400 System Software\actions'.

### Load Switching via Load Card

A load card is a collection of relay channels which usually used to construct the different configurations of simulated load for a UUT. It can be a simple one-to-one or in a multiplechannel bridge configurations. While for the simulated load, depending on the actual load-to-be-connected, it can be purely resistive load, combination of resistive and inductive or just a straight switching path.

Using a load card, it allows the users to connect/disconnect a load channel or select load connections to either pull-up (connect to positive supply) or pull-down (connect to ground) configurations. In TestExec SL, since all node names are already pre-defined in the topology files, configuring a load switching path is easy. A poweron test is a good example to demonstrate how to configure a load card. To supply 12 V to a UUT via a load card, we need to close the switches along the path from power supply to UUT, and then set the power supply to 12 V (see Example 8).

Poweri	ng Up the UUT
Step 1	Click <b>Insert &gt; Testgroup</b> , then type 'Power Supply Setup' in the Testgroup Name space.
Step 2	Click Insert Switching, double-click Add Path in the Parameter space, then add the following switching paths. Path1 - SU0-PowerBus1   loadcard1:Pwr1 Path2 - SU0-PowerBus2   loadcard1:Pwr2 Path3 - loadcard1:Chan1   loadcard1:Load1 Path4 - loadcard1:Chan2   loadcard1:Load2 This switching action closes the relay paths from UUT to power supply via channel one to power bus one (ground connection) and channel two to power bus two (positive supply connection).
Step 3	Insert 'psProgVI' <sup>3</sup> action, set Voltage = 12 and Current = 0.2. This action will set the power supply to 12 V with 200 mA current compliance.
Step 4	Insert 'DelayMillisecond' action, set Milliseconds = 500. This action will set a delay to the testplan for 500 msec, usually for the voltage to stabilize.

 The TS-5400 Application Software package also comes with a set of predefined hardware actions which can be found in default directory 'C:\Program Files\Agilent\TS-5400 System Software\actions'.



Figure 9. Block diagram showing the switching path connections via load card

### Load Switching via Load Card

Agilent load card also includes the sense resistor for measuring current of a particular channel. For example, E6176A load card comes with a 3 W, 0.05  $\Omega$ , 0.1 percent sense resistor for each of the 16 load channels. Users can calculate the current flowing through the path by measuring the voltage drop across the sense resistor with a known value using Ohm's Law (see Example 9).

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Software\actions'.

Measu	ring the current
Step 1	Click <b>Insert &gt; Test</b> , then type 'Check +12V Supply Current' in the Test Name space.
Step 2	Click Insert Switching, double-click Add Path in the Parameter space, then add the following switching paths. Path1 - dmm:Hi > Abus1   Current Sense + Path2 - dmm:Lo > Abus2   Current Sense - Path3 - loadcard1:ISense+   loadcard1:LdSense+2 Path4 - loadcard1:ISense-   loadcard1:LdSense-2 This switching action closes the relay paths from DMM to sense resistor in the load card via Abus1-2 of pin matrix card. Current Sense nodes are located at the SLU backplane which also connected to the load cards.
Step 3	Insert 'dmmMeasureCurrent' <sup>3</sup> action, set AccuracySpeed = 1, ExpectedCurrent = 0.1 Amps and SenseResistance = 0.05 Ohms. This action will trigger the Agilent 34411A DMM to make a DC voltage measurement and then calculate the current by dividing the measured voltage by sense resistor value.
Step 4	Click Limits, set 'Kind of Limits' to 'Min/Max', set min = 0.05 and max = 0.15.
3. The TS-	5400 Application Software package also comes with a set of predefined hardware which can be found in default directory 'C'\Program Files\Anilent\TS-5400 System

Conclusion

The Agilent TestExec SL Switch Manager is an excellent feature created for managing the complex switching for functional tests. The advantage is particularly obvious as the number of switching channel increases. It simplifies the steps needed to generate switching paths and to control their status. On top of that, it also allows users to use logical names to alias the physical switching nodes. These characteristics help users of the TestExec SL to shorten the testplan development time as well as enabling ease of maintenance.

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