Vectorless Test Solutions

An analysis of performance differences between VTEP, FrameScan FX and TestJet Enhanced

White Paper

Table of Contents

Agilent Technologies

The Evolution of TestJet into VTEP

Micro-processors, controller ICs, memory chips and ICs that have speed and voltage levels that are beyond the regular ranges that conventional In-Circuit Testers can support. These devices pose various challenges to test engineers when it comes to test coverage. In today's fast paced manufacturing test environment, test engineers simply cannot afford the time and effort to develop functional test libraries for digital devices. Even if time is not a factor, the complexity of today's integrated circuits makes test libraries development almost impossible.

In 1994, TestJet was invented and launched by Hewlett Packard's Test and Measurement organization, which later became Agilent Technologies. TestJet has since been so widely adopted that almost all ICT vendors today offer this Agilent patented technology. Teradyne leveraged TestJet to develop FrameScan, while GenRad named theirs Opens Xpress and many other companies simply retain the name TestJet as part of their product offerings.

The wide adoption of Agilent TestJet Technology attested to its outstanding capabilities enabling fast, easy and effective test of an IC, connectors and sockets.

TestJet technology was patented and introduced by Agilent in 1994 after several years of research and refinement. The technology makes use of the metal lead frame that connects the external pin of the IC to the internal silicon die. Back then, the size and shape of lead frames were very similar from device to device. With the wide-spread popularity of this type of IC design then, TestJet became the de facto vectorless test solution for IC packages like QFP, SOIC, PLCC, etc.

TestJet uses an external plate, suspended above the component, and separated from the lead frame by the plastic or ceramic material of the device housing. The lead frame and the external plate form a small capacitor that can be measured by stimulation with an AC source. Each pin (input, output and power) consists of a part of the lead frame, enabling each of them to be detected as a separate capacitance.

However, with the improvement of IC packaging technology over the years, lead-frame based design is slowly becoming obsolete with new packages, such as Ball Grid Arrays, taking over. BGA devices typically do not have as much metal framework as compared to the older packages. As TestJet relies heavily on the lead frame of devices for enabling in-circuit testing, the evolution of frame-independent packaging has posed increasing limitations on TestJet.

Without a good lead frame to form good capacitor, TestJet measurements on newer devices have become so small that most in-circuit testers can no longer differentiate between a TestJet Capacitance and an Open connection capacitance. Many ICT vendors try to solve this problem by pumping in a stronger stimulus to obtain a higher measured value. Unfortunately, these methods simply increase the magnitude of the stimulus and response, and fail to provide an effective differentiation between a good and bad solder joint.

To solve this fundamental problem, Agilent came up with a significant change to the fundamental hardware design. The resulting solution became what is now commonly known as **the Agilent *Medalist* Vectorless Test Enhanced Performance (VTEP) technology.**

Agilent's VTEP is a patented technology that builds on the legacy of Agilent TestJet, combining next-generation test hardware and software to dramatically improve test coverage and reduce test development time.

Understanding TestJet Theory

Though TestJet and VTEP may already be popular with many test engineers, it is important to truly understand the test techniques behind them so as to understand the actual difference between a TestJet and VTEP test as well as their capabilities and limitations.

Fundamentally, VTEP and TestJet measure the signals in the same way.

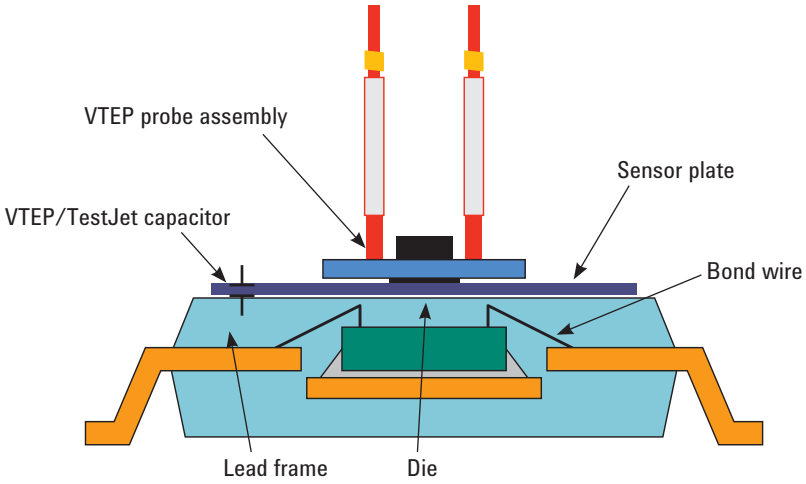

Figure 1. Both VTEP and TestJet employ the same methodology to measure the device signals being tested on printed circuit board assemblies

In the example above (Figure 1) on a regular Quad Flat Package (QFP) device, the VTEP probe measures the small capacitance formed by the VTEP Capacitor between the sensor plate and the lead frame of the IC. In the case of an open in the IC pin soldering, the resulting tiny air gap in the open creates additional capacitance in series with VTEP capacitor. This additional capacitance is much smaller than that of the VTEP capacitor. The series combination of the TestJet capacitor and this additional pin capacitor is smaller than either capacitor. So, by positioning a test threshold, VTEP/TestJet will be able to identify those pins that are significantly smaller than the expected threshold value, and thus discriminate between well- and poorly-soldered connections.

This technique works well with a device that has a significant amount of metallic surface area to form the capacitance with the sensor plate. But when the surface area of the lead frame shrinks, the capacitance shrinks accordingly. Similarly, when the structure of the device under test changes with more capacitance added, like the case of an ungrounded heat sink, the capacitance will be affected.

Understanding Why TestJet is Unable to Test BGA Devices

Why can't TestJet be used to test BGAs?

Ball Grid Array (BGA) packages have a different internal structure compared to that of regular lead frame based components like QFP, etc. BGAs vary in pitch, ball placements, and the presence of thermal plates and shielding. And as BGAs contain little or sometimes no lead frames at all, this leaves the measurement to depend only on the wire bonds and traces, which now measure way below 20fF. With TestJet, both good and bad BGA ball joints will be measured at below 20fF with hardly any differentiation. This renders the TestJet measurement ineffective for BGA testing.

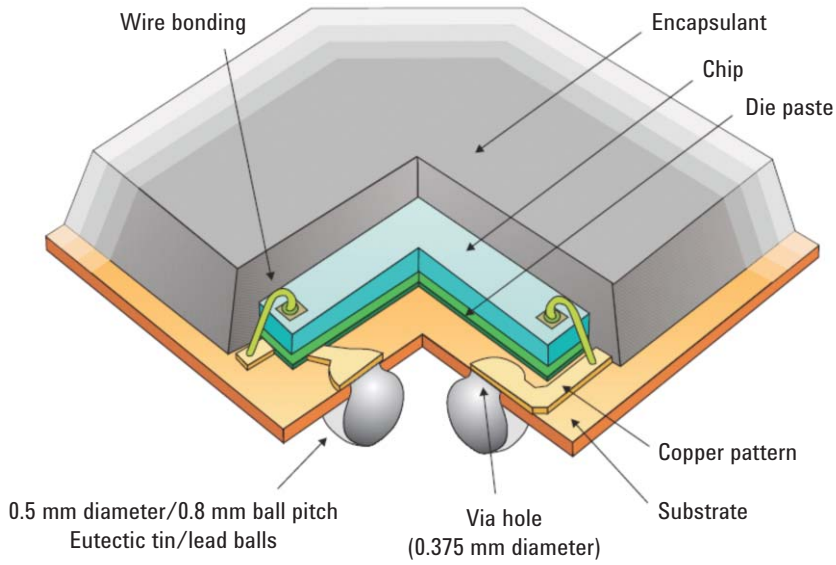

Figure 2. Typical BGA package design

Understanding Why TestJet is Unable to Test Through an Ungrounded Heat Sink

Why can't TestJet test through an ungrounded heat sink?

A heat sink is a piece of metal used to disperse heat through conduction. Heat sinks are usually closely attached to the IC surface via epoxy or simple mechanical hold-down clips or screws. This helps minimize the gap between the heat sink and the surface of the IC.

Given the example below, the heat sink essentially becomes a metallic structure that is inserted into the path of the TestJet capacitor. This splits the original capacitor that is formed by the sensor plate and the lead frame into two capacitors in series. The first capacitor is formed by the lead frame and the heat sink, and the second capacitor is formed by the heat sink and the sensor plate. As the heat sink is not grounded, the TestJet stimulus will propagate through both the capacitors and get measured by the TestJet Probe.

However, instead of a single capacitor, we now have 2 capacitors connected in series. This drastically lowers the overall capacitance measurement, so much so that the tester may not be able to measure anything at all.

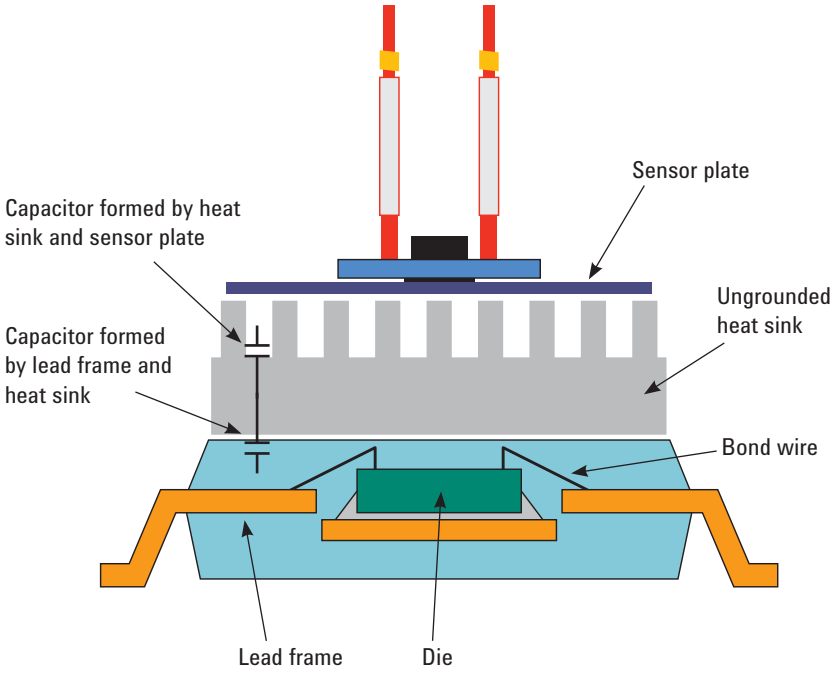

Figure 3. Testing through ungrounded heat sink

Teradyne's Solution: FrameScan FX Software and FSX Probe

Teradyne acquired GenRad in the 2001, and together with it, GenRad's Opens Xpress. There has not been any redesign on the Opens Xpress solution since then. Opens Xpress and Teradyne's FrameScan are TestJet equivalents targeted at large ICs with a good amount of lead frame area. To answer to the challenge of testing BGAs, Teradyne improved FrameScan solution, calling it FrameScan FX. FrameScan FX consists of some software improvements and a new FSX active probe.

The new software incorporates a Precision mode which is similar to Throughput Adjustment 1 on the Agilent TestJet/VTEP solution. This mode basically extends the integration time to collect more samples of the response so as to improve the signal to noise ratio. It also employs a feature to automatically set the test limits on a per-pin basis during test learning process and at runtime; the software can automatically adjust test limits to cater for systematic shift in the measured value as a result of uneven sensor plate positions, etc.

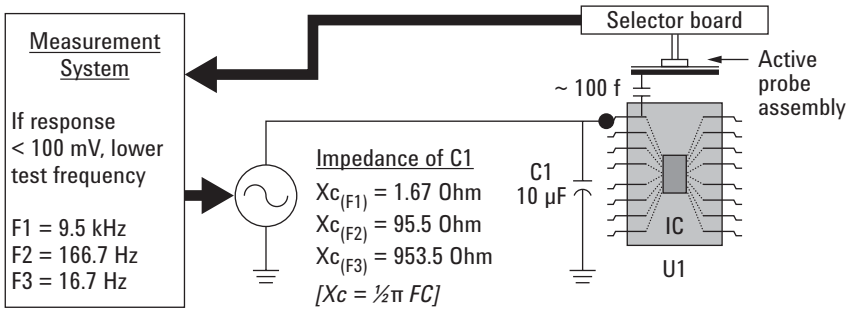

Figure 4. How FrameScan FX works

Another interesting feature that the software offers is the sensing of large capacitive load on the tested pins of the IC and the adjustment of test frequencies, to try to eliminate the loading effects. The standard test stimulus of FrameScan FX is 0.4 V_{peak} at 9.5 kHz. When a test response falls below a 100 mV (internal fixed threshold) due to a large capacitive load on the board, the software automatically drops the test frequency and attempts the measurement again.

According to training material available from Teradyne's website, the tests use three fixed frequencies. Other than the usual 9.5 kHz, the first lower frequency level is 166.7 Hz and the second level is at 16.7 Hz. At these lower frequencies, the large capacitive loads at the DUT will have higher impedance and will not load the signal significantly. However, due to the lower frequency, the impedance of the tested pins with capacitance in the femtofarad range becomes extremely high such that it may result in the response received at the sensor plate becoming very small. If the response is weak, this makes it susceptible to ambient noise and will be dependant on the new FSX probe to filter and boost the signal sufficiently to allow for a good measurement.

The FSX probe is the hardware improvement in the FrameScan FX solution. This low noise amplifier increases the response signal and feeds it back to the mux card for further noise filtering and signal amplification. The FSX probe uses the same selector board (mux card) like the earlier FrameScan amplifiers. This allows users to mix both types of amplifiers into a single fixture with the test limits being learned separately for each type of amplifiers.

TRI's Solution: TestJet Enhanced

TRI's TestJet is the same technology as the aged old TestJet technology that was very well received in the 90s. Similarly, this technology can longer support today's world of BGAs. Therefore, TRI launched an improved version of their TestJet solution and named it TestJet Enhanced. TestJet Enhanced had improvements made to both software and hardware of the TRI tester system. On the hardware portion, a new mux card was introduced together with a new System Management Board (SMB). The original TestJet probe assembly remains unchanged. Therefore, for users to upgrade to use this new technology, all that is needed is to change the mux card and the SMB. Major improvements made to the hardware are the addition of several analog and digital filters. These are being added to support the change in the software testing technique.

TestJet tests are generated by a learning method on the tester. The learning process starts with a standard 10 kHz stimulus and the response is picked up by the standard TestJet probes. The response goes through the mux card and into the SMB. In this path, the response will pass through some amplifier and filter, corresponding to the source frequency. The amplifiers amplify the response with the noise, with the band pass filters filtering it later. The resulting response will then be split into its individual frequency components, like a spectrum analyzer, and attempts to extract only the source frequency component from the response. The magnitude of the extracted frequency component is then checked to determine if the measurement is valid. Determining a valid measurement is simple. A reference value is preset in the system for this purpose. If the measurement does not meet the reference value, then this measurement is considered invalid.

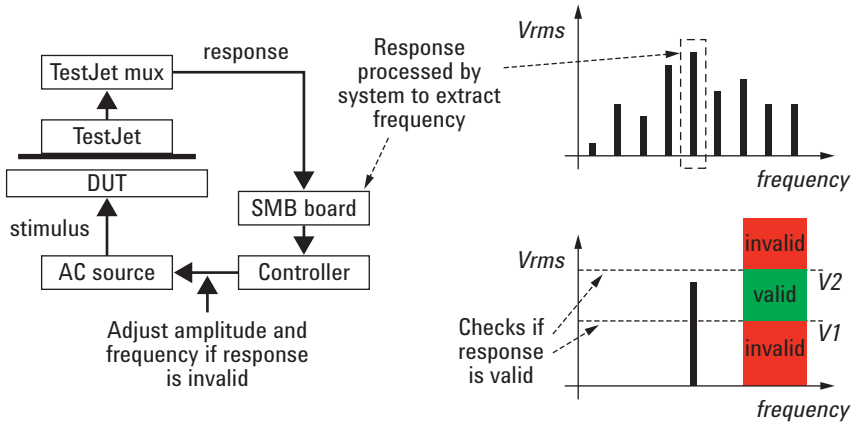

Figure 5. Block diagram of TestJet Enhanced

For invalid measurements, the software instructs the system to increase the amplitude and frequency of the stimulus and repeats the learning process all over again. By increasing the amplitude at the stimulus, it is obvious that the response will increase as well. In addition to the amplitude increment, the frequency is also increased. Since the basic TestJet measurement is really testing a very small capacitor, changes to the frequency simply changes the impedance of the capacitors ($Xc = \frac{1}{2}\pi FC$). Hence, increasing the frequency of the stimulus will make the impedance of the capacitors smaller, thus helping the stimulus to propagate through.

BGAs that have little lead frame form very small capacitors for measurement. As such, with the increment in amplitude and frequency of the stimulus, the impedance of the capacitors is lowered and the stronger signal will then be able to successfully couple over to the TestJet probe assembly for measurement. This is essentially how TRI TestJet Enhanced works.

Agilent's Solution: VTEP

The VTEP hardware offers key improvements over TestJet, allowing the former to provide better and more efficient tests over the older TestJet hardware design. The improvements offered by VTEP provided Agilent the opportunity to innovate new vector-less test techniques on top of the original VTEP hardware.

VTEP has 4X better standard deviation compared with TestJet

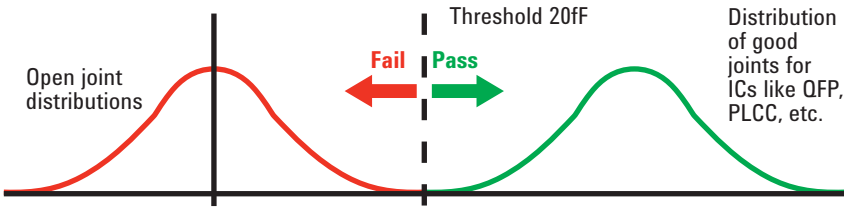

Figure 6A. Distribution of a typical TestJet measurement

The GREEN distribution represents a measurement distribution of a good joint whereas the RED line represents a distribution of an open joint. Because of the availability of lead frames, a good joint typically measures well above 20fF, leaving a nice margin from the failing distribution of a bad joint.

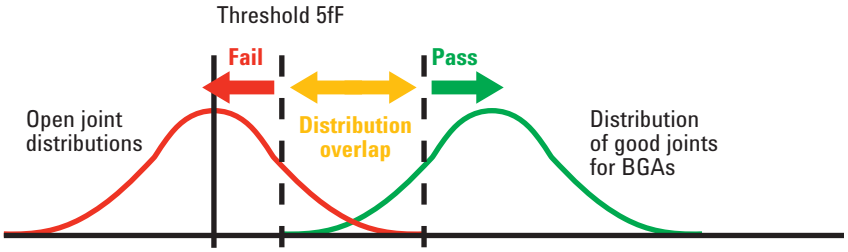

Figure 6B. Distribution overlap between pass and fail for a BGA device without lead frame using TestJet measurement

Applying the same distribution on a BGA device that does not have much lead frame, the measurements becomes a lot smaller, so small that the pass and fail distributions is now overlapping each other (as can be seen from Figure 6B). Because of the lack of lead frame surface area, BGA measurements can fall as low as 5fF. This basically results in unreliable tests as a failed joint may be recognized as a Pass.

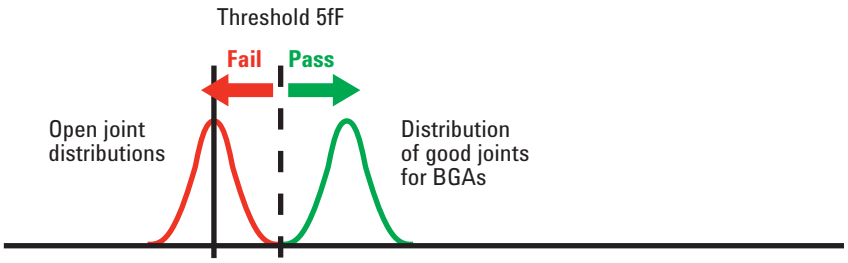

Figure 7. VTEP is able to capture pass and fail measurements clearly, providing increased sensitivity performance compared with TestJet

The a major improvement to the VTEP hardware is the increased performance in the standard deviation of its measurements, which have been verified to be up to four times better than TestJet[1]. The distribution of the measurements becomes much narrower, and therefore, provides effective differentiation between a Pass and Fail joint.

1. *5989-0728EN.pdf*

Agilent's Solution: VTEP (continued)

iVTEP tests µBGA, flip chips and heat sinks

Building on a base of VTEP hardware that can provide high resolution measurements, many cutting edge technologies have since been invented to answer to new industry challenges faced by vectorless test techniques. Amongst these technologies is the iVTEP technology in the VTEP v2.0 test suite.

Micro BGAs and flip chips contain even less lead frame as compared to a typical BGA. This simply means that the measured capacitance is going to shrink, at times to levels below 5fF. Testing pins with such a small capacitance value can no longer depend on a simple "response and limits checks" method where a response is measured by the test system and simply placed on a set of high and low limits to determine its pass/fail result. This is because at such small capacitance, ambient noise and variations in the DUT structure become significant factors affecting the accuracy of the measured result. A slight gap on the sensor plate and the DUT may generate a difference in measurement significant enough to throw it over its test limits. Test methods use different stimuli during the test generation stage, with their software enabled to learn the settings of the stimulus in order to get a decent test response. Then during runtime, the tester simply applies the learnt settings on the stimulus for each pin and takes the result to a set of high and low limits for comparison.

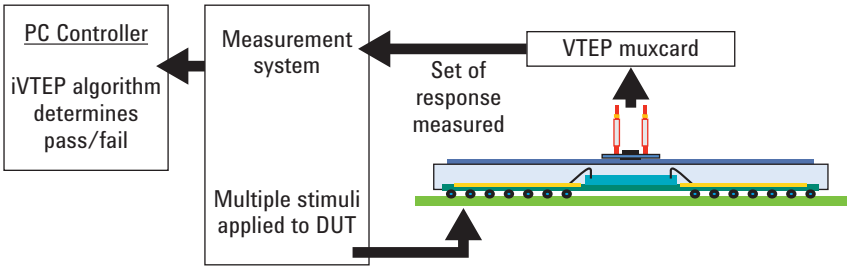

Figure 8. Block diagram of an iVTEP measurement process

iVTEP is a technology that applies a complex algorithm to the measurements taken such that the effect caused by noise and other variations is minimized during each test cycle. To do this, the iVTEP algorithm needs to receive a set of test values taken on the same pin with different stimulus amplitude settings. With these measurements, the algorithm then calculates the actual response by minimizing the effect of noise and other variations. This is the reason why iVTEP takes a few measurements during runtime. By doing so, iVTEP can now effectively differentiate between a good and bad joint even when the capacitance gets very small on a micro BGA or a heat sink.

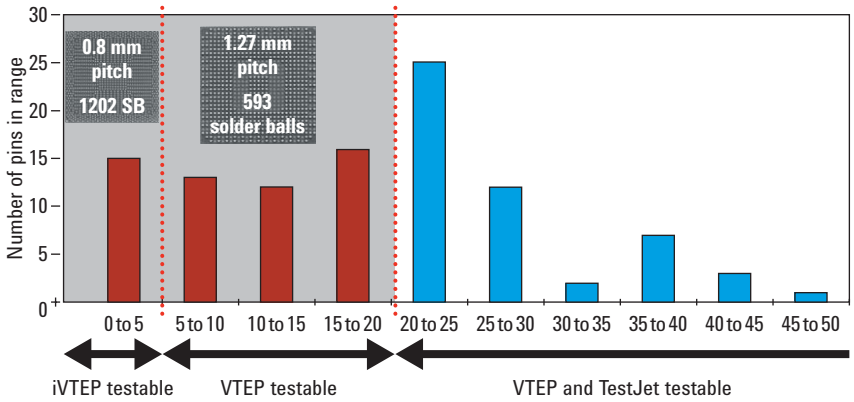

Figure 9. Comparison chart of TestJet, VTEP and iVTEP measurements

Coverage Comparisons

Agilent TestJet Versus VTEP v2.0

A simple comparison was conducted to see the difference in coverage achieved using Agilent TestJet and Agilent VTEP v2.0. Comparison was conducted on a desktop motherboard from an ODM in Taiwan. The motherboard is a mature product running on a TRI TR518 system which does not use TestJet at all. As part of the evaluation requirement, a new Agilent *Medalist* i1000 in-circuit test press down fixture was built and a set of TestJet and VTEP hardware were made available. The test program was regenerated for the board and the coverage of IC and Connectors using TestJet and VTEP tests were respectively collected for comparison. Comparison results show a drastic increase in the coverage percentage just with the use of the VTEP hardware itself. Further improvements were also realized using iVTEP and Network Parameter Measurement (NPM) technology, both part of the VTEP v2.0 test suite.

Table 1. VTEP significantly increases coverage of testable pins compared to TestJet

	TestJet	VTEP	Difference
ICs			
Testable pins	1201	1201	Increased 57.1%
Tested pins	482	1168	
Coverage	40.1%	97.2%	
Connectors			
Testable pins	450	450	Increased 40.8% Additional Coverage on VCC and GND pins also achieved with NPM technology on DDR2 and SATA connectors
Tested pins	260	445	
Coverage	58%	98.9%	
Testing through heat sink			
Testable pins	587	587	Increased 76.8% 131 pins by tested by VTEP 429 pins by tested by iVTEP
Tested pins	109	560	
Coverage	18.6%	95.4%	

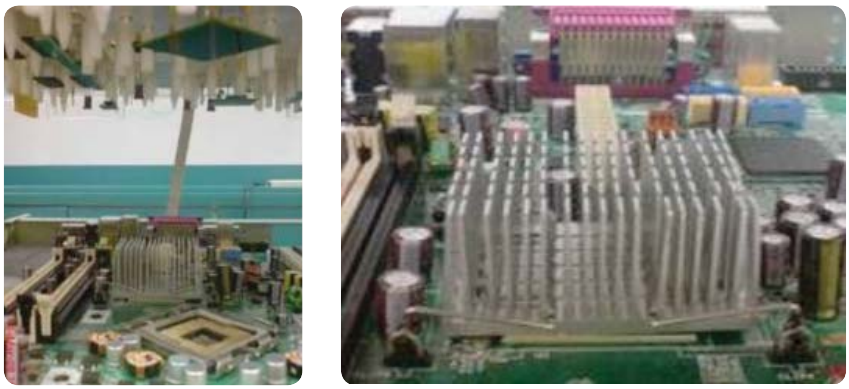

Figure 10. Devices with heat sink testable with iVTEP (close-up on the right)

Coverage Comparisons

Teradyne FrameScan FX Versus Agilent VTEP 2.0

Details of comparisons between Teradyne's Opens Xpress, FrameScan and FrameScan FX for some typical devices on a PC motherboard can be found on Teradyne's website. Agilent conducted a separate experiment using similar devices in terms of functionality and packaging type to obtain the test coverage using both TestJet and VTEP. Results of the experiments are shown in Table 2 below.

Table 2.

Device	Type	Opens Xpress Coverage	FrameScan Coverage	TestJet Coverage	FrameScan FX Coverage	VTEP Coverage
U8A1	82562EZ	3.0%	36.3%	*94.9%*	74.71%	*100%*
U8G1	82801F	56.5%	62.6%	*96.8%*	93.01%	*100%*
U2J1	Unknown	90.09%	90.09%	*No data*	100%	*No data*
U34	Northbridge	90.1%	91%	*83.6%*	95.8%	*98.1%*
U58	CPU socket	82.8%	98.9%	*99.6%*	98.9%	*100%*
J1	DIMM connector	92.8%	100%	*100%*	100%	*100%*

Details of the comparison study

- **U8A1:** 82562EZ is an Ethernet controller in a 15 x 15 mm 196 pin 1 mm-pitch PBGA package. The TestJet and VTEP results are for a similar Intel LAN chip in the same package (82559ER).
- **U8G1:** 82801F is a south bridge. There were approximately 258 signal pins on this 421 pin part. NO pins had values less than 20fF.
- **U2J1:** The device is unknown so VTEP and TestJet data is not provided.
- **U34:** We used 82845 and 82855 as target north bridge chips. It is unclear what north bridge chip Teradyne tested. It could be an older technology since Opens Xpress and FrameScan gave almost the same coverage. With the given data, VTEP provides 14.5% more than TestJet and 2.3% more coverage than FrameScan FX.
- **U58 and J1:** Most DIMMs and sockets are easily tested since they usually provide sufficient signal with relatively little noise. These parts are normally not difficult for technologies such as TestJet. TestJet and VTEP both provided 100% coverage.

From the comparison results, Agilent TestJet demonstrated results comparable with FrameScan FX, while VTEP surpassed both on all device coverage.

Coverage Comparisons

TRI TestJet Versus Agilent VTEP 2.0

Results for the TestJet and VTEP comparison study were collected from an actual production evaluation at a huge volume manufacturing site in Penang, Malaysia. The product is a memory daughter card of medium complexity. As such, there was no digital test requirement in the test strategy. The test platform used on this board was a TR518 deployed with only unpowered analog and TestJet tests.

The evaluation used the Agilent *Medalist* i1000 pressdown in-circuit test system to enable the end-user's TR518 test fixture to be easily ported to the i1000 system without the need to build a new fixture. TRI TestJet probes were replaced by VTEP probes and a VTEP mux card was also attached to the fixture for the evaluation. The main purpose for that evaluation was to evaluate the feasibility of transporting a TR518 fixture and program between the Agilent *Medalist* i1000 and the TR518 system.

Since the test program was converted from the TR518 system, the unpowered analog test coverage is similar. For the comparison of VTEP, the original TRI TestJet test was removed and a VTEP test was generated on the i1000 tester. The below comparison does not include parallel or tied pins. The results showed an increased in the number of testable pins being determined by VTEP over TestJet.

Table 3. Coverage comparison between VTEP and TestJet

			VTEP		TestJet	
Device	Total Pins	Testable	Tested	Coverage %	Tested	Coverage %
U1B1	59	8	7	87.5	4	50
U1C1	59	6	5	83.33	5	83.33
U1C2	59	7	6	85.71	5	71.42
U1C4	59	6	5	83.33	4	66.66
U6A1	24	23	23	100	22	95.65
U8D1	14	12	12	100	11	91.67
J4A1	60	42	42	100	38	90.47
J5F1	150	72	20	27.78	24	33.33

J5F1 is a 90-degree-edge connector. However, due to the design of the fixture where the sensor plate of the VTEP and TestJet probes were mounted on the top plate, the resulting coverage became very limited. This also goes to show the importance of good design and workmanship in the fixture fabrication process.

Pros and Cons of Various Features

The vectorless test solutions offered by Agilent, Teradyne and TRI show some similarities among the features that each provide. Features like automatic threshold settings on per pin basis, adjusting test source parameters for weak measurement pins and improvements to hardware amplifications and filtering are similar in general. There are, however, some considerations to be taken into account when using these features. Below is a table listing some of the features offered and considerations prior to using them.

Table 4. Features table

Feature	Vendor	Considerations
Precision mode	Teradyne	This achieves better noise immunity by taking more samples of the response at the expense of test time.
Slow/fast mode	Agilent	Additional samples are taken from the response to achieve high signal to noise ratio. Test time is affected as a result of the additional samples.
Automatic frequency adjustment for capacitive loaded pins	Teradyne	This is mainly used to counter the loading effects of large capacitors at the pin under test. By dropping to a lower frequency, this makes the impedance of the capacitive load higher, as such, preventing the loading of the test stimulus. However, by lowering the frequency, this also increases the impedance of the lead frame capacitance which is intended to be measured. This results in a weaker response which is susceptible to ambient noise. This may result in unstable or ineffective tests.
Automatic limits adjustments for systematic test value drift	Teradyne	Test measurements may fluctuate due to bad probe contacts or improper positioning of the sensor plates during some test cycles. This results in a systematic drift in test results across the group of pins for the device under test. This drift can be automatically taken into account by changing the test limits to allow it to pass. As this feature runs automatically at runtime, there is a potential risk of the software automatically changing the test limits and passing a defective board.
FrameScan FX per pin test limits generation	Teradyne	Employs an algorithm to calculate the test limits of each pin based on statistical results of adjacent pins. This algorithm attempts to model the effects of stray capacitance on the board resulting from the board traces, etc to the senor plates. This value is connection-independent as it is always present regardless of whether the pin is soldered or not. By being able to estimate this connection-independent part of the measurement, the test limits can be effectively set. The above information is obtained from a published patent. Patent # 5391993. Publication # US005391993A. The patent, dated February 21, 1995, based its algorithm on a QFP-like IC model where pins are arranged around the device in a symmetrical manner. This assumes that the wire bond and lead frame areas of each pin are similar to the pin that its position is directly opposite that of its own. However, this is not applicable in today's environment where BGAs, FlipChips, etc are used on almost all boards.

Feature	Who	Considerations
VTEP per pin test limits generation	Agilent	Using a set of parameters set by the users, the software algorithm derives the test limits of each pin based on its Standard Deviation, Mean, and other statistical data with a set of VTEP parameters definable by the user. Within the set of definable parameters is the Minimum CPK setting which allows the user to put a threshold on the CPK which is being used to determine a testable pin. This results in achieving a stable and repeatable test.
TestJet Enhanced per pin test limits generation	TRI	Test limits generated are not based on any CPK calculations. Test limits are generated automatically by a simple percentage multiplier which can be adjusted by the user. Without taking standard deviations into calculations, it is not possible to guarantee a threshold that can effectively differentiate between a good joint and a bad joint for cases where the good and bad joints measurement distributions overlaps each other.
iVTEP test algorithm	Agilent	Takes multiple test measurements with different source amplitudes and undergo statistical calculations to derive the test results. This effectively removes the effects of noise present in the measurements so as to obtain a stable reading.
NPM test algorithm	Agilent	This provides test coverage on Power and Ground pins on connectors and sockets based on connector modeling and result analysis. All these are built on a high SNR foundation that VTEP hardware achieves.
Cover-Extend technology	Agilent	Combining Boundary Scan technique with VTEP test technology, this provides a means for test developers to overcome limited access issues where test coverage by normal VTEP and TestJet are not possible.

Conclusion

All three vectorless test solutions offer good coverage for conventional devices which offer large metallic surface areas to perform a reliable test comfortably. The real challenge comes with the miniaturization of ICs, connectors and sockets.

Similar to Agilent's VTEP to counter increasingly limited access due to miniaturization, Teradyne's enhanced its FrameScan FX with the new FSX probes. This new set of hardware increases the gain of the amplifiers and makes previously untestable pins, testable again. FSX probes improved signal to noise ratio, giving it the ability to clearly differentiate pass and fail pin readings on BGAs and other small lead frame devices. It is stated in Teradyne's website that FSX probes have better SNR than Agilent's VTEP probes. However, there is a limit to how far this SNR will go. While improving the SNR solves some of the BGA test challenges, this solution will not work for devices that go beyond the simple lead frame capacitance measurement. Devices like µBGAs, flip-chips and heat sinks simply render this hardware unusable.

Teradyne incorporates a software solution to change the test source frequency to counter the effects of capacitive loads on the board. This method may effectively isolate the effects of the capacitive load on the board, but it may cause a drop in test response since the actual capacitance that the stimulus is suppose to measure is very small. In addition, testing a small capacitance usually doesn't go very well with low-frequency stimuli. Also included in the software release is the ability to automatically adjust the test limits during RUNTIME to cater for systematic shift in test devices where the readings drift for a significant set of pins for that particular device. This may be useful, but it is a cause for concern to have the test program automatically and dynamically change its test limits to cater for the board's test readings. This may accidentally pass an defective board without the user ever knowing.

TestJet Enhanced uses a slightly different approach. Instead of improving the gain of the TestJet probes, TRI works on the test stimulus and the receiving hardware to achieve a higher SNR for BGAs. In general, the approach increases the source stimulus, which also increases noise, and lets the receiving mux card and SMB handle the filtering of noise and measurements. If the measurement is low, bump the source stimulus up a notch and repeat the measurement again. This simple and straight forward method solves most of the BGA challenges but again, will not be sufficient for a device that does not have lead frames to rely on.

Another issue with this simple method is the failure to recognize that the response from each pin is different Therefore, simply using an internal threshold value to gauge if a measurement is valid will not be sufficient. Since the response for each pin of a device defers from pin to pin, putting them on a single set of thresholds only means that some of the pins that may be testable but fall below the threshold, may not be turned on for test. On the other hand, pins that may not be testable, may meet the threshold levels due to the increasing of source stimulus and eventually end up turned on for test. This results in ineffective tests which take up test time and offer no real coverage.

Agilent VTEP has similar limitations as those of FrameScan FX and TestJet Enhanced. It too, cannot cater for devices that do not have lead frames with which to allow measurement. This is where Agilent's innovation kicks in. Within the VTEP v2.0 test suite are iVTEP and NPM technologies. With iVTEP and NPM, vectorless testing is no longer just another lead-frame-sensor plate dependant capacitance measurement. What VTEP v2.0 has is a set of complex algorithms that performs analysis on test results to determine a pass or fail. This gives Agilent's Vectorless test solution an edge above the other solutions in the market.

Resources

Websites

http://www.agilent.com/see/vtep
http://www.teradyne.com/ict/teststation-in-circuit-test/framescan.html
http://www.tri.com.tw

Publications and patents

TRI
- Published Application US20080217175

Teradyne
- US Patent # 5391993
- Publication # US005391993A

Appendix – Features Comparison Table

Features	Teradyne FrameScan FX	TRI TestJet Enhanced	Agilent VTEP v2.0
Test source	0.4 V, 9.5 KHz	0.3 V, 10 KHz	0.25 V, 8 KHz
Test probe assembly	Amplifier built into FSX probe	Amplifier built into TestJet probe	Amplifier built into VTEP probe
Mux card	Filters and amplifier built in	Filters and amplifier built in	Filters and amplifier built in
Measurement system	DSP detector (PRISM)	DSP detector (ATM)	Phase sync detector (ASRU)
Test generation	Learn from good board	Learn from good board	Generated from board files
Test limits setting	Algorithm-based	% multiplier from mean value	CPK analysis algorithm
Per pin test limits	Automatic limits setting based on internal algorithm	Automatic % multiplier	Automatic limits setting based on user definable target CPK
Coverage optimization	• Drops frequency on capacitive loaded pins	• Increases frequency and amplitude on weak pins • Uses internal threshold value to determine testable pin	• Increases amplitude on weak pins • Uses iVTEP algorithm to determine testable pins • Uses NPM test technique to check on Connectors/Sockets Power and Ground pins
Stability optimization	• Precision Mode takes larger measurement samples to increase stability • Threshold algorithm adjusts test limits automatically to accommodate systematic shift in test values due to device variations like placement.	• Only one fixed mode of test	• Fast mode for higher test throughput • Slow mode takes larger measurement samples to increase stability
Limited access solutions	No public working solutions at time of release of this document	No public working solutions at time of release of this document	Cover-Extend technology. Hybrid technology between VTEP and Boundary Scan for limited access application. Works for all BScan devices.
Product offering	Licensed software. Requires fixed power supply options	Standard with TR8001 and TR5001 series system. No license required.	Standard with i3070 and i1000. No license required.
Estimated upgrade cost for system	• Software 5.9.0 upgrade – $3500USD • Fixed power supply option – $2200USD • FrameScan licence – $10,000USD	Required SMB card upgrade in system	None

www.agilent.com

Agilent Email Updates

www.agilent.com/find/emailupdates
Get the latest information on the products and applications you select.

Agilent Channel Partners

www.agilent.com/find/channelpartners
Get the best of both worlds: Agilent's measurement expertise and product breadth, combined with channel partner convenience.

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas	
Canada	(877) 894 4414
Latin America	305 269 7500
United States	(800) 829 4444

Asia Pacific	
Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Thailand	1 800 226 008

Europe & Middle East	
Austria	43 (0) 1 360 277 1571
Belgium	32 (0) 2 404 93 40
Denmark	45 70 13 15 15
Finland	358 (0) 10 855 2100
France	0825 010 700*
	*0.125 €/minute
Germany	49 (0) 7031 464 6333
Ireland	1890 924 204
Israel	972-3-9288-504/544
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
Switzerland	0800 80 53 53
United Kingdom	44 (0) 118 9276201

Other European Countries:
www.agilent.com/find/contactus

Revised: October 1, 2009

Product specifications and descriptions in this document subject to change without notice.

Printed in USA, November 3, 2009
5990-4947EN

Agilent Technologies