Make the Move From MTS 160 To *Medalist* i1000D In-Circuit Test

Application Note

Agilent Technologies

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Making the Big Move

Are your manufacturing defect analyzers (MDAs) meeting your testing needs? Do you want something better without needing to pay more?

As technologies push forward, test requirements are getting more stringent and complex. More and more printed circuit board assembly (PCBA) manufacturers are finding ways to refresh their production test strategy in order to deliver quality products, while at the same time keeping to the same low cost operating model that they have with their existing MDA testers.

The low cost operating model and high adaptability of the *Medalist* i1000D in-circuit test (ICT) solution fit these requirements like a glove. They are the main reason for the increasing interest from PCBA manufacturers to adopt the *Medalist* i1000D as a replacement for their old MDA systems which are mostly out of support life. Another reason is the numerous new innovations and features that Agilent introduces every year. By adopting the use of an Agilent ICT tester, manufacturers automatically get access to a wide range of new test technologies and methods.

Being a non-multiplexed system, the *Medalist* i1000D architecture is extremely similar to most MDA systems in terms of test resource structure and fixture wiring requirements. This eases the effort required to move from an old MDA system to the new i1000D.

Although the test program structure may be different between older test platforms and the new i1000D, it is just a matter of using simple translation software to bridge that gap. In most cases, the test files used on the MDAs are text-based and column-formatted. All the test information is consolidated into just a few files and it is not difficult to develop a translation script to automate the test program migration. Boards tested on the old MDAs are usually low in node count. So even if a software translation script is unavailable, creating the i1000D test steps by manual entry of the test parameters is still possible. Tedious it may be, but it is a small price to pay to open up a huge arsenal of the latest test technologies.

The bigger obstacle in migration lies with the need for a new *Medalist* i1000D test fixture. Working under a low cost operating model, manufacturers are often unwilling to make additional investments to build new i1000D test fixtures for their boards. Another reason can be that there are simply too many types of boards being produced, and it is not justifiable to scrap all the old MDA test fixtures and build a new i1000D test fixture for each board. Therefore, manufacturers are adopting a test adaptor based solution so that they can still use their existing MDA test fixtures on the *Medalist* i1000D.

Though reusing existing MDA fixtures may save on costs, it also means that some new test technologies cannot be used. One example is Agilent VTEP v2.0 *Powered*, which cannot be used with old fixtures as they may not have the drilled holes for the VTEP probes. In any case, it is time for the manufacturers to take the first step towards a greater future in production testing.

Be Updated, Not Outdated

Agilent Technologies has been in the forefront of in-circuit test technologies. Over the years, numerous innovations have been introduced to the industry, helping users maximize test coverage and lower testing cost. The *Medalist* i3070 takes the lead to bring ICT testing to a new level, with the *Medalist* i1000D in-circuit tester following closely.

Digital Test's MTS 160 is an old system with analog-only pin cards. It can be upgraded to include up to five digital cards, providing a maximum of 80 digital channels for the system. In today's digital test requirements, 80 digital channels are already insufficient to even perform a boundary scan connect test for a controller IC on most boards. This makes the system rather limited in the area of digital testing.

Without effective digital tests, users have to rely on other vectorless test techniques to achieve a reasonable level of test coverage for the ICs on the board. The answer in this case is OpensCheck, which is similar to Agilent TestJet.

When Agilent introduced TestJet technology a few decades back, it targeted lead frame based devices that provide good and reliable test measurements. However, as the industry evolved, using more BGA and even smaller packages, TestJet proved to be unreliable for these new devices and hence Agilent *Medalist* VTEP v2.0 *Powered* was introduced.

In general, moving the tests on to an Agilent *Medalist* i1000D opens up a whole new world of test possibilities, enabling users to effectively test products with little development effort. With the hybrid pins cards that support both analog and digital test resources, the *Medalist* i1000D is a much more scalable system that can be deployed for multiple product ranges. And with sufficient analog and digital resources, test coverage can be extended.

In some cases, the system has to be able to write manufacturing data such as the serial number and network addresses to the board under test. Using the on-board programming (OBP) library generator, the user can generate SPI or I^2C libraries with just a few clicks of the mouse. This greatly enhances the ability of the system to be used in a wide range of scenarios.

The benefit is evident. Migrating to the *Medalist* i1000D gives more flexibility and capability, while still maintaining the use of the low cost press-down fixtures from the MTS 160 system.

The *Medalist* i1000D is a full-fledged in-circuit tester with the operating model of a low cost MDA. This is the value proposition of the i1000D.

About the Digital Test MTS 160

The MTS 160 system from Digital Test is basically an analog system with multiplexed test resources of up to 1280. The test system consists of an analog measurement unit (AMU) on the first slot of the card cage, and a maximum of 10 analog mux cards in the following slots. However, if powered capability is required, an optional functional module rack has to be installed in the card cage, which reduces the number of usable slots for the analog mux cards (Figure 2).

Each analog mux card has four edge connectors with 32 resources each, making up 128 resources per card. These connectors are connected with 32-pin flat cables to the fixture on the press-down unit.

Note that the edge connectors are 34-pin connectors. Therefore, two pins of each 34-pin connector are left unconnected (NC). This is similar on the flat cables as well. Details of the resource allocations can be found in the appendix.

Figure 1. Digital Test MTS 160

Figure 2. Functional module rack installed in the card cage

About the Digital Test MTS 160

In addition to the functional module rack taking up usable slots, the system uses the test resources on the first mux card for press-down unit controls and also for nail finding. The first 32 resources are therefore reserved, making the first usable test resource start only at nail 33. On the MTS 160, test resources are referred to as Mux#, which will translate to Nail# on the *Medalist* i1000D. Table 1 shows the usage of the first six nails on the MTS 160.

Table 1. Usage of nail resources to control press-down unit

Test Resources for mux card 1	Usage
Nail 1 shorted to Nail 2	Signifies the press is in DOWN position
Nail 3	Controls the lighting of the PASS lamp
Nail 4	Controls the lighting of the FAIL lamp
Nail 5	Controls the press UP after test completion
Nail 6	Connected to GND of press-down unit control board

Figure 3. Functional rack installation in card cage reduces usable card slots

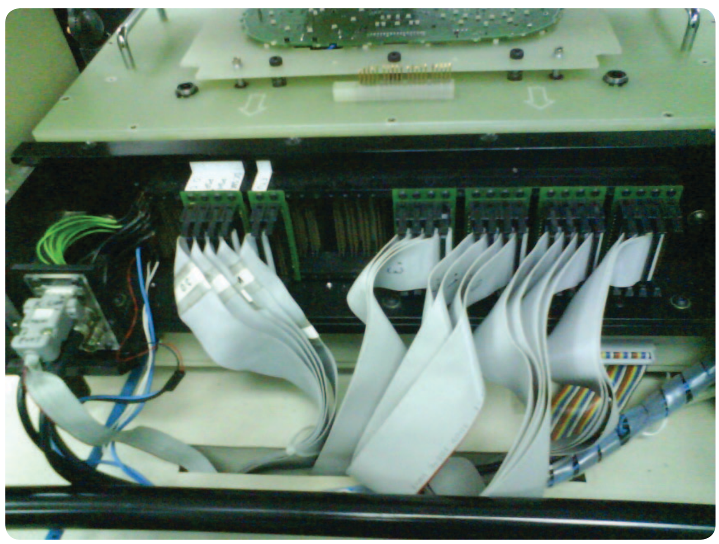

Figure 4. 32-pin flat cable connection to fixture interface

The test resources on the analog mux cards are multiplexed at 16:3. Each nail has three relays behind it, which connect to three of the measurement buses (A, B and C). Each set of 16 nails are connected together after their relays to these three measurement buses. These three buses are then further multiplexed into the rest of the buses (D, E and F). At any one instance, the user cannot connect two nails within a 16 nail block to both A and F, B and E, as well as C and D.

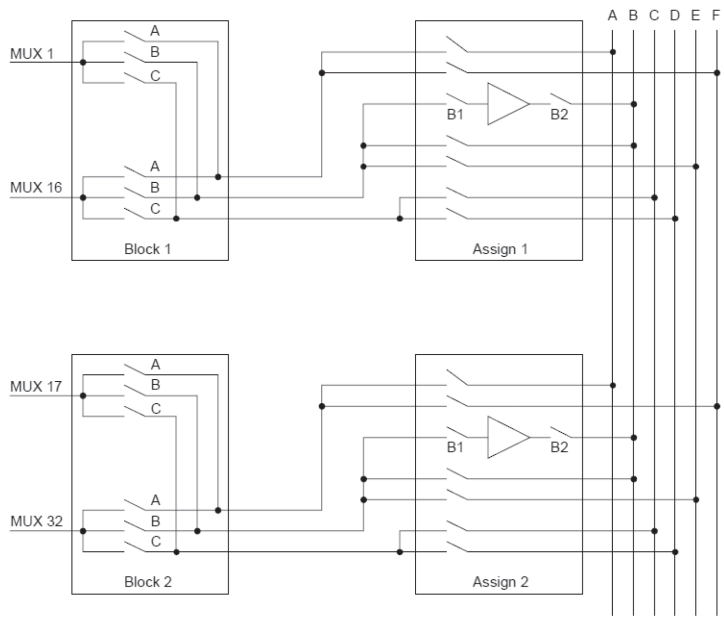

Figure 5. Test resource multiplexing of analog mux card

About the Digital Test MTS 160

About the Test Fixture

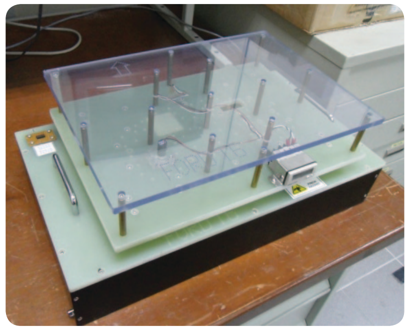

Figure 6. Front view of test fixture

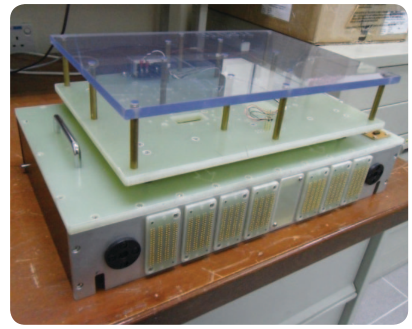

Figure 7. Back view of test fixture

The MTS 160 system uses an auto fixture lock mechanism to connect the fixture to the edge connectors, which in turn are connected to the mechanism and transferred to a panel of nails. The auto fixture lock mechanism simply pulls the fixture onto the panel of nails, making contact with the test resources. The wiring of the test fixture is similar to any MDA analog fixture, where each probe is wired to its designated nail number.

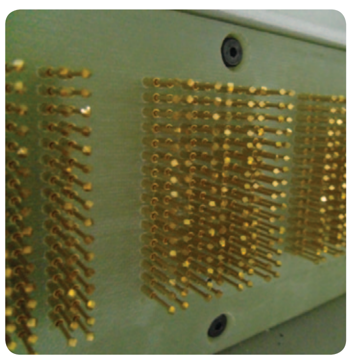

Figure 8. Resource nails on tester

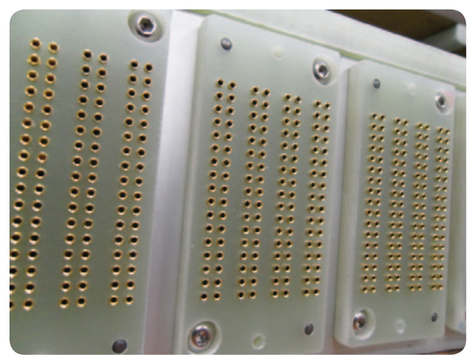

Figure 9. Receiver pad on fixture

Migration Process

Migration from a MTS 160 system to the *Medalist* i1000D involves hardware migration and software conversion. Hardware migration addresses the possibility of reusing MTS 160 test fixtures on the *Medalist* i1000D while software conversion retains the test limits and preferences.

Hardware Migration

It is always recommended that a new test fixture be built for the target test system, which will ensure that the new fixture is designed to perform to the requirements of that system. Of course, in a tight budget situation, reusing the existing fixture is the best solution. The following discusses how MTS 160 test fixtures can be reused on the *Medalist* i1000D.

Figure 10 shows the back of a sample MTS 160 test fixture that is adapted for use on the *Medalist* i1000D system. The test resources are organized in blocks of 128 pins. Each analog mux card in the card cage is connected to a block on the fixture.

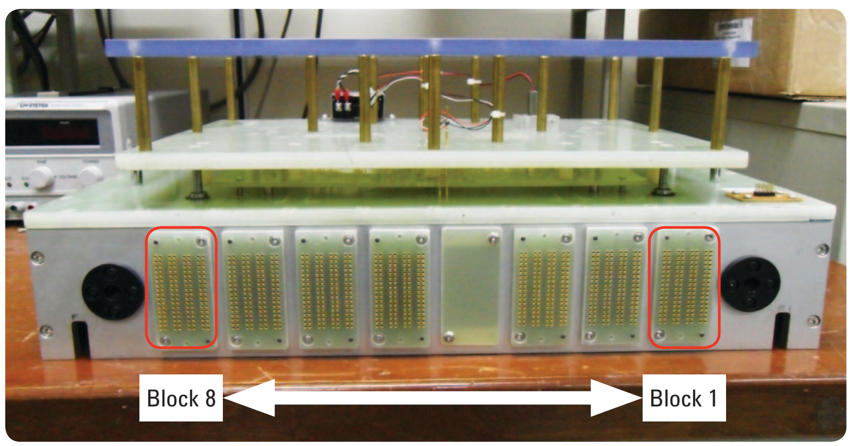

Figure 10. Test resource interface at back of MTS 160 fixture

Migration Process

The i1000D test resources are provided in 64-pin flat cables and require the test fixture to have the mating 64-pin connectors to receive the flat cables. This is a totally different interface from the MTS 160 fixture, therefore it is necessary to build an adaptor to interface between the i1000D flat cables and the MTS 160 test fixture. Building the adaptor is an additional cost, but it is a one-time investment which allows the reuse of all existing MTS 160 fixtures.

104	105	72	73	40	41	8	9
103	106	71	74	39	42	7	10
102	107	70	75	38	43	6	11
101	108	69	76	37	44	5	12
100	109	68	77	36	45	4	13
99	110	67	78	35	46	3	14
98	111	66	79	34	47	2	15
97	112	65	80	33	48	1	16
128	113	96	81	64	49	32	17
127	114	95	82	63	50	31	18
126	115	94	83	62	51	30	19
125	116	93	84	61	52	29	20
124	117	92	85	60	53	28	21
123	118	91	86	59	54	27	22
122	119	90	87	58	55	26	23
121	120	89	88	57	56	25	24

Figure 11. Test resource pin mapping for block 1 of MTS 160 fixture

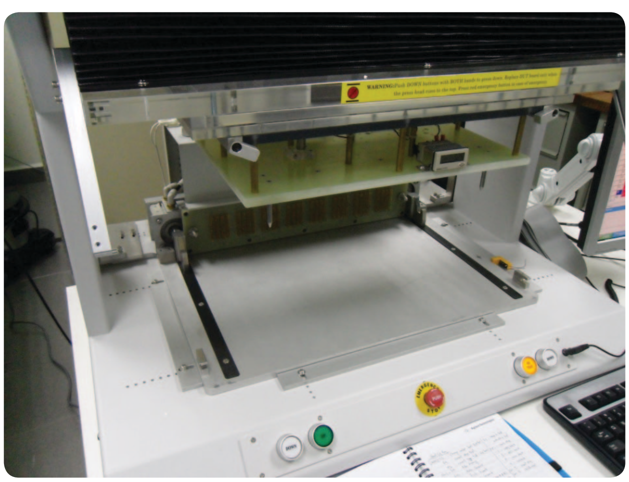

Figure 12. Customized MTS 160 fixture adaptor on i1000D press-down unit

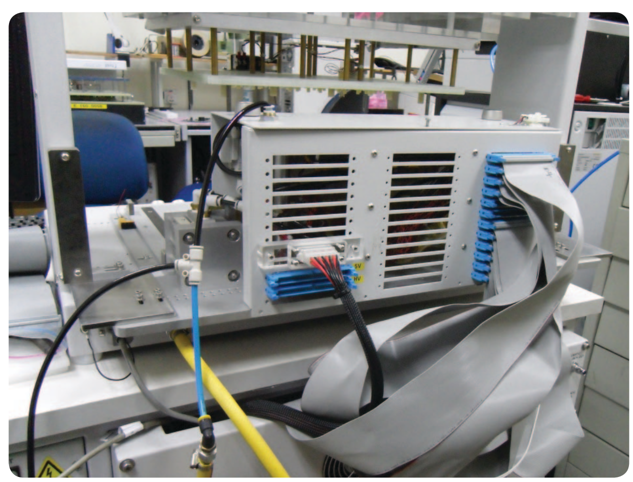

Figure 13. Back view of customized MTS 160 fixture adaptor where 64-pin flat cables are connected

Migration Process

Test resource wiring

The MTS 160 system offers a total of 1,280 resources. This means that it uses a total of 10 blocks. For the purpose of this evaluation, consider a project that does not require the full 10 blocks of test resources. Instead, the test fixture and adaptor are only built to support a total of eight blocks.

Within the eight blocks, only five blocks are assigned for analog test resources. This means the analog node count supported will be 5 x 128 = 640 nodes. Depending on the project requirements, blocks 1 and 5 will be selectively wired in the fixture. However, at the back of the adaptor, all the five blocks will be wired to 10 x 64-pin connectors, which in turn correspond to the 5 x 128-pin analog pin card in the i1000D. The remaining three blocks are reserved for DUT power supply wiring, external relay control wiring and any other functional test module requirements which will be discussed in the next section.

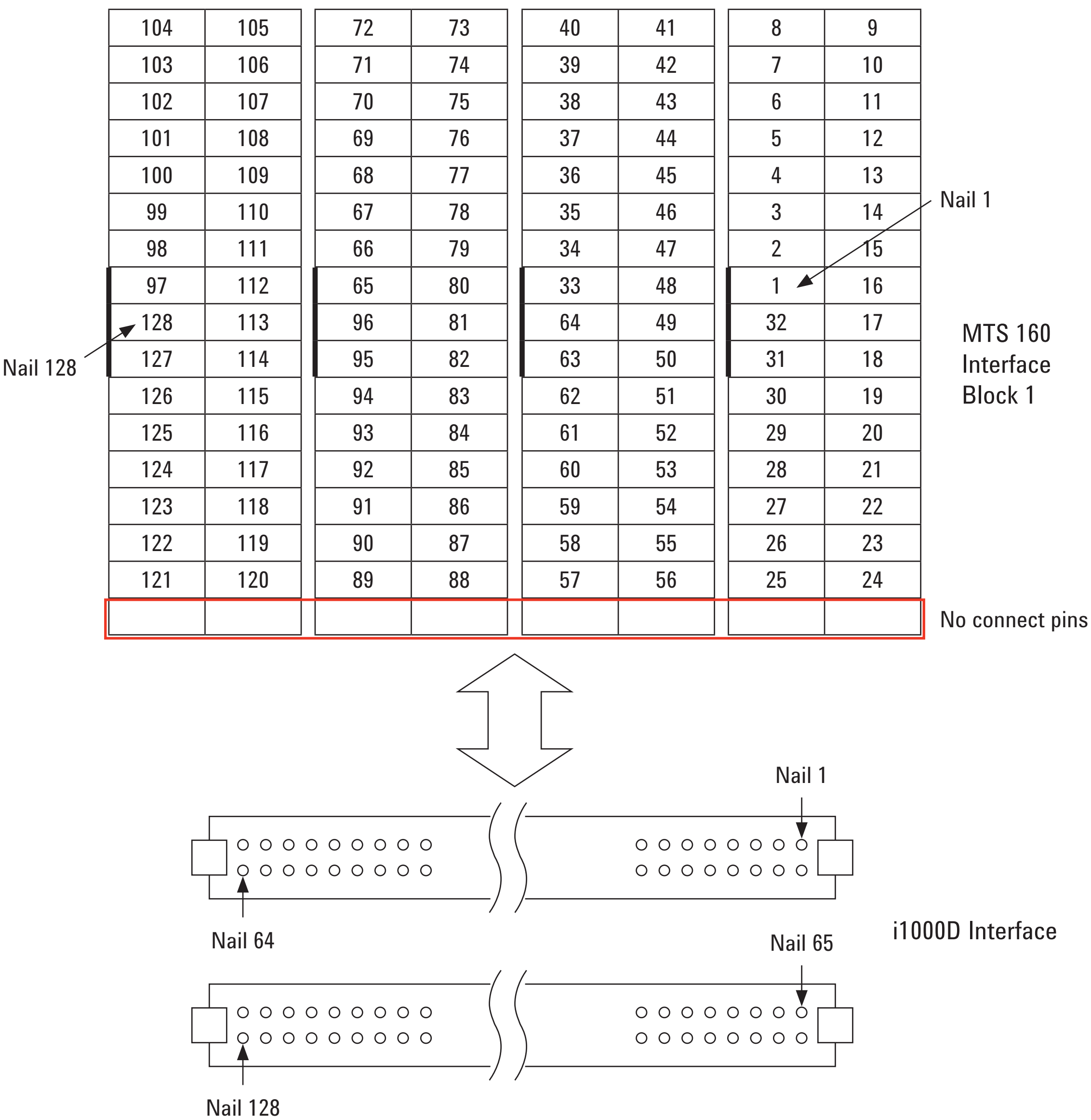

Figure 14. Test resource mapping between MTS 160 and i1000D

Wiring for the test resources is straightforward. Although the pin out position of both test systems is different, there is no multiplexing requirement between the resources. The wiring simply goes from Nail to Nail. For example, Nail 1 on the MTS 160 fixture interface will be wired to Nail 1 of the i1000D fixture interface and so on. The nail numbers start from the middle of the connector in the adaptor and increment around the connector. Note that there are two pins on the connector which are left unconnected as it is a 34-pin connector.

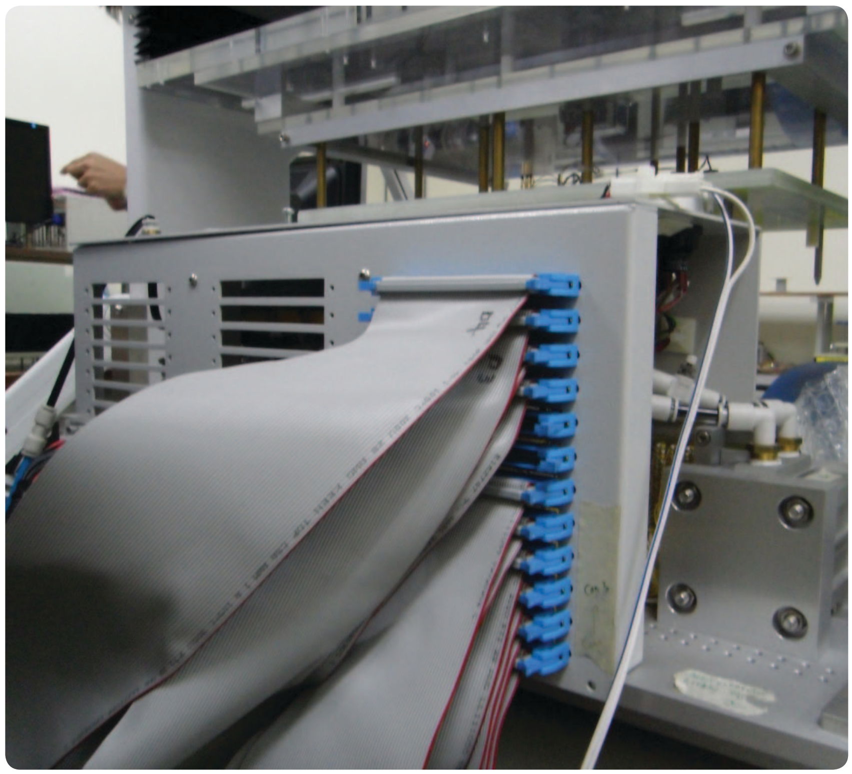

Figure 15. Test resource 64-pin flat cables from i1000D system connected to back of adaptor

Migration Process

Functional test module wiring

The functional test module resources can be assigned to any of the remaining three blocks on the adaptor. There is no standardization as to which block should contain these functional test resources. The functional test module is an optional module on the MTS 160 and its resources are output to 32-pin flat cables similar to those used in the test resource wiring.

Depending on the user preference, these resources may be assigned to any of the block locations as long as all the test fixtures are built to target the assigned block locations when they need to use these functional test resources. For example, if the user decides to have the DUT PS resources assigned to block 6, then all the MTS 160 test fixtures that need to use the DUT PS resources will have to tap the resources from block 6 itself.

Figure 16 shows the resource pin out for the different functional test modules. Each table corresponds to one of the 32-pin connectors within a block. The adaptor needs to wire these resources according to the block and connector location used by the MTS 160 test fixtures.

PSH	
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
S 1+	S 1–
PS1	PS1
PS1	PS1

PSH

Single channel Hi-Power DUT Supply

PS+/–	
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
A-GND	A-GND
S 3+	S 3–
PS3	PS3
PS3	PS3
S 2+	S 2–
PS2	PS2
PS2	PS2

PS+/–

Dual channel DUT Supply

OC	
OC 16	OC 32
OC 15	OC 31
OC 14	OC 30
OC 13	OC 29
OC 12	OC 28
OC 12	OC 27
OC 10	OC 26
OC 9	OC 25
OC 8	OC 24
OC 7	OC 23
OC 6	OC 22
OC 5	OC 21
OC 4	OC 20
OC 3	OC 19
OC 2	OC 18
OC 1	OC 17

Open Collector

32 channel transistor switch to system ground

DCSM	
GND 2	GND 4
DCS 2	DCS 4
DCS 1	DCS 3
GND 1	GND 3
DCM 4+	DCM 4–
A-GND	A-GND
DCM 3+	DCM 3–
A-GND	A-GND
DCM 2+	DCM 2–
A-GND	A-GND
DCM 1+	DCM 1–

DCSM

Quad channel DC voltage source

DS	
	DS 16
	DS 15
	DS 14
	DS 13
	DS 12
	DS 11
	DS 10
	DS 9
	DS 8
	DS 7
	DS 6
	DS 5
	DS 4
	DS 3
	DS 2
	DS 1

Driver/Sensor

16 channel digital driver and sensor

MFTU	
Start 8	Stop 8
Start 7	Stop 7
Start 6	Stop 6
Start 5	Stop 5
Start 4	Stop 4
Start 3	Stop 3
Start 2	Stop 2
Start 1	Stop 1

Non multiplexed Freq/Time unit

8 frequency and time interval measurement channels

FTU	
A-GND	A-GND
Start 8	Stop 8
A-GND	A-GND
Start 7	Stop 7
A-GND	A-GND
Start 6	Stop 6
A-GND	A-GND
Start 5	Stop 5
A-GND	A-GND
Start 4	Stop 4
A-GND	A-GND
Start 3	Stop 3
A-GND	A-GND
Start 2	Stop 2
A-GND	A-GND
Start 1	Stop 1

Freq/Time unit

8 to 1 multiplex frequency and time interval measurement channel

Figure 16. Functional test module resources pin out

Migration Process

The resources for the functional test modules will come from the *Medalist* i1000D. The user can decide what i1000D resource to use for each of the functional test modules. For example, the user may choose to use the N6700 DUT PS unit as a source to supply both the PSH and PS+/– channels, or may decide to use a DUT PS card instead. Table 2 shows a high level mapping of the *Medalist* i1000D resources to the MTS 160 functional test modules.

Table 2. Functional test module resource mapping

MTS 160 functional test modules	*Medalist* i1000D test resources
PSH	Use N6700, DUT PS or HV DUT PS cards. Each unit/card provides up to four programmable channels.
PS+/–	Use N6700, DUT PS or HV DUT PS cards. Each unit/card provides up to four programmable channels.
Open Collector	Use any 32 channels of digital resources with PinDrive mode to drive High and Low. May need level shifter if required voltage is above 5 V.
DCSM	Use any four channels of digital resources with PinDrive mode to drive the required voltage source. May need additional driver circuit if required voltage is above 5 V or current is above 300 mA.
Driver/Sensor	Use any channel of digital resources.
MFTU	Connect to Freq Mux card with buffer boards.
FTU	Connect to Freq Mux card with buffer boards.

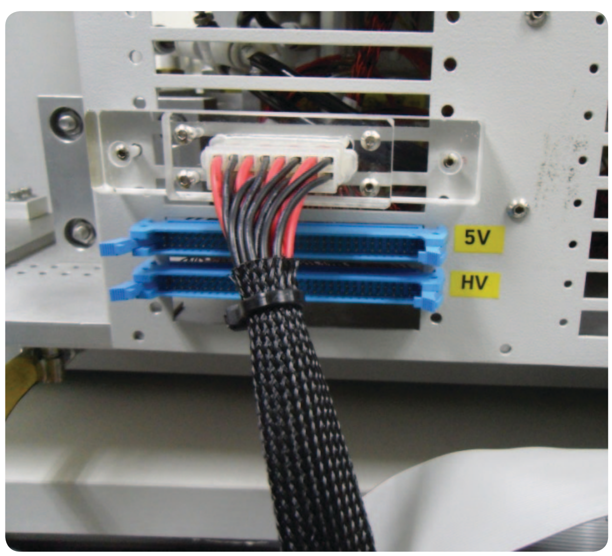

Figure 17. Connections from i1000D providing N6700 DUT PS and HV DUT PS card connections

Migration Process

Software Conversion

Test program conversion is usually a challenge when there is no translator software available to automate the process. In some cases, software conversions may not even be possible when the source files are encrypted. In such cases, the only way to create a *Medalist* i1000D test program which can still use the existing fixture wiring will be to manually enter the test information based on schematics, BOM and fixture nail information. Usually, there will be schematics where the nail numbers are indicated.

The i1000D test program or the ATD file is a simple text-based file which contains all the test information for each device. For a new test fixture development, the ATD file is generated automatically by the *Medalist* i1000D, using the BOMtoATD software. It basically consists of the test nail numbers for each device, their expected values and tolerances.

The BOMtoATD software reads in the BOM, PIN and NAIL files. The PIN and NAIL files are output files from CAD translation software. These files determine the test resource numbers to be wired to the nodes on the board. The test fixtures and programs are then built based on these files.

However, because the intention is to reuse the existing test fixture from the MTS 160, the CAD translation software cannot be allowed to reassign the test nail numbers to the nodes. Instead, the same test nail assignments which were done on the MTS 160 test fixture during its initial development must be used.

If the original PIN and NAIL files from the MTS 160 fixture are available, then simply use the BOMtoATD software to generate the ATD file for the i1000D. The result is a i1000D test program that will use the same test resource wiring of the MTS 160 fixture. However, often users do not keep these files or the files are not updated. In such cases, the ATD file will need to be generated manually.

The usage of BOMtoATD is discussed in the application note "Converting Tescon Point 70 Fixtures and Programs for Use on the *Medalist* i1000D In-Circuit Test System[1]", which describes migration from an MDA to the *Medalist* i1000D.

1. *http://cp.literature.agilent.com/litweb/pdf/5990-5457EN.pdf*

Migration Process

Looking at the MTS 160 test program

The MTS 160 test program is created by the CITE software. The structure is basically a series of VB based source files which are compiled into executables (exe) for runtime. Not all the files are needed for conversion. The information that needs to be extracted from the test program is the device's net list, expected values and test tolerances.

In the test program folder, there is a folder named "TPSRC", containing subfolders named after the DUTs. Within this folder, there are other folders that are named under the DUT's name. Select In each DUT folder there are several source files with the extension ".BAS". These are the source files that will be compiled together to form the runtime executable.

For conversion purposes, look for the file named "<*DUTname*>.BAS". A sample of this source file can be found in the Appendix.

Extract from source file:

```
Sub DRTest()

' -------------------------------------------------------------------
' Testing Diode-Resistor Parallel Combinations
' -------------------------------------------------------------------

   ' APG_NOTE : R136//LD137
   Text "R136//LD137=<1k5_0W25_1%><288><289>//<Super RED><N288><N289>"
   SV "250mV DC2 Delay=1ms MR=1.50K Tol=+-8 A=(288) B=(289)"
   SI "2.53mA DC2 Delay=1ms MV=1.90 Tol=+-30 A=(288) B=(289)"

End Sub
```

The source file is a text-based file that can be opened with any text editor. Information regarding the device test resource assignments, expected value, and tolerance can be extracted from this file. The tests are organized into different subroutines. The example above shows a simple subroutine test for a diode in parallel with a resistor. The code starts with a text message describing the test, followed by two test statements which measure the resistance (MR) and voltage (MV).

```
Text "R136//LD137=<1k5_0W25_1%><288><289>//<Super RED><N288><N289>"

SV "250mV DC2 Delay=1ms MR=1.50K Tol=+-8 A=(288) B=(289)"
SI "2.53mA DC2 Delay=1ms MV=1.90 Tol=+-30 A=(288) B=(289)"
```

Decoding the test statements:

SV = constant Voltage source test
SI = constant Current source test
Delay = delay time
MR = Expected resistance (nominal value)
MV = Expected voltage (nominal value)
Tol = Tolerance +/–
A = Nail number connected to device
B = Nail number connected to device

Migration Process

With an understanding of the test statements, either develop a program to extract the required information and create the i1000D ATD file, or simply enter the information in the i1000D Test Editor interface. Entering all the device information from scratch into the Test Editor interface will be a tedious and time consuming task. Also, because it is done manually, it is prone to mistakes and is only feasible if the board is small.

It is still possible to make use of the BOMtoATD software to generate the ATD file so that it contains all the correct test information like Part(refdes), Type, Values and Tolerances. The only missing piece of information will be the Nail numbers of each of the devices to be tested. This cuts down the ATD generation time and effort significantly as the user only needs to manually enter the nail information of each device.

The following steps summarize the test generation process.

1. Start by obtaining a correct BOM for the DUT.
2. Format the BOM according to the i1000 BOM format requirements.
3. Obtain a PIN file from any other i1000 project or other means.
4. Obtain a NAIL file from any other i1000 project or other means.
5. Launch BOMtoATD and load the formatted BOM, dummy PIN and NAIL files.
6. Convert the files into an ATD file and save it. BOMtoATD will attempt to match the parts in the BOM with the PIN and NAIL files. Obviously, this will fail as the PIN and NAIL files are dummies. The result of BOMtoATD conversion is an ATD file which will have all the parts in the BOM listed, but mostly commented due to the fact that they were not found in the PIN file. However, the key point is that all the steps will already have the device name, value and tolerances included. Only the Nail information is missing.
7. Load the converted ATD file into the *Medalist* i1000D software.
8. Open the Test Editor interface. Most of the test steps will be skipped.
9. Manually un-skip all the test steps.
10. Refer to the MTS 160 test file and fill in the Nail numbers for each of the devices in the Test Editor interface. For those devices that do not have nail access, skip the step by pressing F2.
11. Once completed, the test program is ready for debug. During debug, it is helpful to re-check the Nail numbers in case errors were made during the manual entry.

Conclusion

In conclusion, the migration of an old MTS 160 fixture and program to a new *Medalist* i1000D is definitely possible. Though the process may not be as straightforward as some other conversions, it is an achievable task.

The key to a successful conversion is the accuracy of the adaptor being built. This plays an important part in getting the right test resources to the right probes on the fixture. Wrong wiring will simply mean a mismatch of test resources. It is important for all parties involved in the conversion project to define and agree on the requirements before the adaptor is built. Users must follow the design of the adaptor when they need to build new fixtures. Though it is recommended that an actual i1000D fixture be built for any new project, some users may choose to continue building fixtures based on the MTS 160 design so that they can be used in both the i1000D and the MTS 160 system. In such cases, the allocation of test resources needs to match between the MTS 160 and the adaptor.

With the adaptor built and the original test fixtures running on the *Medalist* i1000D, users can then decide to take a step further and enhance their test coverage by utilizing the more advanced test features that are available on the i1000D. One good example is the use of the VTEP technology to enable effective test coverage on difficult IC packages. Other usage may be to move the offline programming operations for memory devices onto the i1000D so as to shorten the process flow and reduce handling requirements.

More complex functional testing may now be conducted on the test station using the *Medalist* i1000D PinDrive test mode. This feature allows the user to selectively drive any of its digital channels to provide an easy way to implement functional tests on the i1000D. The digital channels can be used as inputs to drive certain patterns to the controller on the DUT to initiate a functional test sequence, then have the i1000D measure and check the responses.

Appendix

Sample of PIN File

E9900 eM-Test Expert (R)

Part Pins List 0/1100 Selected Parts 20-Mar-2007 10:35

INCH units

Part Pin	Name	T/B X	Y	Layer	Net	Nail(s)
Part C1		(T)				
1	1	0.5124	4.3500	1	02_23_64	453
2	2	0.4376	4.3500	1	SERIES_02_23_64	533
Part C2		(T)				
1	1	–0.0250	8.7750	1	DCOM	1
2	2	–0.1250	8.7750	1	VCC	2
Part R1		(T)				
1	1	0.5124	4.2500	1	02_23_64	453
2	2	0.4376	4.2500	1	VCC	2
Part R2		(T)				
1	1	0.4376	4.1500	1	DCOM	1
2	2	0.5124	4.1500	1	02_23_64	453
Part J8		(T)				
1	1	2.5250	7.9500	1	DCOM	1
2	2	2.4750	7.9500	1	02_14_64	622
3	3	2.4250	7.9500	1	02_22_64	425
4	4	2.3750	7.9500	1	N$152684	308
5	5	2.3250	7.9500	1	02_20_64	460
6	6	2.2750	7.9500	1	02_17_64	534
7	7	2.2250	7.9500	1	DCOM	1
8	8	1.9750	7.9500	1	VCC	2
9	9	1.9250	7.9500	1	VCC	2
10	10	1.8750	7.9500	1	VCC	2
11	11	1.8250	7.9500	1	DCOM	1
12	12	1.7750	7.9500	1	DCOM	1
13	13	1.7250	7.9500	1	DCOM	1
14	14	1.6750	7.9500	1	VCC	2
15	15	1.6250	7.9500	1	VCC	2
16	16	1.5750	7.9500	1	VCC	2
17	17	1.5250	7.9500	1	DCOM	1
18	18	1.4750	7.9500	1	02_15_64	623
19	19	1.4250	7.9500	1	DCOM	1
20	20	1.3750	7.9500	1	VCC	2
21	21	1.3250	7.9500	1	VCC	2
22	22	1.2750	7.9500	1	VCC	2

Appendix

Sample of NAIL File

E9900 FABMASTER (R)
Test Fixture Nails 884/5682 Selected Drills 5-Mar-2007 13:08
884 Nails, 898 Nets INCH units

Nail	X	Y	Type	Grid	T/B	Net	Net Name	Virtual Pin/Via
$1	1.0713	3.5229	2	8D	(B)	#873	DCOM	PIN J3.242
$1	–0.1910	7.5364	2	9G	(B)	#873	DCOM	PIN J4.11
$1	2.9500	–0.0500	1	7A	(B)	#873	DCOM	PIN TP_1038.1
$1	8.2500	11.5500	1	3J	(B)	#873	DCOM	PIN TP_17.1
$1	2.7500	11.5500	1	7J	(B)	#873	DCOM	PIN TP_72.1
$1	7.8500	–0.0500	1	3A	(B)	#873	DCOM	PIN TP_989.1
$1	6.0000	5.0000	1	5E	(B)	#873	DCOM	PIN JMP10.3
$1	10.7000	3.3250	1	1D	(B)	#873	DCOM	PIN JMP9.3
$2	5.9406	4.7248	2	5E	(B)	#1	VCC	PIN J10.2
$2	1.3343	4.5004	2	8E	(B)	#1	VCC	PIN J10.235
$2	2.8304	3.6804	2	7D	(B)	#1	VCC	PIN J3.197
$2	–0.0335	7.3002	2	9G	(B)	#1	VCC	PIN J4.30
$2	6.2500	11.5500	1	4J	(B)	#1	VCC	PIN TP_37.1
$2	9.8500	2.4500	1	2C	(B)	#1	VCC	PIN TP_529.1
$3	1.1500	11.0500	1	8J	(B)	#117	02_05_164	PIN TP_176.1
$4	1.2500	11.0500	1	8J	(B)	#129	02_05_64	PIN TP_175.1
$5	1.3500	11.0500	1	8J	(B)	#85	02_04_164	PIN TP_174.1
$6	1.4500	11.0500	1	8J	(B)	#97	02_04_64	PIN TP_173.1
$7	1.5500	11.0500	1	8J	(B)	#116	02_05_163	PIN TP_172.1
$8	1.6500	11.0500	1	8J	(B)	#128	02_05_63	PIN TP_171.1
$9	1.7500	11.0500	1	8J	(B)	#84	02_04_163	PIN TP_170.1
$10	1.8500	11.0500	1	8J	(B)	#96	02_04_63	PIN TP_169.1
$11	1.9500	11.0500	1	8J	(B)	#115	02_05_162	PIN TP_168.1
$12	2.0500	11.0500	1	8J	(B)	#127	02_05_62	PIN TP_167.1
$13	2.1500	11.0500	1	8J	(B)	#83	02_04_162	PIN TP_166.1
$14	2.2500	11.0500	1	8J	(B)	#95	02_04_62	PIN TP_165.1
$15	2.3500	11.0500	1	7J	(B)	#114	02_05_161	PIN TP_164.1
$16	2.4500	11.0500	1	7J	(B)	#126	02_05_61	PIN TP_163.1
$17	2.5500	11.0500	1	7J	(B)	#82	02_04_161	PIN TP_162.1
$18	2.6500	11.0500	1	7J	(B)	#94	02_04_61	PIN TP_161.1
$19	1.1500	11.5500	1	8J	(B)	#54	02_03_164	PIN TP_88.1
$20	1.2500	11.5500	1	8J	(B)	#65	02_03_64	PIN TP_87.1
$21	1.3500	11.5500	1	8J	(B)	#23	02_02_164	PIN TP_86.1
$22	1.4500	11.5500	1	8J	(B)	#34	02_02_64	PIN TP_85.1
$23	1.5500	11.5500	1	8J	(B)	#53	02_03_163	PIN TP_84.1
$24	1.6500	11.5500	1	8J	(B)	#64	02_03_63	PIN TP_83.1
$25	1.7500	11.5500	1	8J	(B)	#22	02_02_163	PIN TP_82.1
$26	1.8500	11.5500	1	8J	(B)	#33	02_02_63	PIN TP_81.1
$27	1.9500	11.5500	1	8J	(B)	#52	02_03_162	PIN TP_80.1
$28	2.0500	11.5500	1	8J	(B)	#63	02_03_62	PIN TP_79.1
$29	2.1500	11.5500	1	8J	(B)	#21	02_02_162	PIN TP_78.1
$30	2.2500	11.5500	1	8J	(B)	#32	02_02_62	PIN TP_77.1
$31	2.3500	11.5500	1	7J	(B)	#51	02_03_161	PIN TP_76.1
$32	2.4500	11.5500	1	7J	(B)	#62	02_03_61	PIN TP_75.1
$33	2.5500	11.5500	1	7J	(B)	#20	02_02_161	PIN TP_74.1
$34	2.6500	11.5500	1	7J	(B)	#31	02_02_61	PIN TP_73.1
$35	3.5500	11.0500	1	7J	(B)	#113	02_05_144	PIN TP_152.1
$36	3.6500	11.0500	1	6J	(B)	#125	02_05_44	PIN TP_151.1
$37	3.7500	11.0500	1	6J	(B)	#81	02_04_144	PIN TP_150.1
$38	3.8500	11.0500	1	6J	(B)	#93	02_04_44	PIN TP_149.1
$39	3.9500	11.0500	1	6J	(B)	#112	02_05_143	PIN TP_148.1
$40	4.0500	11.0500	1	6J	(B)	#124	02_05_43	PIN TP_147.1
$41	4.1500	11.0500	1	6J	(B)	#80	02_04_143	PIN TP_146.1
$42	4.2500	11.0500	1	6J	(B)	#92	02_04_43	PIN TP_145.1
$43	4.3500	11.0500	1	6J	(B)	#111	02_05_142	PIN TP_144.1
$44	4.4500	11.0500	1	6J	(B)	#123	02_05_42	PIN TP_143.1
$45	4.5500	11.0500	1	6J	(B)	#79	02_04_142	PIN TP_142.1
$46	4.6500	11.0500	1	6J	(B)	#91	02_04_42	PIN TP_141.1
$47	4.7500	11.0500	1	6J	(B)	#110	02_05_141	PIN TP_140.1
$48	4.8500	11.0500	1	6J	(B)	#122	02_05_41	PIN TP_139.1
$49	4.9500	11.0500	1	5J	(B)	#78	02_04_141	PIN TP_138.1
$50	5.0500	11.0500	1	5J	(B)	#90	02_04_41	PIN TP_137.1
$51	3.5500	11.5500	1	7J	(B)	#50	02_03_144	PIN TP_64.1

Appendix

Sample of Formatted BOM for *Medalist* i1000

C6003;C;0.47uF;10%;10%;;0.47uF;
C6006;C;470pF;10%;10%;;470pF;
C6007;C;220pF;10%;10%;;220pF;
C6010;C;470pF;10%;10%;;470pF;
C6011;C;220pF;10%;10%;;220pF;
C6018;C;0.22uF;10%;10%;;0.22uF;
CN6000;J;;;;;3Pin connector;
CN6150;J;;;;;13Pin connector;
D6000;Q;;;;;D10XB60S;
D6001;Q;;;;;MA2J1110GLS0;
D6003;Q;;;;;MA4J1130GLS0;
F6001;JP;1JP;F;F;;FUSE (H.B.C.);
FB6100;JP;1JP;F;F;;"INDUCTOR, FERRITE BEAD";
FB6101;JP;1JP;F;F;;"INDUCTOR, FERRITE BEAD";
FB6600;L;0.45UH;10%;10%;;0.45UH;
FB6601;L;0.45UH;10%;10%;;0.45UH;
IC6101;IC;;;;;MM1431CURE;
IC6102;IC;;;;;CXD9969P;
IC6200;IC;;;;;MIP2H2;
IC6251;IC;;;;;MM1530CURE;
IC6300;IC;;;;;MM3313AFFE;
JR605;JP;1JP;F;F;;3216;
JR606;JP;1JP;F;F;;"CONDUCTOR, CHIP";
L6000;JP;1JP;F;F;;LINE FILTER COIL;
L6151;L;4.7UH;10%;10%;;4.7UH;
L6501;L;165UH;10%;10%;;165UH;
L6550;L;260UH;10%;10%;;260UH;
L6600;L;100UH;10%;10%;;100UH;
Q6100;Q;;;;;TK8A50D;
Q6101;Q;;;;;TK8A50D;
Q6300;Q;;;;;2SA1364-T111-1DE;
Q6302;Q;;;;;2SC3052EF-T1-LEF;
Q6305;Q;;;;;ISA1235AC1TP-1EF;
Q6400;Q;;;;;RT1N14BC-TP-1;
R6010;R;1.0M;10%;10%;;1.0M;
R6011;R;1.0M;10%;10%;;1.0M;
R6015;R;560K;10%;10%;;560K;
R6016;R;6.8;10%;10%;;6.8;
R6017;R;100K;10%;10%;;100K;
R6018;R;470K;10%;10%;;470K;
R6019;R;560K;10%;10%;;560K;
R6100;R;150K;10%;10%;;150K;
R6102;R;100;10%;10%;;100;
R6103;R;12K;10%;10%;;12K;
R6105;R;2M;10%;10%;;2M;
R6106;R;2M;10%;10%;;2M;

Appendix

MTS 160 Edge Connectors Resource Allocation for Mux Card 1 to 5

Conn 4 Mux 5

nc	nc
633	632
634	631
635	630
636	629
637	628
638	627
639	626
640	625
609	624
610	623
611	622
612	621
613	620
614	619
615	618
616	617

Conn 4 Mux 4

nc	nc
505	504
506	503
507	502
508	501
509	500
510	499
511	498
512	497
481	496
482	495
483	494
484	493
485	492
486	491
487	490
488	489

Conn 4 Mux 3

nc	nc
377	376
378	375
379	374
380	373
381	372
382	371
383	370
384	369
353	368
354	367
355	366
356	365
357	364
358	363
359	362
360	361

Conn 4 Mux 2

nc	nc
249	248
250	247
251	246
252	245
253	244
254	243
255	242
256	241
225	240
226	239
227	238
228	237
229	236
230	235
231	234
232	233

Conn 4 Mux 1

nc	nc
121	120
122	119
123	118
124	117
125	116
126	115
127	114
128	113
97	112
98	111
99	110
100	109
101	108
102	107
103	106
104	105

Conn 3 Mux 5

nc	nc
601	600
602	599
603	598
604	597
605	596
606	595
607	594
608	593
577	592
578	591
579	590
580	589
581	588
582	587
583	586
584	585

Conn 3 Mux 4

nc	nc
473	472
474	471
475	470
476	469
477	468
478	467
479	466
480	465
449	464
450	463
451	462
452	461
453	460
454	459
455	458
456	457

Conn 3 Mux 3

nc	nc
345	344
346	343
347	342
348	341
349	340
350	339
351	338
352	337
321	336
322	335
323	334
324	333
325	332
326	331
327	330
328	329

Conn 3 Mux 2

nc	nc
217	216
218	215
219	214
220	213
221	212
222	211
223	210
224	209
193	208
194	207
195	206
196	205
197	204
198	203
199	202
200	201

Conn 3 Mux 1

nc	nc
89	88
90	87
91	86
92	85
93	84
94	83
95	82
96	81
65	80
66	79
67	78
68	77
69	76
70	75
71	74
72	73

Conn 2 Mux 5

nc	nc
569	568
570	567
571	566
572	565
573	564
574	563
575	562
576	561
545	560
546	559
547	558
548	557
549	556
550	555
551	554
552	553

Conn 2 Mux 4

nc	nc
441	440
442	439
443	438
444	437
445	436
446	435
447	434
448	433
417	432
418	431
419	430
420	429
421	428
422	427
423	426
424	425

Conn 2 Mux 3

nc	nc
313	312
314	311
315	310
316	309
317	308
318	307
319	306
320	305
289	304
290	303
291	302
292	301
293	300
294	299
295	298
296	297

Conn 2 Mux 2

nc	nc
185	184
186	183
187	182
188	181
189	180
190	179
191	178
192	177
161	176
162	175
163	174
164	173
165	172
166	171
167	170
168	169

Conn 2 Mux 1

nc	nc
57	56
58	55
59	54
60	53
61	52
62	51
63	50
64	49
33	48
34	47
35	46
36	45
37	44
38	43
39	42
40	41

Conn 1 Mux 5

nc	nc
537	536
538	535
539	534
540	533
541	532
542	531
543	530
544	529
513	528
514	527
515	526
516	525
517	524
518	523
519	522
520	521

Conn 1 Mux 4

nc	nc
409	408
410	407
411	406
412	405
413	404
414	403
415	402
416	401
385	400
386	399
387	398
388	397
389	396
390	395
391	394
392	393

Conn 1 Mux 3

nc	nc
281	280
282	279
283	278
284	277
285	276
286	275
287	274
288	273
257	272
258	271
259	270
260	269
261	268
262	267
263	266
264	265

Conn 1 Mux 2

nc	nc
153	152
154	151
155	150
156	149
157	148
158	147
159	146
160	145
129	144
130	143
131	142
132	141
133	140
134	139
135	138
136	137

Conn 1 Mux 1

nc	nc
25	24
26	23
27	22
28	21
29	20
30	19
31	18
32	17
1	16
2	15
3	14
4	13
5	12
6	11
7	10
8	9

Appendix

MTS 160 Edge Connectors Resource Allocation for Mux Card 6 to 10

Conn 4 Mux 10

nc	nc
1273	1272
1274	1271
1275	1270
1276	1269
1277	1268
1278	1267
1279	1266
1280	1265
1249	1264
1250	1263
1251	1262
1252	1261
1253	1260
1254	1259
1255	1258
1256	1257

Conn 4 Mux 9

nc	nc
1145	1144
1146	1143
1147	1142
1148	1141
1149	1140
1150	1139
1151	1138
1152	1137
1121	1136
1122	1135
1123	1134
1124	1133
1125	1132
1126	1131
1127	1130
1128	1129

Conn 4 Mux 8

nc	nc
1017	1016
1018	1015
1019	1014
1020	1013
1021	1012
1022	1011
1023	1010
1024	1009
993	1008
994	1007
995	1006
996	1005
997	1004
998	1003
999	1002
1000	1001

Conn 4 Mux 7

nc	nc
889	888
890	887
891	886
892	885
893	884
894	883
895	882
896	881
865	880
866	879
867	878
868	877
869	876
870	875
871	874
872	873

Conn 4 Mux 6

nc	nc
761	760
762	759
763	758
764	757
765	756
766	755
767	754
768	753
737	752
738	751
739	750
740	749
741	748
742	747
743	746
744	745

Conn 3 Mux 10

nc	nc
1241	1240
1242	1239
1243	1238
1244	1237
1245	1236
1246	1235
1247	1234
1248	1233
1217	1232
1218	1231
1219	1230
1220	1229
1221	1228
1222	1227
1223	1226
1224	1225

Conn 3 Mux 9

nc	nc
1113	1112
1114	1111
1115	1110
1116	1109
1117	1108
1118	1107
1119	1106
1120	1105
1089	1104
1090	1103
1091	1102
1092	1101
1093	1100
1094	1099
1095	1098
1096	1097

Conn 3 Mux 8

nc	nc
985	984
986	983
987	982
988	981
989	980
990	979
991	978
992	977
961	976
962	975
963	974
964	973
965	972
966	971
967	970
968	969

Conn 3 Mux 7

nc	nc
857	856
858	855
859	854
860	853
861	852
862	851
863	850
864	849
833	848
834	847
835	846
836	845
837	844
838	843
839	842
840	841

Conn 3 Mux 6

nc	nc
729	728
730	727
731	726
732	725
733	724
734	723
735	722
736	721
705	720
706	719
707	718
708	717
709	716
710	715
711	714
712	713

Conn 2 Mux 10

nc	nc
1209	1208
1210	1207
1211	1206
1212	1205
1213	1204
1214	1203
1215	1202
1216	1201
1185	1200
1186	1199
1187	1198
1188	1197
1189	1196
1190	1195
1191	1194
1192	1193

Conn 2 Mux 9

nc	nc
1081	1080
1082	1079
1083	1078
1084	1077
1085	1076
1086	1075
1087	1074
1088	1073
1057	1072
1058	1071
1059	1070
1060	1069
1061	1068
1062	1067
1063	1066
1064	1065

Conn 2 Mux 8

nc	nc
953	952
954	951
955	950
956	949
957	948
958	947
959	946
960	945
929	944
930	943
931	942
932	941
933	940
934	939
935	938
936	937

Conn 2 Mux 7

nc	nc
825	824
826	823
827	822
828	821
829	820
830	819
831	818
832	817
801	816
802	815
803	814
804	813
805	812
806	811
807	810
808	809

Conn 2 Mux 6

nc	nc
697	696
698	695
699	694
700	693
701	692
702	691
703	690
704	689
673	688
674	687
675	686
676	685
677	684
678	683
679	682
680	681

Conn 1 Mux 10

nc	nc
1177	1176
1178	1175
1179	1174
1180	1173
1181	1172
1182	1171
1183	1170
1184	1169
1153	1168
1154	1167
1155	1166
1156	1165
1157	1164
1158	1163
1159	1162
1160	1161

Conn 1 Mux 9

nc	nc
1049	1048
1050	1047
1051	1046
1052	1045
1053	1044
1054	1043
1055	1042
1056	1041
1025	1040
1026	1039
1027	1038
1028	1037
1029	1036
1030	1035
1031	1034
1032	1033

Conn 1 Mux 8

nc	nc
921	920
922	919
923	918
924	917
925	916
926	915
927	914
928	913
897	912
898	911
899	910
900	909
901	908
902	907
903	906
904	905

Conn 1 Mux 7

nc	nc
793	792
794	791
795	790
796	789
797	788
798	787
799	786
800	785
769	784
770	783
771	782
772	781
773	780
774	779
775	778
776	777

Conn 1 Mux 6

nc	nc
665	664
666	663
667	662
668	661
669	660
670	659
671	658
672	657
641	656
642	655
643	654
644	653
645	652
646	651
647	650
648	649

Appendix

Sample of <DUTname>.BAS Source File

Note: The following file has been edited to reduce the number of lines. The format of the file remains unchanged.

```
Sub DRTest()
' ------------------------------------------------------------------
' Testing Diode-Resistor Parallel Combinations
' ------------------------------------------------------------------
   ' APG_NOTE : R136//LD137
   Text "R136//LD137=<1k5_0W25_1%><288><289>//<Super RED><N288><N289>"
   SV "250mV DC2 Delay=1ms MR=1.50K Tol=+-8 A=(288) B=(289)"
   SI "2.53mA DC2 Delay=1ms MV=1.90 Tol=+-30 A=(288) B=(289)"
End Sub

Sub PinCheckTest()
' ------------------------------------------------------------------
' PinCheck Test
' ------------------------------------------------------------------
   ' APG_NOTE : DEFPINLIST
   Def_PinList "PL01 = (1,136-174,177-190,192,193,195-197,201-204,206-297,299-301)"
   Def_PinList "PL02 = (303,306,308-320,324,325,330-335,338,339,345-350,352-354)"
   Def_PinList "PL03 = (358,360,363,367-374,377,378,381,382,384-388,390,397,399)"
   Def_PinList "PL04 = (401,402,404-410,419,421-426,428-431,434,441-450)"
   ' APG_NOTE : PINCHECK
   Text "PinCheck"
   PinCheck "(PL01,PL02,PL03,PL04,208,202)"
End Sub

Sub RCTest()
   Message$ = "Resistor Capacitor Test"
   ' APG_NOTE : R59//C55
   Text "R59//C55=<10k_0W1_5%><N226><N266>//<100n_50V_20><226><266>"
   SV "250mV DC2 Delay=1ms MR=10K Tol=+-15 A=(266) B=(226) C=(433) D=(0)"
   SV "250mV AC=1000.000 Delay=1mS MC=100nF Tol=+-31 MR=10.0000KOhm Tol=* A=(266) B=(226) C=(433)"
End Sub

Sub DischargeTest()
' ------------------------------------------------------------------
' Discharge Large Capacitors
' ------------------------------------------------------------------
    ' APG_NOTE : C5//C6//C4
   Text "C5//C6//C4=<68n_50V_20%><N206><N433>//<10n_50V_20%><N206><N433>//<470u_25V_+50-20%_radial><N206><N433>"
   Discharge "(206,433)"
End Sub

Sub ContinuityTest()
' ------------------------------------------------------------------
' Continuity (Connectors) Test
' ------------------------------------------------------------------
    ' APG_NOTE : L36 <Do Not Debug>
   Text "L36=<A2C00020459>"
   CONT "(428,208) RMAX100"
End Sub

Sub ShortTest()
' ------------------------------------------------------------------
' Short Test
' ------------------------------------------------------------------
  ' APG_NOTE :
   Text "Short test for all nets"
   OpenTest "(101-512#138,175,176,195,203,205-206,208,210-211,213-214,220,227,246,257,261,286,315,364-366,372,374-376,380,383,
389-393,428,431-434,443)RMAX10"
   EndMsg
End Sub
```

Appendix

Sample of <DUTname>.BAS Source File *(continued)*

```
Sub DiodeTest()
' -----------------------------------------------------------------
' Diode Test
' -----------------------------------------------------------------
    ' APG_NOTE : D2
   Text "D2/=<S1J><N205><N206>"
   SI "5mA DC=150us VMax=2V Delay=1ms MV=750m Tol=+-30 A=(205) B=(206)"
   Text "D2/R=<S1J><N205><N206>"
   SI "5mA DC=150us VMax=2 V Delay=1mS MV=2V Tol=+-30 A=(206) B=(205)"
End Sub

Sub IC21Test()
' -----------------------------------------------------------------
' IC21 Test
' -----------------------------------------------------------------
   ' APG_NOTE : IC21
   Text "IC21 Pin_1=<N433><N252>"
   SI "5mA DC=150us Vmax=2V Delay=0.60ms MV=750m Tol=+-30   A=(433) B=(252)"
   ' APG_NOTE : IC21
   Text "IC21 Pin_2=<N433><N256>"
   SI "5mA DC=150us Vmax=2V Delay=0.60ms MV=750m Tol=+-30   A=(433) B=(256)"
End Sub

Sub LEDTest()
' -----------------------------------------------------------------
' LED Test
' -----------------------------------------------------------------
   ' APG_NOTE : LD17
   Text "LD17/F=<Pure green><N232><N266>"
   SI "5mA DC=150us VMax=3V Delay=1mS MV=1.9V Tol=+-20 A=(232) B=(266)"
   Text "LD17/R=<Pure green><N232><N266>"
   SI "5mA DC=150us VMax=3V Delay=1mS MV=3.0V Tol=+-20 A=(266) B=(232)"
End Sub

Sub ZenerDiodeTest()
' -----------------------------------------------------------------
' Zener Diode Test
' -----------------------------------------------------------------
   ' APG_NOTE : Z102
   Text "Z102/F=<ZD_27V><N433><N278>"
   SI "5mA DC=10.000 Delay=10mS MV=750mV Tol=+-30 A=(433) B=(278)"
End Sub

Sub TransistorTest()
' -----------------------------------------------------------------
' Transistor Test
' -----------------------------------------------------------------
   ' APG_NOTE : T94
   Text "T94/BC=<BCR141><N260><N207><N433>"
  ' SI "10mA DC2 Delay=1ms MV=750m Tol=+-30 A=(207) B=(260)"
   SV "250mV DC=80.000 Delay=80mS MR=40KOhm Tol=+-30 A=(207) B=(260)"
   Text "T94/BE=<BCR141><N260><N207><N433>"
  ' SI "10mA DC2 Delay=1ms MV=750m Tol=+-30 A=(207) B=(433)"
   SV "250mV DC=20.000 Delay=20mS MR=40KOhm Tol=+-30 A=(207) B=(433)"
End Sub
```

Appendix

Sample of <DUTname>.BAS Source File *(continued)*

```
Sub ResistorTest()
' -------------------------------------------------------------------
' Resistor Test
' -------------------------------------------------------------------
   ' APG_NOTE : LS104
   Text "LS104=<Loud_Speaker 5%><N206><N278>"
   SV "250mV DC=20.000 Delay=20mS MR=100Ohm Tol=+-15 A=(206) B=(278)"
   ' APG_NOTE : R8
   Text "R8=<10k_0W1_5%><N208><N204>"
   SV "250mV DC2 Delay=1ms MR=10K Tol=+-15 A=(208) B=(204)"
End Sub

Sub CapacitorTest()
' -------------------------------------------------------------------
' Capacitor Test
' -------------------------------------------------------------------
   ' APG_NOTE : C13
   Text "C13=<1n_50V_10%><N433><N204>"
   SV "250mV AC=1000.000 Delay=20mS MC=1nF Tol=+-30 A=(433) B=(204) C=(208,206) D=(278)"
   ' APG_NOTE : C14
   Text "C14=<68n_50V_20%><N209><N433>"
   SV "250mV AC1 Delay=1ms MC=68n Tol=+-30 A=(433) B=(209)"
End Sub

Sub ElecCapacitorTest()
' -------------------------------------------------------------------
' Electrolytic Capacitor Test
' -------------------------------------------------------------------
    ' APG_NOTE : C4//C5//C6
   Text "C4//C5//C6=<68n_50V_20%><N206><N433>//<10n_50V_20%><N206><N433>//<470u_25V_+50-20%_radial><N206><N433>"
   SI "5mA DC=10.000 Delay=1mS ME=470.0800uF Tol=+50-20 A=(206) B=(433) C=(319,334)"
End Sub
```

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