Addressing the Challenges of High-Speed Digital I/O for Aerospace Defense Applications

Application note

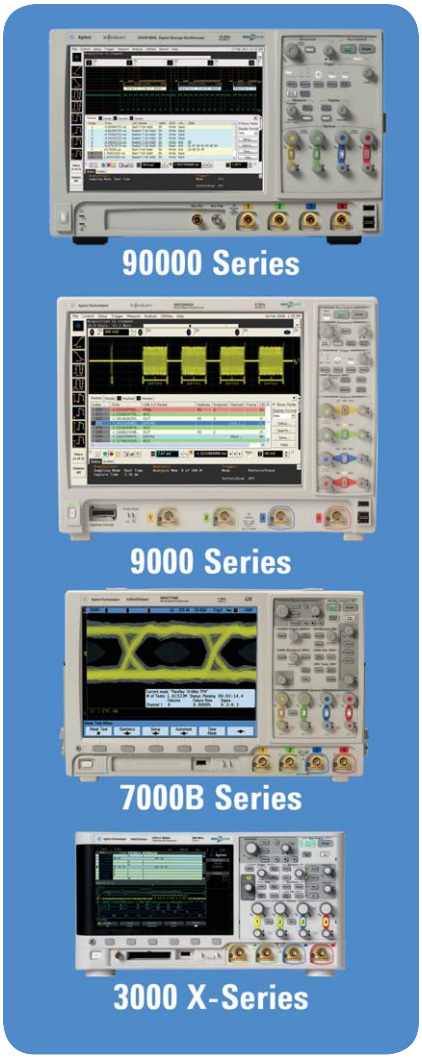
Introduction

The evolution to reconfigurable multipurpose radar, EW, and military communications systems to address tomorrow's emerging threats is driving new system-level architectural and I/O requirements. In addition, supporting an increasingly networked infrastructure with high data throughput and low latency is becoming key for network-centric applications–all of which must be deployed faster and at a lower cost with today's tightening budgets.

These trends are driving implementation changes from the system level down to digital components, including the digital interfaces that are used. Today's systems increasingly rely on reconfigurable hardware such as field programmable gate arrays (FPGAs), digital signal processors (DSPs), and general-purpose processors (GPPs). High-speed I/O is needed to support high data rates between these devices, as well as memory, storage, and graphic processors/displays.

Commercial-off-the-shelf (COTS) technologies used today by the computer industry can offer performance and cost benefits for increased data throughput capacity to support these demands. However, migration to these technologies also introduces significant design and test challenges, especially as COTS technologies evolve to multi-Gb/s data rates. This application note discusses physical layer and protocol layer test challenges for COTS technologies, as well as established commercial test solutions that can help to mitigate risks in migrating to these technologies for aerospace/defense applications.

In addition, fiber-based technologies offer benefits for high data throughput, reduced weight and volume, and lower susceptibility to EMI and interference. These benefits can make fiber attractive for aircraft and ship applications, as well as digital beam-forming antenna array applications where data demands increase rapidly with increasing array sizes and the larger numbers of transmit/receive (T/R) modules. This application note will also discuss test challenges and commercial test solutions for fiber digital I/O technologies to help mitigate risk in upgrading to fiber-based technologies.



Agilent Technologies

Test Challenges of High-Speed Digital I/O Technologies

The need for higher data throughput and lower latency introduces a number of digital I/O challenges to consider, both at the physical layer and at the protocol layer. First, we will look at physical layer and protocol layer challenges, followed by technology-specific considerations for some of the COTS technologies, both copper and fiber, which may be of interest for defense applications.

Appendix A shows a comprehensive list of COTS digital I/O technologies and test solutions being used today for commercial applications, which may also be of interest for defense applications. These interfaces range from 1 Mb/s to multi-Gb/s for various applications, including microprocessors, FPGAs, memory, graphics/display, and storage.

While a detailed exploration of each of these technologies is beyond the scope of this application note, we will discuss some key technologies and their physical layer and protocol layer testing challenges. This application note provides a brief overview of a subset of the COTS digital I/O technologies listed in Appendix A.

Please contact Agilent Technologies for more in-depth application and solution information for any technologies of interest listed in Appendix A.

Physical Layer Test Challenges

Digital signals are subject to analog parametric issues when they are implemented into real systems with PC board traces, connectors, and cables. Impedance mismatch, noise, and jitter impact the physical layer performance and the signal integrity of the bus. At these high data rates, bit unit intervals become so small that system noise, crosstalk from adjacent electrical signals, or even electromagnetic interference can impair the signal integrity. In addition, channel skin effects and a lossy signal path can further degrade signal integrity, which can degrade the bit error rate (BER) performance at the device receiver.

These impairments can negatively impact the reliability and robustness of the digital I/O link performance, which is critical for defense applications. Oscilloscopes are essential to characterizing and validating digital I/O performance, and to the integration of these COTS technologies. Oscilloscopes mitigate design and implementation risks in deploying these technologies. However, there are several key factors you should consider.

Sufficient oscilloscope bandwidth is important for capturing adequate signal content from the digital waveform (for example, the 5th harmonic on a waveform with fast edges) to accurately measure rise and fall times. Without sufficient bandwidth, the measured test signal might appear to be distorted relative to the actual signal.

In addition to bandwidth, you should also consider the oscilloscope's noise performance. At high data rates, the error introduced by an oscilloscope can become appreciable and can start impacting the measured design performance. Having more bandwidth in an oscilloscope with poor noise floor performance can increase measurement uncertainty and decrease measurement accuracy, which could lead to reduced design margins. Oscilloscope bandwidth, combined with low noise performance, is needed to accurately measure the true performance of high-speed digital I/O COTS technologies.

The jitter performance of your oscilloscope is another key consideration. The system's total jitter (TJ) can impact the reliability and robustness of the high-speed digital I/O link. Jitter is defined as the deviation of a signal transition from its ideal time. It affects the ability of a multi-Gb/s receiver to properly recover the clock and sample the incoming data, causing system error. If there is too much jitter, system errors can occur. The higher the data transfer rate, the less tolerant the receiver is to jitter. Jitter is statistical in nature, and it can be broken down into two main categories: deterministic jitter (DJ) and random jitter (RJ). DJ is correlated and bounded. It can be caused by intersymbol interference, crosstalk, subharmonic distortion and other spurious events such as power-supply switching. In contrast, RJ is uncorrelated and unbounded jitter caused by thermal or other physical, random processes. You need an oscilloscope with low intrinsic jitter to accurately measure the jitter performance of the digital I/O link to help ensure its reliability and robustness for defense applications.

Digital I/O link reliability and robustness are critical for defense applications where you need to ensure a high probability of mission success. Selecting a digital oscilloscope with the highest bandwidth and lowest noise and jitter measurement floor can ensure measurement accuracy and higher design margins and help to mitigate risk in migrating to COTS digital I/O technologies.

Protocol Layer Test Challenges

Engineers traditionally have used oscilloscopes exclusively for physical layer testing. When they needed to test the protocol layer, engineers had to manually decode waveforms captured by the oscilloscope or search for a protocol analyzer customized for a specific bus. In today's systems, serial buses often provide critical access points for debug and characterization.

Physical layer issues can manifest themselves at the protocol layer, particularly at higher bus speeds. You can use an oscilloscope for debugging these types of issues since they provide insight across both physical and protocol layers. Oscilloscope-based protocol analysis also allows you to attach oscilloscope probes for mid-bus probing, which means you can passively monitor serial signals without breaking the bus or changing timing or parametric behavior of the bus. Passive monitoring can uncover physical layer problems that traditional protocol analysis will not necessarily reveal.

Protocol analysis in an oscilloscope is designed to extend oscilloscope debugging capability, not to replace traditional protocol analyzers. Correlation between physical layer and protocol layer measurements can provide insight into physical layer issues that cause protocol issues. Oscilloscopes with protocol analysis viewers provide powerful time-correlated views of waveforms, symbols, character-, link-, and transaction-layer packet data down to the bit level. This makes it easy for you to isolate communication faults to logic or analog sources. For example, this capability makes it easy to trigger on an issue that manifests itself at the protocol layer and quickly zoom to the physical layer measurement to see if it is caused by a signal integrity issue.

Figure 1. Three instruments in one – a 9000 Series oscilloscope with built-in protocol analysis for USB, I²C, RS-232, SPI, CAN, FlexRay, and PCI Express®

Serial packet content is fed from front-end input circuitry to the oscilloscope trigger to enable real-time serial packet triggering. You can specify a number of protocol-specific trigger conditions. The oscilloscope circuitry compares these conditions to the incoming serial stream and in real time can determine when to trigger, either repetitively or via a single-shot measurement.

Oscilloscopes that include hardware-based serial decode capability perform serial decode in hardware instead of software, which speeds time required for processing and update rate while minimizing dead time between oscilloscope acquisitions. When you are making single-shot measurements with an oscilloscope, processing via either software or hardware is adequate. You can potentially miss events using software triggering due to blind time between acquisitions, as well as the time required to decode between acquisitions. Appendix B shows a table of serial bus protocols, and a summary of software vs. hardware triggering options.

Protocol Layer Test Challenges (cont)

As multi-Gb/s serial links are deployed, it is less obvious whether to choose a traditional protocol analyzer or outfit a more general-purpose oscilloscope with protocol analysis. Digital oscilloscopes do not replace protocol analyzers, but they do provide oscilloscope-centric hardware engineers the capability of analyzing issues across both the physical and protocol layer domains. This can help you understand and debug issues when you transition designs to COTS digital I/O technologies, which can help ensure reliable and robust link performance for a higher probability of mission success.

So, when is a traditional protocol analyzer required for debug and validation of a system? What capabilities distinguish it from the oscilloscope solution we just described?

An oscilloscope-based protocol solution, for example, is limited to making measurements on PCIe® links with a single bidirectional lane, also called PCIe bi-one (x1). More sophisticated digital systems such as servers include multi-lane PCIe links that are x4, x8 and x16 in lane width. For these multi-lane PCIe links, a protocol analyzer measurement solution such as the PCIe Gen3 U4300 Series, as shown in Figure 2, is the right tool.

Figure 2. U4300 Series PCIe Gen3 protocol analyzer

Another capability in the U4300 Series PCIe protocol solution is the ability to define complex, serial packet oriented triggers. FPGA hardware makes it possible to do this. For example, with a protocol analyzer, you can define a trigger such as "trigger on a memory read request from an endpoint to the root-complex when a particular data pattern is transmitted, and send a cross trigger to an external oscilloscope when this happens."

Also, the U4300 Series protocol solution includes an exerciser which can become "part" of the link to act like a root complex or end point and which can generate traffic such as that associated with a link training sequence state machine (LTSSM), a transaction-layer packet (TLP) or a data link layer packet (DLLP), including the insertion of errors.

Protocol analysis helps to ensure that the functionality of your COTS digital I/O design is robust, to help ensure a higher probability of mission success.

Addressing Test Challenges for COTS Digital I/O Technologies

The previous sections described general physical-layer and protocol-layer considerations and test challenges. This section will provide an overview of some of the COTS-specific technologies listed in Appendix A which may be of interest for defense applications.

CAN

http://cp.literature.agilent.com/litweb/pdf/5990-5077EN.pdf
http://cp.literature.agilent.com/litweb/pdf/5990-6677EN.pdf

Description: CAN is a message-based protocol, designed specifically for automotive applications, but it is now also used in other areas such as industrial automation and medical equipment. CAN and LIN are the backbones for communication among many separate controllers, sensors, actuators, and ECUs located throughout automotive and industrial designs. These serial bus interfaces provide content-rich points for debug and test.

Challenges: These protocols transfer bits serially, so using a traditional oscilloscope has limitations. Manually converting captured 1's and 0's to protocol requires significant effort, can't be done in real-time, and opens the door for potential for human error. In addition, traditional scope triggers are not sufficient for specifying protocol-level conditions.

Solution: Extend your scope capability with Agilent's CAN, LIN and FlexRay triggering and decode application. This application makes it easy to debug and test designs that include these buses using either your InfiniiVision 3000 X-Series or 7000 Series oscilloscope, or Infiniium 9000/90000 Series oscilloscope.

- Set up your scope to show CAN, LIN or FlexRay protocol decode in less than 30 seconds.
- Get access to a rich set of integrated protocol-level triggers.
- Save time and eliminate errors by viewing packets at the protocol level.
- Use time-correlated views to quickly troubleshoot serial protocol problems back to their timing or signal integrity root causes.

DDR

http://cp.literature.agilent.com/litweb/pdf/5989-7243EN.pdf

Description: Double data rate DRAM is a class of memory integrated circuits used in computer system and embedded system designs such as consumer and mobile devices. The bus interface has high data transfer rates up to 2133MT/s. The DRAM specification standards are developed by JEDEC. The specification contains electrical, timing and clock parameters that can be used as reference to qualify the DRAM for optimal performance in a memory system design.

Challenges: One of the biggest challenges in DDR memory bus test and debug is separating read and write data for measuring data valid windows with real-time eye diagrams. One way to separate read or write commands is to do command decode using RAS, CAS, WE, CS and clock. This method is tedious with limited probing points on tight board space.

The memory industry is trending towards smaller packages and demanding, more capacity and less power consumption, so designs are becoming more compact and data transfer speeds are increasing. The limited board space makes it extremely hard for designers to design in footprints or connectors for debug and characterization purposes.

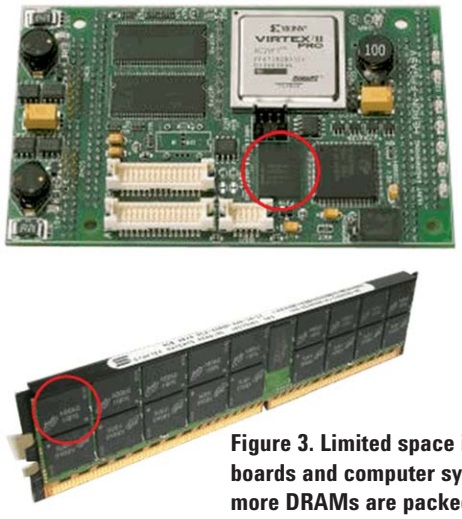


Figure 3. Limited space in embedded boards and computer systems means more DRAMs are packed into a DIMM configuration to enable higher capacity.

Solution: Using an oscilloscope with InfiniiScan+ software and the zone qualify trigger tool provides the easiest and quickest method to separate read and write signals. Instead of needing to access all the command bus signals–RAS, CAS, WE, CS and clock–you only need to probe the data strobe, DQS and data DQ. You will see two distinctive burst patterns. By drawing a trigger zone on one of the DQS burst patterns, you can separate the read and write data.

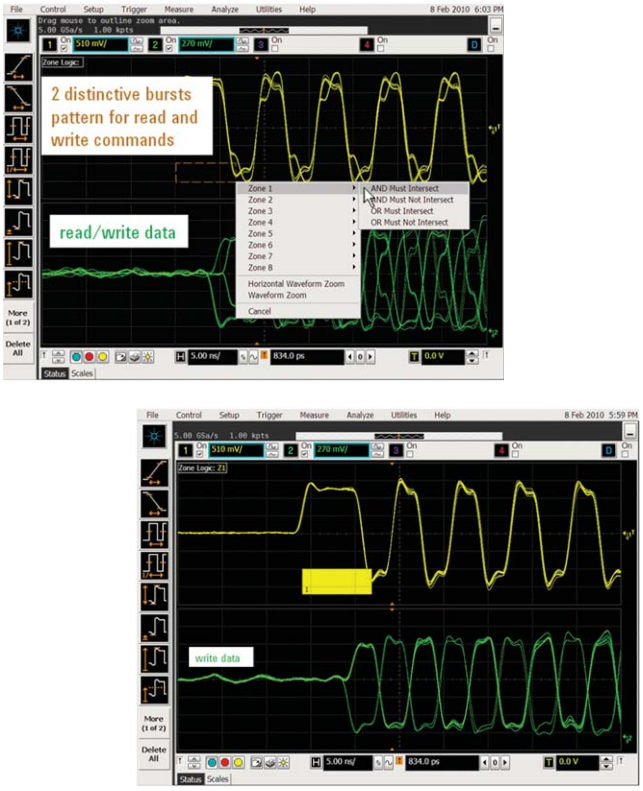


Figure 4. Using InfiniiScan software's zone qualify trigger enables you to trigger on read or write bursts to separate read and write data for eye diagram testing. Read data is edge aligned with the strobe while the write data is center aligned with the strobe.

The DDR BGA interposer probing solution helps resolve the issue with limited board space and enables probing at the DRAM as specified by the JEDEC specification. The probe has small keep-out volume and can be attached directly to an embedded design board or a DIMM configuration using a standard BGA rework station. Signals are routed out from the DRAM to the probing pads to provide connections to the oscilloscope.

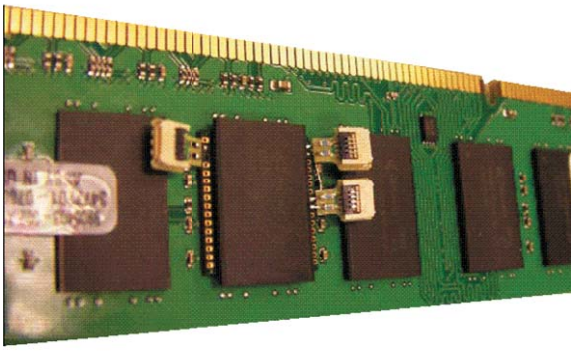


Figure 5. The BGA probe is soldered between the DRAM and the DIMM to provide connection to the oscilloscope ZIF probe heads.

Reference material

Agilent U7231A DDR3 Compliance Test Application Data Sheet (5989-7243EN)

W2635/6A DDR3 BGA Probe Adapter Data Sheet (5989-7643EN)

A Time Saving Method for Analyzing Signal Integrity in DDR Memory Buses Application Note (5989-6664EN)

It's also important for validation and performance teams to have a functional view of DDR memory if they have a fundamental concern about whether the memory system is operating properly from a memory protocol and data transfer point of view. For that type of application, a logic analyzer with a DDR memory decoder is required, such as the U4154A logic analyzer shown in Figure 6.

With this solution it is possible to make measurements on the fastest DDR systems, such as 2133 MT/s DDR3 memories. Capabilities such as synchronous state capture up to 2.5 GT/s in full channel mode, coupled with a 2.5 GT/s 8 level sequencer, the ability to sample data eyes as small as 100 ps by 100 mV, and the ability to set sample points with 5 ps and 5 mV precision, allow you lock onto your fast DDR address, control and data signals with a very low error rate for validation and debug.

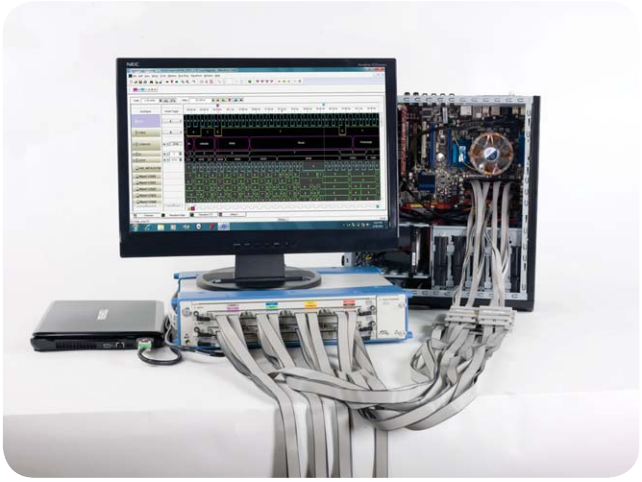


Figure 6. U4154A-4 Gb/s DDR3 logic analyzer solution

Such an analyzer also gives you a view of the signal integrity of your DDR signals, including characteristics like a byte lane shift. A tool called "Eye Scan" yields a view of each eye as shown in figure 7.

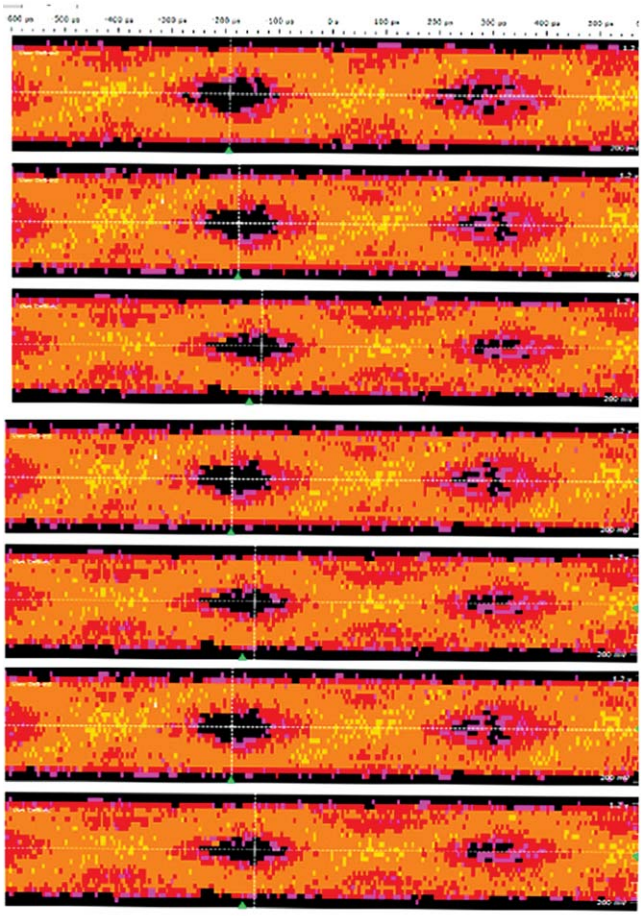


Figure 7. Eye scan trace of DDR data eyes and a byte lane shift

Ethernet

http://cp.literature.agilent.com/litweb/pdf/5989-1527EN.pdf

Description: The Ethernet standard (IEEE 802.3) is widely deployed today, ranging from 10BASE-T (10 Mb/s), 100BASE-TX (100 Mb/s), and 1000BASE-T (250 Mb/s, 4 lanes) and 10 Gb/s in twisted pair to 1, 10, 40, and 100 Gigabit Ethernet in fiber. Designs implementing 10/100/1000M Ethernet must characterize each of the three electrical standards for full compliance. For some 10-Gigabit Ethernet standards, designers must characterize the four XAUI electrical streams operating at 3.125 Gb/s, the combined
10-Gb/s electrical signal, and finally the 10-Gb/s optical signal.

Challenges: The high data rates of Gigabit Ethernet require wide bandwidths and low noise/jitter from real-time digital oscilloscopes to provide adequate margin in debugging physical layer issues. A wide range of electrical tests must be performed to ensure compliance with IEEE 802.3-2005 and ANSI X3.263-1995 standards.

Solution: Agilent Technologies N5392B Ethernet electrical performance validation and compliance software for Infiniium Series oscilloscopes provides a fast and easy way to verify and debug 1000BASE-T, 100BASE-TX and 10BASE-T Ethernet designs. The Ethernet electrical test software automatically executes Ethernet physical-layer (PHY) electrical tests, and it displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely the device passed or failed each test. The Ethernet electrical performance validation and compliance software performs a wide range of electrical tests to meet the Ethernet electrical specifications for 1000BASE-T, 100BASE-TX and 10BASE-T systems as documented in the IEEE 802.3-2005 and ANSI X3.263-1995 standards. Consider U7236A for 10GBASE-T and N5431A for XAUI (they are similar to N5392, but N5392 does not cover these Ethernet standards). Also consider the N5395C test fixture for 10/100/1000 BASE-T measurements, and the U7237A test fixture supporting the U7236A 10GBASE-T.

Fibre Channel (FC) and 10 Gbit Ethernet (10 GbE)

www.agilent.com/find/dcax

Description: 8G Fibre Channel and 10-Gbit Ethernet were developed at approximately the same time, which allowed companies and standards to leverage many technologies. Consequently, electrical and optical parameters tests are similar.

10-Gbit Ethernet is the incremental step up from 1 GbE. However, the speed increase has been so significant that the IEEE developed optical interfaces and electrical interfaces in parallel. The electrical interfaces are for short distances (typically 3 to 10 m) and are derived from interface requirements between the host (server, switch router) and an optical transceiver.

Fibre Channel originated in the 1980s as a commercial storage and peripherals networking protocol. More recently, Fibre Channel has become a potential technology for MIL-STD-1553 applications.** Payload throughput ranges from 100 Mbytes/s to 1600 Mbytes/s, requiring signaling rates between 1.0625 Gbaud and 14.025 Gbaud.

**http://www.t11.org/t11/stat.nsf/8ae7a802dbcaea9585256e5c0071f3f0/7bfccdb2535b70b585256df10057d652?OpenDocument

Challenges: Components, subsystems and total solutions for storage area networks tend to be price sensitive. Interoperability has been paramount for vendors and the standards body. As a result, INCITS has specified performance criteria for Fibre Channel at various points in the link to ensure reliable communication under worst-case conditions and for any combination of compliant hardware and software. These requirements make it essential to test at all design levels and to some extent also in the component manufacturing process. For example, today's 8-14G optical transmitters for Fibre Channel or Ethernet applications have low manufacturing costs, yet also possess process variations that make it necessary to tune and test each one individually.

Solution: Testing flexibility is essential to address different interoperability points. Communication typically starts in an ASIC, continues via a printed circuit board (PCB) to a transceiver module, then over multi-mode (or less commonly single-mode) fiber to the transceiver on the other side, then via a PCB to another ASIC. Manufacturers of passive components and systems test the PCB and related components such as connectors using the 86100C/D DCA with a TDR module. Semiconductor manufacturers test their ASICs using a DCA with an 86108A precision waveform analyzer (and 86118A dual remote heads and 86107A precision timebase if the design will be future-proofed to 25-40 Gb/s). Optical transceiver manufacturers tune and test the transmitter with the 86100C/D DCA and an optical module (such as the 86105C, 86105D or 86115D). Most of these tests also involve a pattern generator (PG) or bit error rate tester such as the N4903B J-BERT. J-BERTs have the advantage of also performing receiver stress tests – in essence, they verify that an optical receiver or the receiving ports of an ASIC will achieve the desired low bit error ratio (BER) even in the presence of significant jitter or amplitude interference.

System-level tests typically do not have access to a clock signal. An optical or electrical clock recovery provides the necessary signals to trigger a DCA or error detector for a J-BERT. Clock recovery also allow engineers to test the performance of oscillators and phased-locked loops (PLLs) commonly found in subassemblies or complete systems (for example, server, router and switch systems).

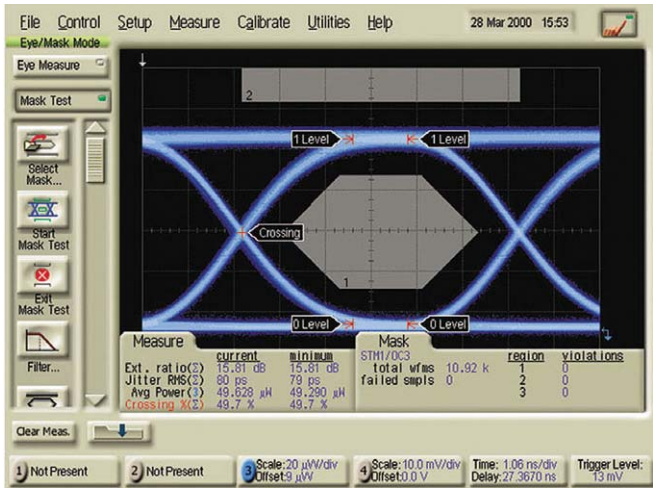


Figure 8. DCA-J eye mask measurement

I²C

http://cp.literature.agilent.com/litweb/pdf/5990-3925EN.pdf
http://cp.literature.agilent.com/litweb/pdf/5990-6677EN.pdf

Description: I²C (inter-integrated circuit) is a 2-wire serial interface used to attach low-speed peripherals to a motherboard, embedded system, or cell phone. I²C buses are pervasive in electronic designs and often used for configuration management.

Challenges: In many designs an I²C bus provides a content-rich point for debug and test. However, since I²C transfers bits serially, using a traditional oscilloscope has limitations. Manually converting captured 1's and 0's to protocol requires significant effort, can't be done in real-time, and opens the door for potential human error. In addition, traditional scope triggers are not sufficient for specifying protocol-level conditions.

Solution: Agilent's I²C triggering and decode application makes it easy to debug and test designs that include I²C protocols using your scope.

- Set up your scope to show I²C protocol decode in less than 30 seconds.
- Get access to a rich set of integrated protocol-level triggers.
- Save time and eliminate errors by viewing packets at the protocol level.
- Use time-correlated views to quickly troubleshoot serial protocol problems back to their timing or signal integrity root cause.

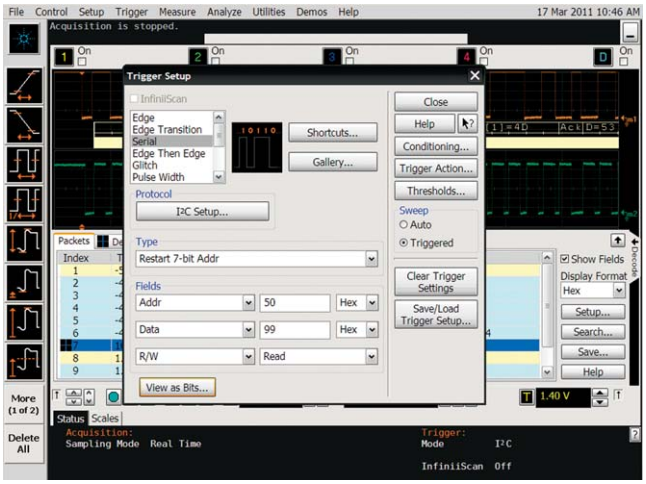


Figure 9. I²C trigger setup on a 9000 Infiniium Series oscilloscope

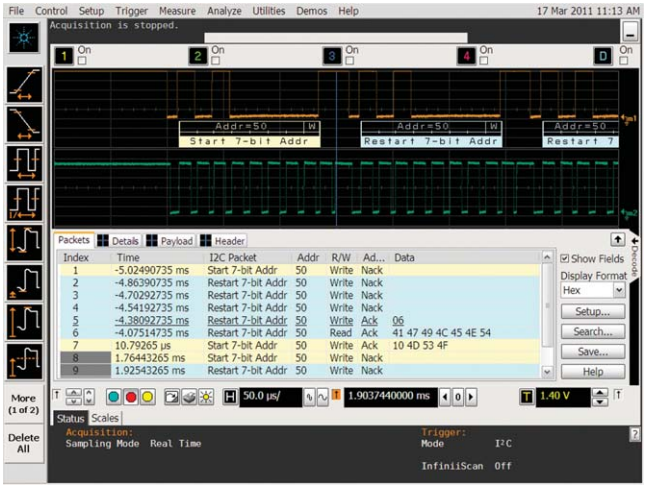


Figure 9a, I²C measurement on an Infiniium Series oscilloscope

JTAG

Description: The IEEE 1149.1 standard, often referred to as JTAG (Joint Test Access Group) standard, is widely used for board testing and as a critical IC interface. Nearly every electronic device incorporates JTAG, yet few tools provide JTAG protocol decode.

Challenges: While oscilloscopes have long been used to debug JTAG (IEEE 1149.1) signal integrity issues, Agilent's Infiniium Series is the first oscilloscope family to support JTAG protocol decode. While the need to decode JTAG may be infrequent, the difficult process of manually decoding JTAG TAP controller states, including instruction and data register values, is time consuming and error prone.

Solution: The N8817A JTAG decode for Infiniium 9000, 90000, and 90000 X-Series oscilloscopes enables JTAG decode, from TMS, TDI, TDO, and TCK signals acquired on either scope or digital (MSO) channels. This application imports device names and opcodes from industry-standard BSDL files, displays JTAG protocol in real time, and flags certain types of error conditions.

The multi-tab protocol viewer includes search capabilities and correlation between the waveforms and the selected packet, enabling you to quickly move between the physical and protocol layer information using the time-correlated tracking marker.

See real-time time-aligned decode of JTAG (IEEE 1149.1) from TDI, TDO, TMS and TCK signals.

- Quickly describe each unique scan chain and import BSDL files for each device in the chain
- View JTAG protocol including device names, OPCODES, and flagging of certain error conditions
- Use time-correlated views to move between protocol and physical layer views.

MIL-STD-1553

http://cp.literature.agilent.com/litweb/pdf/5990-4924EN.pdf

Description: MIL-STD-1553 is a legacy 1Mb/s avionics differential serial bus that uses self-clocking Manchester II bi-phase encoding. The electrical/physical layer voltage swings can range from 18 to 27 V p-p for transformer coupled, or 6 to 9 V p-p for direct coupled.

Challenges: Protocol testing can involve evaluating specific command, status, and data words to debug issues that may be occurring in a MIL-STD bus. However, using standard edge triggering typical of digital oscilloscopes yields a composite picture of all words repetitively overlaid on top of one another, making it difficult to diagnose and isolate issues. An external synchronization signal to use as a trigger source can sometimes help, but it is typically not available.

Moving from the protocol domain into the physical layer domain yields another set of challenges. Although MIL-STD-1553 is a digital data bus, the actual differential signals are very much analog in nature and no longer ideal 1's and 0's when employed into a real system consisting of stubs, terminals, couplers, and long transmission line cabling. Impedance mismatch, noise, and jitter can impact the physical layer performance and the signal integrity of the bus.

Solution: Using a scope with a MIL-STD-1553 decode and trigger option opens up the possibility of isolating acquisitions and measurements on particular transmitted or received words. The oscilloscope can be set up to trigger on specific data transmissions, which enables parametric measurements to be performed on specific transmitted or received words.

For physical layer testing, eye-diagram measurements provide a composite measure of the overall system signal integrity by overlaying all bits of each word tested. Eye-diagrams can be used to show worst-case timing variations, such as jitter and zero-crossing distortion, as well as vertical errors possibly caused by system noise or insufficient signal amplitudes induced by transmission line discontinuities, attenuations, and reflections.

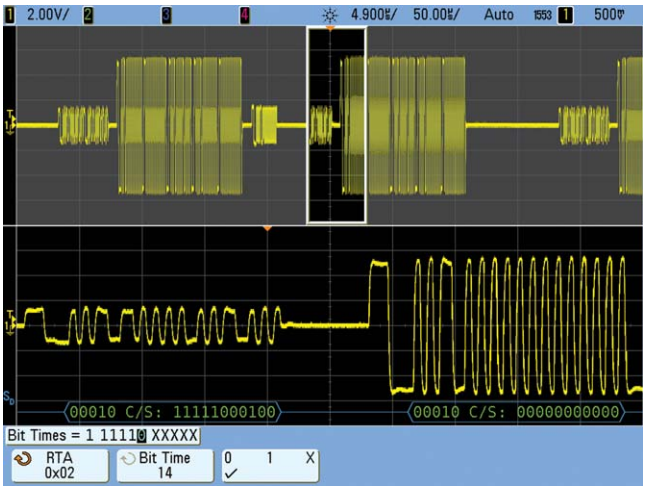


Figure 10. Set up MIL-STD-1553 trigger on specific data transmissions

Conventional eye-diagram displays are typically created using a reference clock as the scope's trigger source while capturing the signal repetitively with the timebase set up to display one or two bit times. Unfortunately, many of today's serial buses, including MIL-STD-1553 signals, do not provide an explicit clock signal from which to use as a trigger source. The MIL-STD-1553 system's clock must therefore be recovered/extracted from the serially transmitted data using either hardware or software techniques. Agilent's InfiniiVision Series scopes use a unique hardware-based clock recovery algorithm to create a MIL-STD-1553 eye-diagram display as shown below.

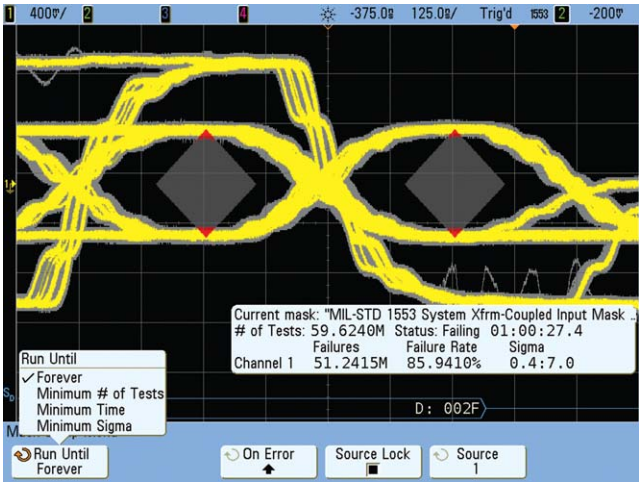


Figure 11. Setup MIL-STD-1553 eye diagram measurement

PCI Express

http://cp.literature.agilent.com/litweb/pdf/5989-1240EN.pdf

http://cp.literature.agilent.com/litweb/pdf/5990-6599EN.pdf

http://cp.literature.agilent.com/litweb/pdf/5989-4087EN.pdf

Description: PCI Express is a serial high speed interconnect that replaced legacy bus-based PCI and PCI-X technologies, and it is now migrating from desktop to embedded applications. PCI Express operates more like a network than a bus. It uses a point-to-point topology, with separate serial links connecting peripherals to the processor. Data rates range from 2.5 GT/s (PCIe 1.0) to 8 GT/s (PCIe 3.0 specification is not yet final at the time of this writing) using up to 32 lanes. Specifications and compliance tests are defined by the PCI Special Interest Group (PCI-SIG®).

Challenges: The transition from parallel to serial technology requires very different debug methods and tools. Many of these designs will leverage silicon and other IP already on the market. A key concern is how to evaluate, choose and select components and IP for your specific application. Lastly, probing an embedded link is significantly more challenging compared to motherboards and add-in cards since it is unlikely a standard PCI Express connector exists between transmitter and receiver.

Solution: Agilent Technologies N5393C PCI Express electrical performance validation and compliance software which works with the 90000A or 90000 X-Series Infiniium oscilloscopes to provide a fast and easy way to verify and debug PCI Express designs. The PCI Express electrical test software automatically executes PCI Express electrical checklist tests and displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely the device passed or failed each test.

The N5393C PCI Express electrical test software includes tests for verifying that transmitters are compliant with the PCI Express 3.0 BASE specification at 8 GT/s. It includes uncorrelated jitter tests, calculates de-emphasis and preshoot values for specified de-emphasis presets, and performs reference clock tests. In addition to supporting PCIe 3.0 measurements, the N5393C PCI Express electrical performance validation and compliance software performs a wide range of electrical tests as per the PCI Express 1.0a, 1.1, and 2.0 electrical specifications.

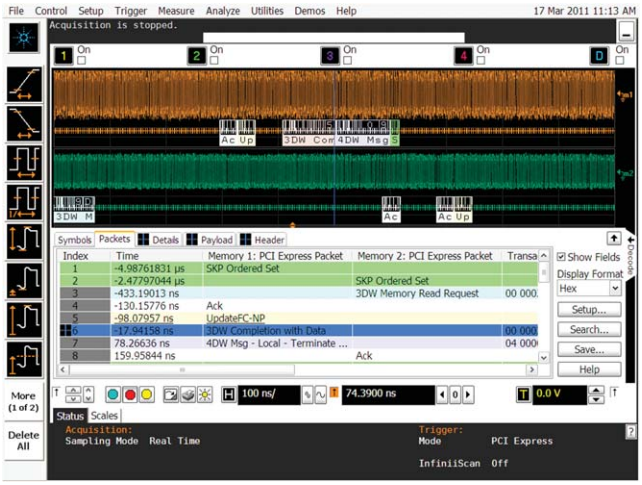


Figure 12. PCI-Express measurement on an Infiniium 9000 Series oscilloscope

In addition to transmitter (TX) testing, receiver (RX) testing is critical for error-free transmission in systems with transfer rates greater than 5 GT/s. Transmission of such fast signals across printed circuit boards (PCBs) can significantly deteriorate the signals to the extent that the eyes at the receiver (RX) inputs may be completely closed. TX de-emphasis only partially compensates channel-induced data dependent jitter (DDJ) such as inter-symbol interfererence (ISI), so RX equalization must also be included to enable error free transmission. Therefore RX testing is no longer optional and thus is included in standards such as the base and the card electro-mechanical (CEM) specification of PCI Express® rev. 3.0 that support transfer rates of 8 GT/s. A suitable test set-up based on the Agilent J-BERT N4903B and automation of the calibration procedure is available with the N5990A option 101 automation SW.

As mentioned earlier, Agilent U4300 Series PCIe protocol solutions include protocol analyzers and exercisers that offer multiple PCIe lane support as well as advanced protocol oriented triggering.

RS-232/422/485/UART

http://cp.literature.agilent.com/litweb/pdf/5990-3923EN.pdf
http://cp.literature.agilent.com/litweb/pdf/5990-6677EN.pdf

Description: RS-232 is the traditional name for a series of standards for serial binary single-ended data and control signals connecting between DTE (data terminal equipment) and DCE (data circuit-terminating equipment). RS-232 is commonly used in computer serial ports and is used extensively in aero-defense electronics. RS-422 provides for data transmission using balanced or differential signaling, point to point, or multi-drop.

Challenges: Digital communications networks implementing the RS-485 standard can be used effectively over long distances and in electrically noisy environments. Multiple receivers may be connected to such a network in a linear, multi-drop configuration. These characteristics make these networks useful in industrial environments and similar applications.

RS-232 and other UART (universal asynchronous receive and transmit) interfaces are widely used today in electronic designs. In many designs these serial buses tend to provide content-rich points for debug and test. However, since these protocols transfer bits serially, using a traditional oscilloscope has limitations. Manually converting captured 1's and 0's to protocol requires significant effort, can't be done in real-time, and opens the door for potential human error. In addition, traditional scope triggers are not sufficient for specifying protocol-level conditions.

Solution: Extend your scope capability with Agilent's RS-232/UART triggering and decode application. This application makes it easy to debug and test designs that include RS-232/UART protocols using either your InfiniiVision 3000 X-Series or 7000 Series oscilloscope, or your Infiniium 9000, 90000, or 90000 X-Series scope.

- Set up your scope to show RS-232/UART protocol decode in less than 30 seconds.
- Get access to a rich set of integrated protocol-level triggers.
- Save time and eliminate errors by viewing packets at the protocol level.
- Use time-correlated views to quickly troubleshoot serial protocol problems back to their timing or signal integrity root cause.

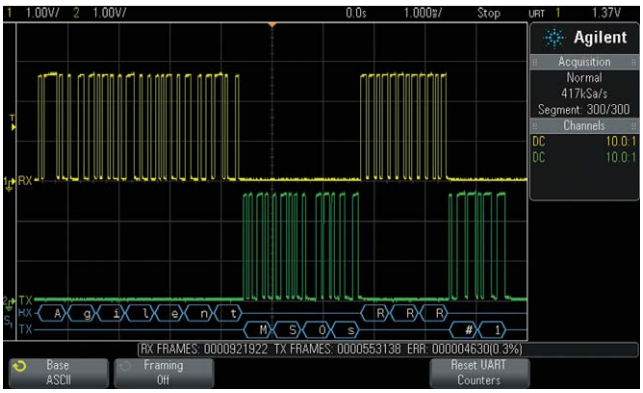


Figure 13. RS-232 protocol analysis on a 3000 X-Series oscilloscope

SPI

http://cp.literature.agilent.com/litweb/pdf/5990-3925EN.pdf
http://cp.literature.agilent.com/litweb/pdf/5990-6677EN.pdf

Description: The SPI (serial peripheral interface) bus is a synchronous serial data link standard that operates in full duplex mode. Devices communicate in master/slave mode, where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines. SPI can be configured as a 2-wire, 3-wire, or 4-wire bus and is used extensively for internal communication in embedded systems.

Challenges: In many designs a SPI bus provides a content rich point for debug and test. However, since SPI transfers bits serially, using a traditional oscilloscope has limitations. Manually converting captured 1's and 0's to protocol requires significant effort, can't be done in real-time, and opens the door for potential human error. In addition, traditional scope triggers are not sufficient for specifying protocol-level conditions.

Solution: Agilent's SPI triggering and decode application makes it easy to debug and test designs that include SPI protocol using your scope.

- Set up your scope to show SPI protocol decode in less than 30 seconds.
- Get access to a rich set of integrated protocol-level triggers.
- Save time and eliminate errors by viewing packets at the protocol level.
- Use time-correlated views to quickly troubleshoot serial protocol problems back to their timing or signal integrity root cause

Summary

Rapidly evolving COTS digital I/O technologies offer many potential benefits for increased data throughput and lower latency in aerospace/defense applications. However, as data rates increase to multi Gb/s, significant design margin and testing challenges emerge at both the physical and protocol layers. As the data rates increase, design margins decrease, and you need increased measurement fidelity to evaluate performance and debug issues.

Digital oscilloscopes with wide bandwidths, low noise, and low jitter provide the signal fidelity you require to measure the true performance of your designs. Compliance software applications for many of the COTS digital I/O technologies, combined with decode and protocol triggering, add the functionality needed for compliance testing and debugging. In addition, protocol analyzers help to ensure robust functionality of COTS digital I/O technologies leveraged into aerospace/defense applications.

Agilent's solutions are driven and supported by Agilent experts involved in international digital standards committees. Agilent digital test solutions can help you in migrating to these technologies with a comprehensive suite of high-speed digital test solutions and application expertise. Contact your local Agilent Technologies representative to see how Agilent's high-speed digital solutions can help you reduce risk and help you ensure success in migrating to digital I/O COTS technologies.

Related Links

Related Links

Title	Type	Link
Oscilloscope Solutions for Industry Standards	Poster	http://cp.literature.agilent.com/litweb/pdf/5989-6704EN.pdf
DDR Memory Application	Web page	www.agilent.com/find/ddr
DisplayPort Design and Test	Web page	www.agilent.com/find/DisplayPort
Ethernet Design and Test	Web page	www.agilent.com/find/ethernet
Digital Visual Interface (DVI)	Web page	www.agilent.com/find/DVI
HDMI Design and Test	Web page	www.agilent.com/find/HDMI
MIPI- Mobile Industry Processor Interface Test	Web page	www.agilent.com/find.MIPI
PCI Express Design and Test	Web page	www.agilent.com/find/pciexpress
Serial Attached SCSI (SAS)	Web page	www.agilent.com/find/SAS
Serial ATA (SATA) Design and Test	Web page	www.agilent.com/find/SATA
USB Design and Test	Web page	www.agilent.com/find/usb

Appendix A- COTS Digital I/O Technologies and Agilent Technologies Digital Test Solutions

Industry standard	Type	Application	Device performance	Oscilloscope and software	Compliance/ physical payer	Protocol	Logic analyzers, protocol analyzers, ARBs, pulse generators, JBERTs, noise generators, design tools
CAN (controller area network)	Serial	Controller-device communication	Up to 1 Mb/s	• 3000 X-Series with DSOX3AUTO • 7000 Series with N5424A protocol triggering and decode software • 9000 Series with N8803B protocol triggering and decode software • 90000 and 90000 X-Series with N8803A protocol triggering and decode software		X	• 16800/16900/U4154A Series logic analyzer with ALD analysis probe • 81150A pulse function arbitrary noise generator
DDR1 and LPDDR	Parallel	Memory	200-400 Mb/s	• 9000, 90000 or 90000 X-Series (2.5 GHz or higher recommended) with U7233A compliance test application software	X	X	• U4154A or 16900 Series logic analyzer with B4623A and B4622A
DDR2 and LPDDR2	Parallel	Memory	400-1066 Mb/s	• 9000, 90000 or 90000 X-Series (4 GHz or higher recommended) with N5413B compliance test application	X	X	• U4154A or 16900 Series logic analyzer with B4621A, B4622A or B4623A • JBERT N4903B or 81250A ParBERT
DDR3	Parallel	Memory	800-2133 Mb/s	• 90000 or 90000 X-Series (6 GHz or higher recommended) with U7231A compliance test application software	X	X	• U4154A or 16900 Series logic analyzer with B4621A or B4622A

Industry standard	Type	Application	Device performance	Oscilloscope and software	Compliance/ physical payer	Protocol	Logic analyzers, protocol analyzers, ARBs, pulse generators, JBERTs, noise generators, design tools
DisplayPort	Parallel	Display	1.62, 2.7,5.4 Gb/s/lane with 1,2, or 4 lanes	• 90000 or 90000 X-Series (8 GHz or higher recommended) with U7232 compliance test software	X		• U4154A or 16900 Series logic analyzer with FuturePlus analysis probe • J-BERT N4903B or 86100D DCA-X plus N5990A software
DVI	Parrallel	Graphics/display	Up to 3.96 Gb/s	• 90000 Series 4 GHz or higher with N5394A electrical performance validationand compliance software	X		
Ethernet	Serial	Local area networks	10 Mb/s -1Gb/s	1000/100/10 BaseT • 9000, 90000 or 90000 X-Series with N5392A conformance 10G/40G/100G • 86100D DCA-X Series software	X		• 81130A, 81132A, 81134A pulse generators, 81250A ParBERT
10 Gb Ethernet	Serial	Local area networks	10.3 Gbaud	• 86100C DCA-J/86100D DCA-X sampling oscilloscope	X		• N4903B J-BERT
Fibre Channel	Serial	Storage area networks	1/2/4/8/10/14 Gbaud	• 86100C DCA-J/86100D DCA-X sampling oscilloscope	X		• N4903B J-BERT
FlexRay	Serial	Controller-device communication	Up to 20 Mb/s	• 7000 Series with N5432C protocol triggering, decode and mask testing software • 9000 Series with N8803B protocol triggering and decode software • 90000 and 90000 X-Series with N8803A protocol triggering and decode software	X	X	• 81150A pulse function arbitrary noise generator
GDDR5	Parallel	Graphics/memory	Up to 8 Gb/s	• 90000 or 90000 X-Series oscilloscopes	X		* U4154A logic analyzer with flying lead probes to 1.5 Gb/s or Soft Touch up to 4 Gb/s
HDMI	Parallel	Display	250 MB/s-2.97 Gb/s per lane	• 9000, 90000 or 90000 X-Series (4 GHz or higher, 8 GHz recommended) with N5399B compliance software	X		• N5998A protocol analyzer and generator • E4887A TMDS signal generator + N5990A software, 81150A for HDMI Ethernet and audio return channel testing
High-speed Optical	Serial	System/storage		Fibre Channel, 10G/40G/100G Ethernet, SONET/SDH, PON • 86100D DCA-X Series Complex modulation (OMA) • N4391A optical modulation analyzer			
I^2C (inter-IC bus)	Serial	Device communication	Up to 3.4 Mb/s	• 3000 X-Series with DSOX3EMBD • 7000 Series with N5423A protocol triggering and decode software • 9000 Series with N5391B protocol triggering and decode software • 90000 and 90000 X-Series with N5391A protocol triggering and decode software		X	• 16800 Series logic analyzer with ALD analysis probe
JTAG (IEEE 1149.1)	Serial	Board test, IC debug port	Up to 100 Mb/s	• 9000, 90000 and 90000 X-Series with N8817A protocol decode software		X	

Industry standard	Type	Application	Device performance	Oscilloscope and software	Compliance/ physical payer	Protocol	Logic analyzers, protocol analyzers, ARBs, pulse generators, JBERTs, noise generators, design tools
LIN	Serial	Integration of sensors and actuators	Up to 625 kb/s	• 3000 X-Series with DSOX3AUTO • 5000, 6000, or 7000 Series with N5424A bus triggering and decode software • 9000 Series with N8803B protocol triggering and decode software • 90000 and 90000 X-Series with N8803A protocol triggering and decode software		X	
MIL-STD 1553	Serial	Avionics Bus	Up to 1 Mb/s	• 7000 Series with N5469A triggering and decode and mask testing software	X	X	• 81150A pulse function arbitrary noise generator
MIPI (D-Phy and M-Phy)	Serial	Chip/chip	D-PHY (up to 1.5 Gbps) M-PHY (up to 6.0 Gbps)	• 9000, 90000 and 90000 X-Series with option N8802A for D-Phy protocol decode	X, UDA	X	• 81250 ParBERT + 81150 pulse function arbitrary noise generator + N5990A automation software • N4851B MIPI D-PHY analyzer, N4861B stimulus (16800 or 16900) • N5343A MIPI M-PHY DigRF V3/V4 analyzer, N5344A exerciser (standalone)
PCI Express	Multi serial	Processor/ peripherals	2.5 Gb/s, 5 Gb/s, 8 Gb/s	• 9000, 90000, or 90000-X Series with N5364A/B protocol triggering and decode software • 86100D DCA-X Series with PLL and PLC testing software *1.0a and 1.1* • 90000 or 90000 X-Series (>6 GHz) with N5393B compliance software *2.0 and 3.0* • 90000 or 90000 X-Series (>12 GHz) with N5393B compliance software	X	X	• J-BERT N4903B + N5990A test automation software or 81250 ParBERT + E2960A Series PCIe protocol analyzer exerciser and jammer tools* • U4301A PCIe Gen 1/2/3 analyzer, U4305A exerciser
RS-232/422/ 485/UART	Serial	Computer serial port	Up to 10 Mb/s	• 3000 X-Series with DSOX3COMP • 7000 Series with N5457A protocol triggering and decode software • 9000 Series with N5462B protocol triggering and decode software • 90000 and 90000 X-Series with N5462A protocol triggering and decode software		X	• 16800 Series logic analyzer with ALD analysis probe
SAS 3G, 6G and 12G (Serial Attached SCSI)	Serial	Computer/storage	1.5-12 Gb/s	• 90000 Series (12 GHz recommended) with N5412B (6G SAS) • 90000 X-Series with UDA (12G SAS)	X, UDA	X	• J-BERT N4903B, 81134A pulse pattern generator, plus N5990A automotive software • U3051A and U3052A SerialTek SAS/SATA analyzer • U3053A and U3054A jammer and BIST

Industry standard	Type	Application	Device performance	Oscilloscope and software	Compliance/ physical payer	Protocol	Logic analyzers, protocol analyzers, ARBs, pulse generators, JBERTs, noise generators, design tools
SATA (Serial ATA) I/II/III	Serial	Computer/storage	1.5-6 Gb/s	• 90000 or 90000 X-Series (12 GHz recommended) with N5411B compliance software • 90000 or 90000 X-Series with N8801A protocol decode software	X	X	• J-BERT N4903B, 81134A pulse pattern generator, plus N5990A automotive software • U3051A and U3052A SerialTek SAS/SATA analyzer • U3053A and U3054A jammer and BIST
SPI (serial peripheral interface)	Serial (2-4 wire)	Point-to-point communication	Up to 50 MB/s	• 3000 X-Series with DSOX3COMP • 7000 Series with N5423A protocol decode software • 9000 Series with N5391B protocol triggering and decode software • 90000 or 90000 X-Series with N5391A protocol decode software		X	• 16800 Series logic analyzer with ALD analysis probe
USB (2.0 and 3.0)	Serial	Processor/ peripherals	1.5 MB/s- 4.8 GB/s	**USB 2.0** • 9000 or 90000 Series with N5416A compliance test software • 9000, 90000 or 90000 X-Series with N5464B or N5464A protocol triggering and decode software **USB 3.0** • 90000 Series with U7243A compliance test software • 90000 or 90000 X-Series with N8805A protocol decode software	X	X	• 16800/16900/U4154A Series logic analyzer with FuturePlus analysis probe • 81134A pulse pattern generator + N5990A automation software (USB 2.0) • J-BERT N4903B + N4916B de-emphasis box + N5990A automation software (USB 3.0)
XAUI	Serial	Chip/chip	Up to 10 Gb/s	• 90000 Series with N5431 AXAUI electrical validation application software	X		

Serial bus protocol	Infiniium 9000 Series		Infiniium 90000 Series
	SW trigger	HW trigger	SW trigger
I2C		√	√
SPI		√	√
RS-232		√	√
CAN		√	√
LIN		√	√
USB		√	√
PCIe		√	√
JTAG	√		√
MIPI D-Phy	√		√
8B/10B	√		√
SATA	√		√

Appendix B- Software vs. Hardware Triggering Options for Serial Bus Protocols

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