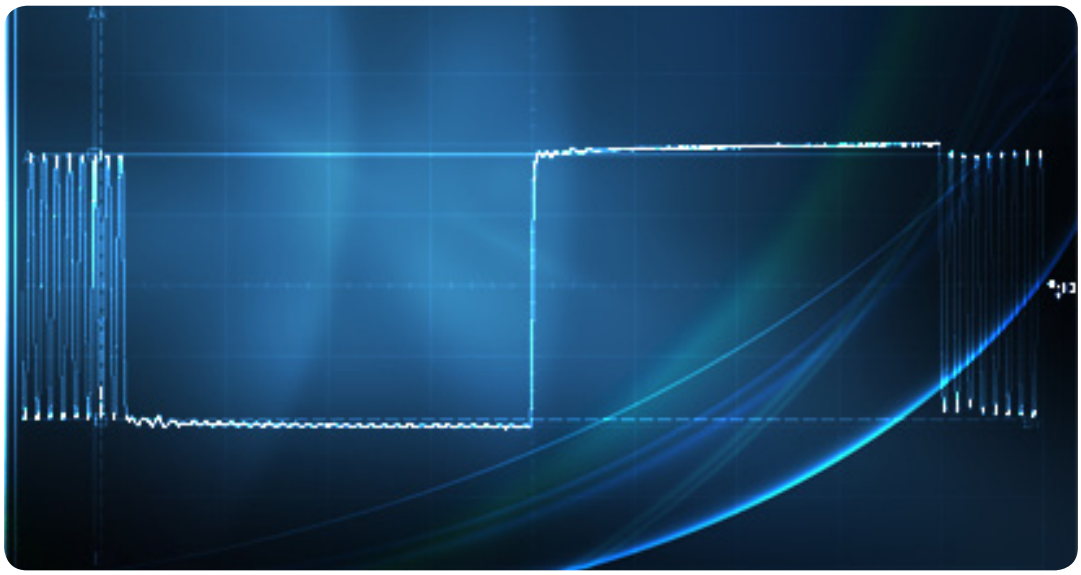
How to Pass Receiver Test According to PCI Express® 3.0 CEM Specification with Add-In Cards and Motherboards

Application Note



Agilent Technologies

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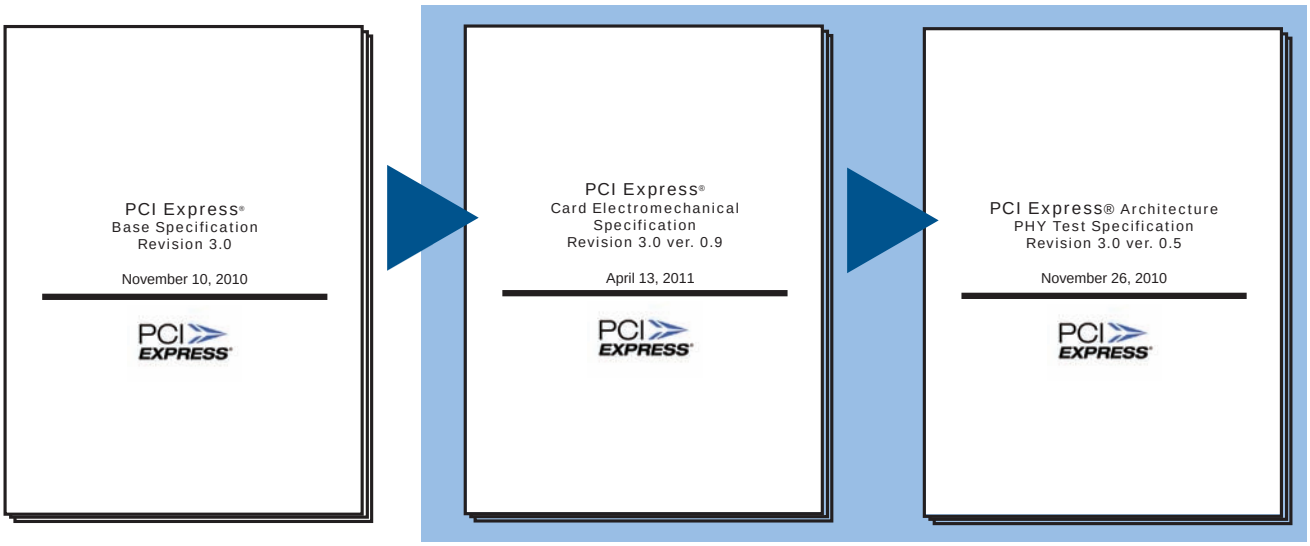
1. Introduction

Since the release of the PCIe® base specification revision 3.0 (rev. 3.0) in November 2010, many semiconductor vendors have tested their bare ASICs accordingly [1]. Now PCIe 3.0 add-in cards (AICs) and motherboards (MBs) with PCIe 3.0 slots are being developed. These items need to be tested according to the PCIe Card Electromechanical (CEM) Specification [2], for which the Serial Enabling Group (SEG) is currently generating the PHY Test Specification [3] (see Figure 1).



Base Specification (1.0)

Developed by:

Electrical Work Group (EWG)

- Contains compendium of system knowledge
- Can directly be applied to ASIC test

Card Electromechanical (CEM) Specification (0.9)

Developed by:
Electro-Mechanical work group

- Applies to add-in cards and mother boards (MB)
- Reduces card manufacturer's need to study the base specification
- Increases reproducibility through PCI-SIG – supplied compliance base board (CBB) and compliance load board (CLB)

Phy Test Specification (0.5)

Developed by:

Serial Enabling Group (SEG)

- defines detailed compliance tests procedures based on CEM specification and practical experience from workshops

Figure 1. Sequential development of the PCIe specifications relevant for the PHY and their scope

At time of issue of this document neither the CEM Specification (currently version 0.9) nor the PHY Test Specification (currently version 0.5) has been released. This application note represents a snapshot of the status at the time of issuing.

Its intent is to assist card vendors through pre-release testing. As the specifications are not yet final, target values for calibration or the calibration procedure may change. The reader is advised to check the current version of the relevant specification and if it differs from those mentioned above, check for possible changes.

The biggest change between PCIe 2.x and rev. 3.0 is that RX testing on cards will now be normative. This application note provides insight into the calibration method and tests, as well as the tools available from Agilent Technologies. Designed to help integrators with the transition to rev. 3.0, these solutions leverage Agilent's experience from active participation in the related PCI-SIG® workgroups and workshops.

About this document

This application note describes the steps necessary to run a receiver compliance test on PCIe 3.0 AICs or MBs:

1. Calibration of the closed-eye receiver stress signal according to the PHY test specification. It differs from PCI Express rev. 2.x in two ways:
   a) the RX stress signal is eventually specified by the eye height and width and no longer by its individual signal impairments
   b) the reference plane for the specification is defined inside the ASIC, i.e. after the (reference) receiver's equalization, necessitating post processing of the measured test signal
2. Steering the device under test (DUT) through the link training and status state machine (LTSSM) into loopback
3. Counting bits and errors of the signal looped back to determine bit error ratio (BER) and verify compliance

2. Overview of the RX Test and Calibration Procedure

2.1. Generic RX test: an overview

The RX test is used to determine the receiver's capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing, the input of the RX under test is stimulated with a calibrated stressed eye signal from a bit error ratio tester's pattern generator (BERT PG). This signal is composed of the impairments to be expected at the RX input when it is operating in a target system. These include timing impairments such as jitter and superimposed voltages, emulating crosstalk. The latter one is sometimes called noise, which might imply a Gaussian distribution. For test purposes, however, this noise voltage is of sinusoidal shape.

Correct detection of the digital content can be checked with the BERT's error detector (ED), after the RX output signal is looped back internally through the transmitter (TX)[1] of the DUT. A simplified block diagram for an RX test is shown in Figure 2.

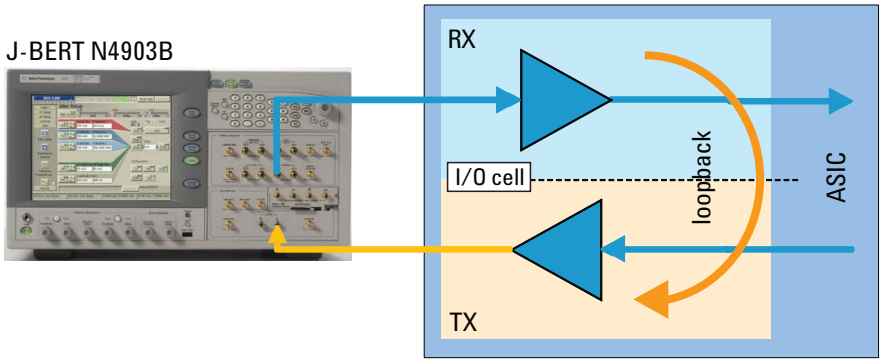


Figure 2 Simplified block diagram for an RX test

1. *The TX is assumed to operate error free*

2.2. Calibration method of the RX stress test signal for PCIe CEM rev. 3.0

Proper calibration of the stress signal is essential to achieve a valid and reproducible test result that eventually guarantees interoperability. For the CEM Specification several measures were taken in order to achieve this goal. First, compared to the Base Specification, the RX specification was simplified by removing parameters such as common mode voltage stress and jitter tolerance frequency sweep. Second, the PCI-SIG rev. 3.0 test tools, which include compliance test boards and SigTest software, create a well-defined test environment.

However, the simple PCIe 2.x approach that specifies the stress signal by individually calibrating random and sinusoidal jitter (RJ and SJ) is no longer possible for a couple reasons:

- In a real system, still there is RJ and bounded uncorrelated jitter (BUJ) which during a test is emulated by a PG's RJ and sinusoidal jitter (SJ). However, at 8 GT/s the largest portion of the jitter is caused by high frequency loss of the PC-board material, resulting in data dependant jitter (DDJ), particularly inter-symbol interference (ISI).

  In the rev. 3.0 test setup for AICs using SIG-supplied test boards, the majority of the DDJ is purposely caused by the rev. 3.0 compliance base board (CBB) riser card (see Figure 7). However, all other test setup components, such as cables, splitters, DC-blocks and even the BERT PG itself, also create non-negligible DDJ. Compared to PCIe 2.x, subtle differences between test setups from different vendors have a greater effect on the resulting stress signal. As it is impractical to accurately specify all the parameters influencing DDJ and individually measure them with sufficient accuracy, the stress signal is specified as the result of all influencing effects by its eye-opening in terms of eye-height (EH) and eye-width (EW).
- Measuring the stress components of the test pattern directly at a test point best emulating the RX input, which is at the TX connectors of the compliance load board (CLB), is not possible since the eye at this test point is closed.
- Consequently, similar to the Base Specification, the stress signal's eye opening is defined after an adaptive reference equalizer (EQ) with a continuous time linear equalizer (CTLE) and a decision feedback equalizer (DFE), clocked by a reference clock recovery (CR) circuit [1].

1. CTLE with seven different "DC-attenuation" settings peaking at 4 GHz
2. Reference CR specified by OJTF with no peaking and 10 MHz BW
3. One tap DFE with a specified limit for d1 of ±30 mV

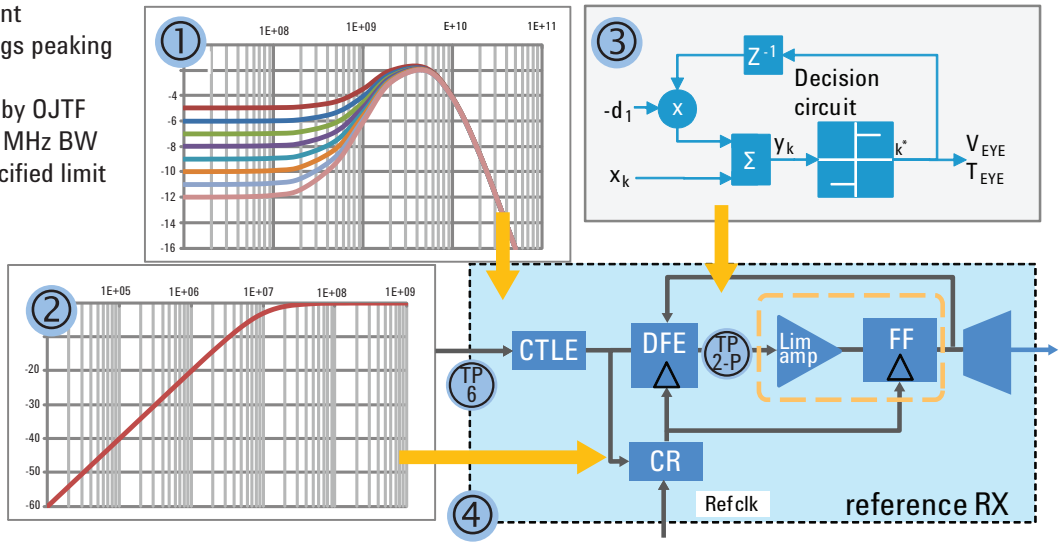


Figure 3. Reference RX (4) with its EQ components, CTLE (1) , and DFE (3) clocked via CR (2)

For the calibration of the RX stress signal at least two methods were available: the method used in the Base Specification and the following alternative. The latter is based on the consideration that during an RX test the BERT PG emulates the TX. Therefore, the calibration of the RX stress signal can use the same method used for the TX compliance test. This means the rev. 3.0 compliance pattern carrying all specified impairments is captured with a real time oscilloscope and then post-processed by the SigTest software that is provided to PCI-SIG members. It optimizes the reference RX's CTLE and DFE, and calculates EH and EW.

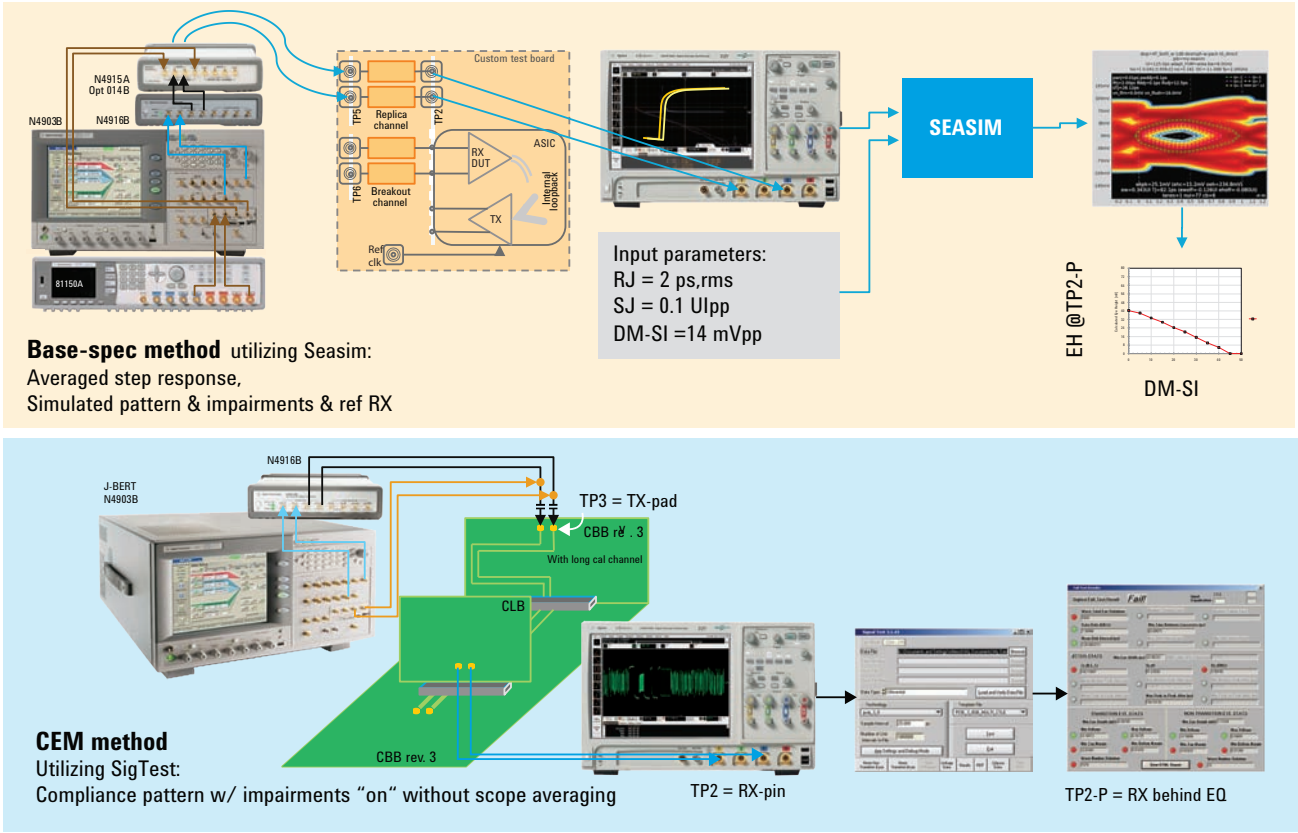


Figure 4. Comparison of the calibration methods between the Base Specification and the CEM Specification

This calibration approach differs from the Base Specification that uses the Seasim software to simulate the stress signal based upon an averaged step response (this method was chosen because the measurement is not compromised by the scope noise [4]).

Note: The SEG is currently working to achieve correlation between the different approaches followed by the Electrical Work Group (EWG) for the Base Specification using the statistical eye analysis simulator (SeaSim) method and the SEG method, which is specified in the PHY Test Specification using the SigTest. Depending on the outcome of this work, there is a chance that the currently applied method will need adjustments.

2.3. Calibration and test procedure

At the high data rate of 8 GT/s it is necessary to de-embed the test setup to compensate for its frequency response using the BERT's EQ. This post-cursor setting has to be accounted for when generating EQ presets during the RX test. Generator adjustments are described in Section 3. The two-stage calibration of the stress signal with pre-calibration of individual impairments and final adjustment of EH and EW, is described in Section 4. How to set the DUT into loopback and the RX test itself is described in Section 5.

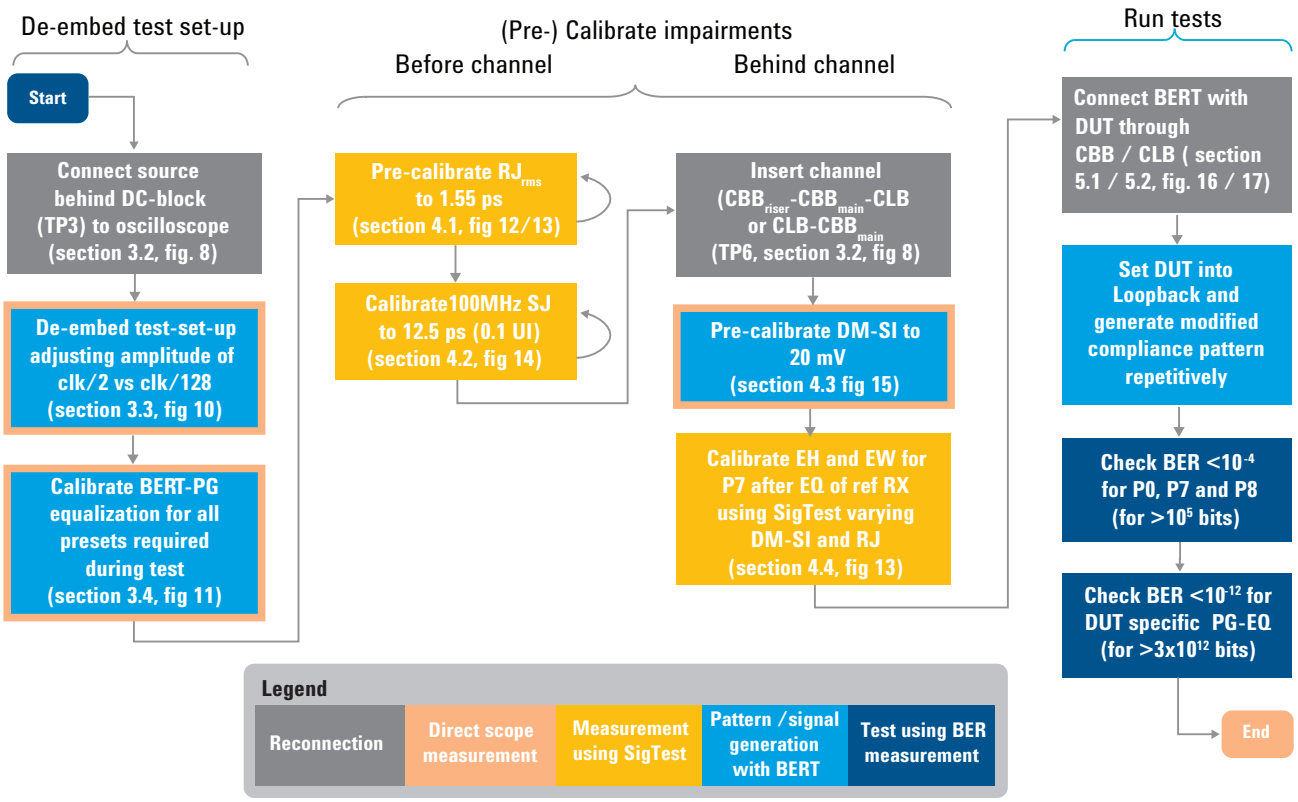
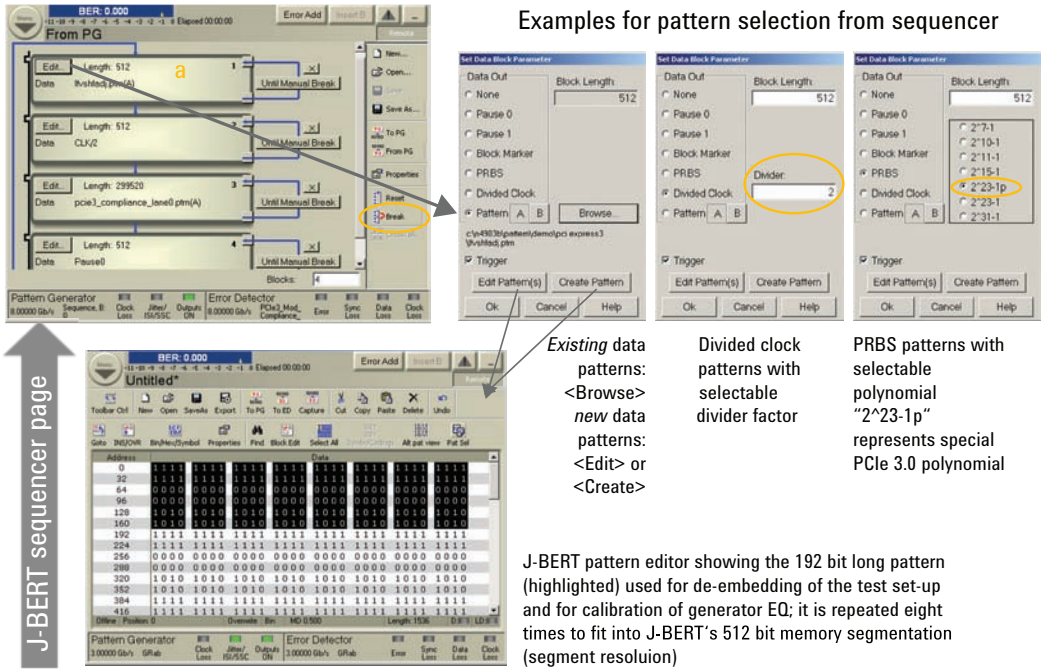


Figure 5. Flow chart of BERT-PG de-embedding, stressed eye signal calibration, and RX test according to PCIe CEM Specification 3.0 rev. 3.0



J-BERT pattern editor showing the 192 bit long pattern (highlighted) used for de-embedding of the test set-up and for calibration of generator EQ; it is repeated eight times to fit into J-BERT's 512 bit memory segmentation (segment resoluion)

Figure 6. Data setup on Agilent's J-BERT using the pattern sequencer allows easy set-up of algorithmic patterns such as pause, divided clock, PRBS, and fast-switching between them using the <Break> button (circled)

Note: For the different steps of the calibration process a variety of data patterns is required. These can easily be set up and accessed using the Agilent Technologies N4903B J-BERT high-performance serial BERT's powerful pattern sequencer with its manual sequence advance functionality as shown in Figure 6.

3. Set-up for Calibration, De-embedding, and BERT-EQ Calibration

3.1. The PCI-SIG-supplied test boards: CBB and CLB

Figure 7 shows the rev. 3.0 CBB and compliance load board (CLB) used for testing according to the CEM Specification. Unlike rev. 2, this CBB consists of two boards: the main card and the riser card (Figure 7e and 7f). With the additional connector between the two boards and the traces on the riser card, the new (rev. 3) CBB better represents the situation on server boards.

The RX SMP connectors on the riser card and CLB are intended to be electrically identical to the pad of the ASIC's TX. To achieve this, structures simulating the package can be found on the card (Figure 7a, b, and g). Two versions of the CLB are available: a card with a 1x and a 16x connector and another one with a 4x and an 8x connector (not shown).

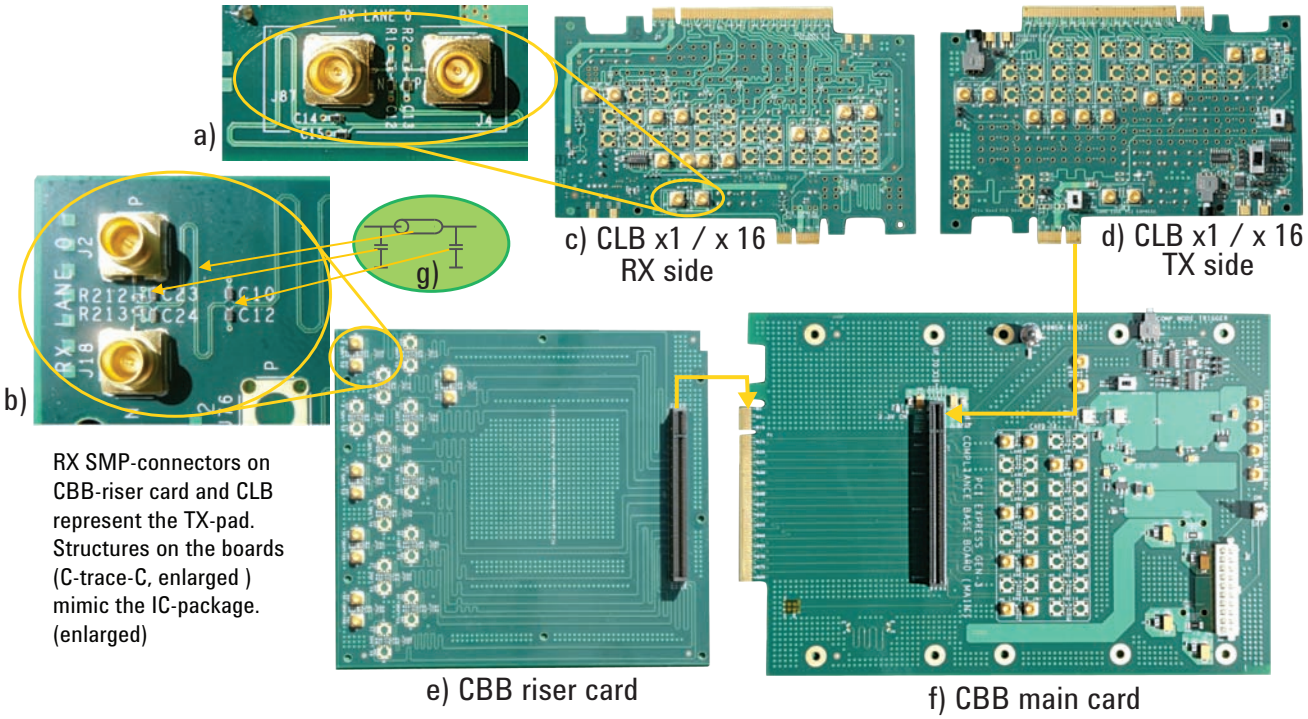


Figure 7. Revision 3 CBB and CLB boards: a and b) Details of the CLB and riser card showing package simulation with g) equivalent circuit, 1x and 16x CLB, c) RX side, d) TX side, e) CBB riser card and f) CBB main board with PCIe connector for CLB (center) and edge connector (left) for riser card

3.2. The setup for calibration

The set-up for calibration is shown in Figure 8. The BERT PG output signal is superimposed with a differential noise voltage, i.e. the differential mode sinusoidal interference (DM-SI). As shown in Figure 8, the output of the Agilent N4916B de-emphasis signal converter, driven from the Agilent N4903B, is combined with the DM-SI coming from the P1 outputs of the N4903B-J20, using asymmetrical splitters. DC blocks are used to achieve the desired AC coupling. (See Table 2 in Section 7.1 for a complete listing of required instruments and accessories.) A phase-matched set of low-loss cables with SMP connector ends represents the test signal generator output (TP3). The CBB and CLB form the channel, causing the more or less dominant part of the stress signal's DDJ to close the eye.

Depending on whether the AIC or MB is to be tested, connections and signal flows differ:

- AIC: Cables shown as 1 in Figure 8 (Cables ①) are connected to the RX connectors on the riser card of the CBB. The signal flows through both PCIe connectors via the CBB main board into the CLB TX SMP-connectors (also see Figure 16).
- MB: Cables ① are connected to the RX connectors on the CLB and the signal flows through the PCIe connector on the CBB main card to its TX connectors (also see Figure 17).

For calibration, some parameters are measured at TP3 in Figure 8, before the channel, dotted lines ①, or at TP6 behind the channel, solid lines shown as ② in Figure 8.

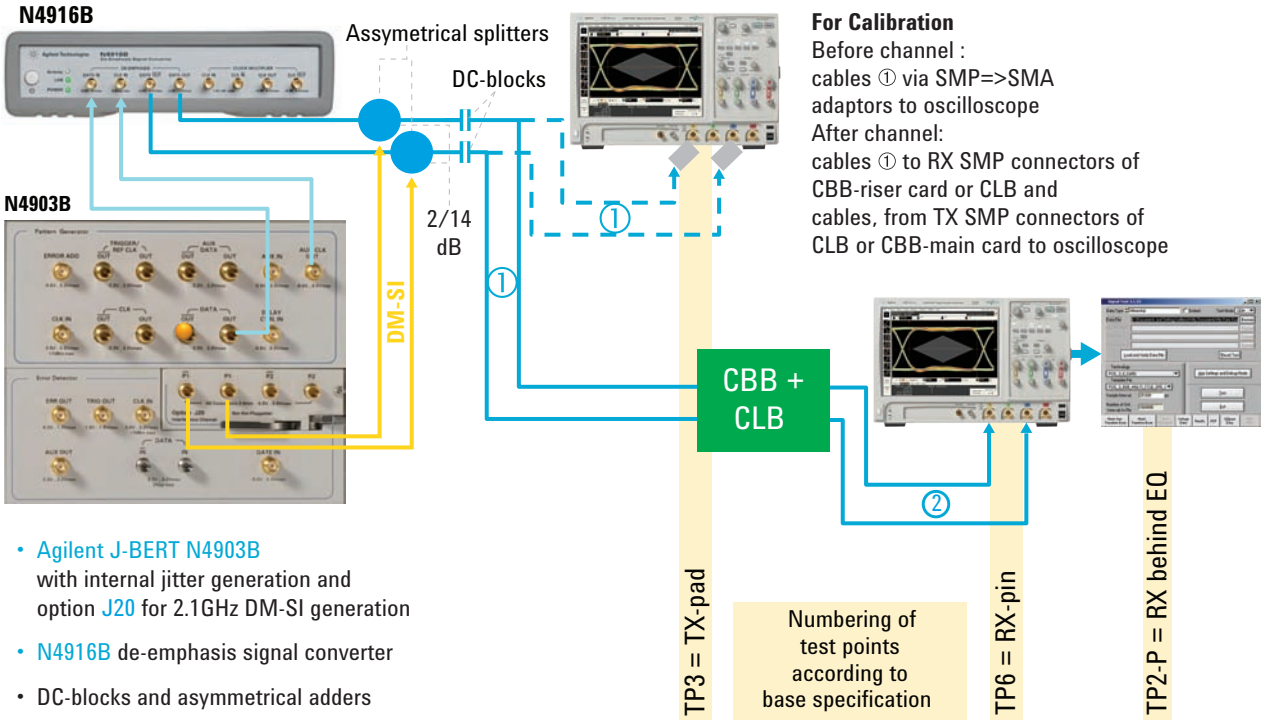


Figure 8. Set up for calibration

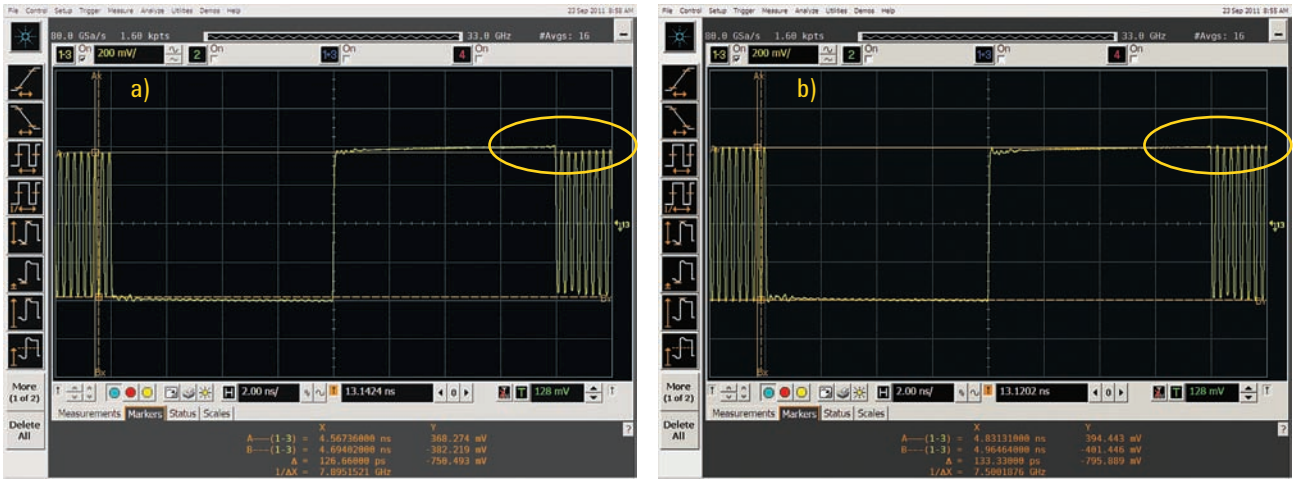
3.3. De-embedding of test setup

As previously mentioned, in both test cases the RX connectors on the riser card for AIC test and on the CLB for MB test are intended to represent the TX-pads of a PCIe ASIC. This means that nearly ideal, undisturbed signal performance shall be achieved at the SMP connectors of the cable pair ① shown in Figure 8, making an adjustment necessary for a couple reasons:

1. Test equipment's intrinsic signal performance and the frequency response of the combination of cables, splitters, and DC-blocks is not ideal.
2. At the same time, the parameters are not identical for test equipment, the setup, or the accessories offered by different instrument vendors.

The desired signal performance is an overall flat frequency response with identical amplitude for low frequency (LF) and high frequency (HF) signal content. This is achieved by adjusting the BERT PG's EQ using a test pattern with sufficient and easily-observable HF and LF content. Therefore the pattern consists of 64 ones and 64 zeroes (a clock/128 representing the LF portion) followed by 64 bits of 1010 (a clock/2 representing the fundamental frequency of 4 GHz). The compliance pattern also contains such a section.

Figure 9a shows the non-ideal frequency response of the complete test setup at TP3. The HF pattern is about 0.5 dB down compared to the LF portion. Figure 9b shows the adjusted waveform. It is achieved by changing the setting of the de-emphasis post-cursor (Post-Cur1) on the N4903B/N4916B output until both the HF and LF signal amplitudes are identical and subsequently readjusting the output amplitude of the N4903B/N4916B to 800 mVpp (see Figure 10).



a) *b)*

Figure 9. Screenshot of a repetitive pattern of 64 ones, 64 zeroes, and 64 "1010"; a) amplitude of HF signal (clock/2) is a little bit too small compared to the LF signal (clock/128, 64 x 1 - 64 x 0); b) frequency response of the test setup properly compensated with -0.7 dB

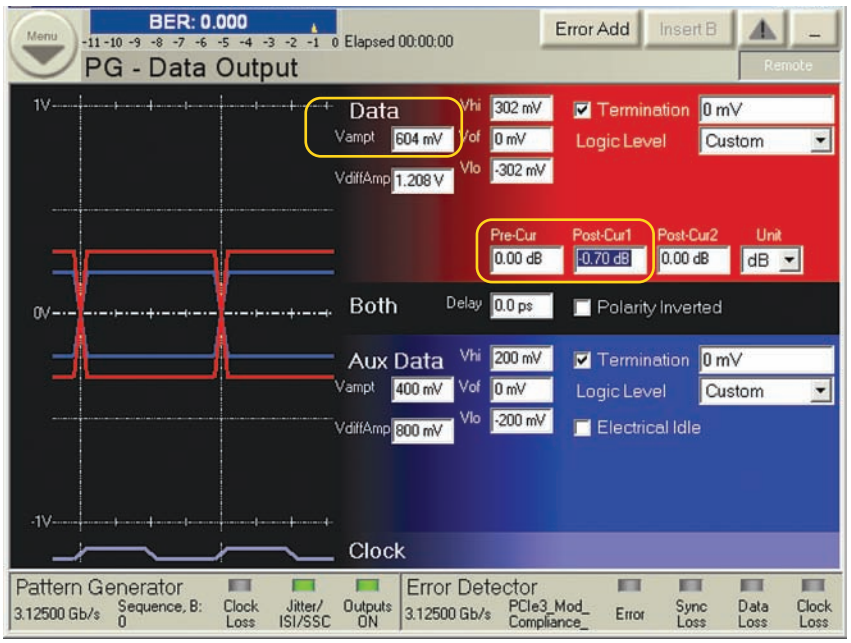


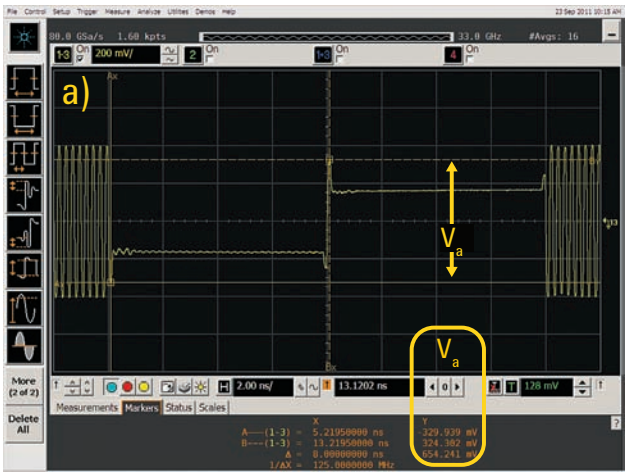
Figure 10. Data output set-up page of J-BERT: input fields for amplitude (Vampt) and EQ (Pre-Cur, Post-Cur1) are marked with the yellow boxes. Note that Post-Cur2 is not used for this application.

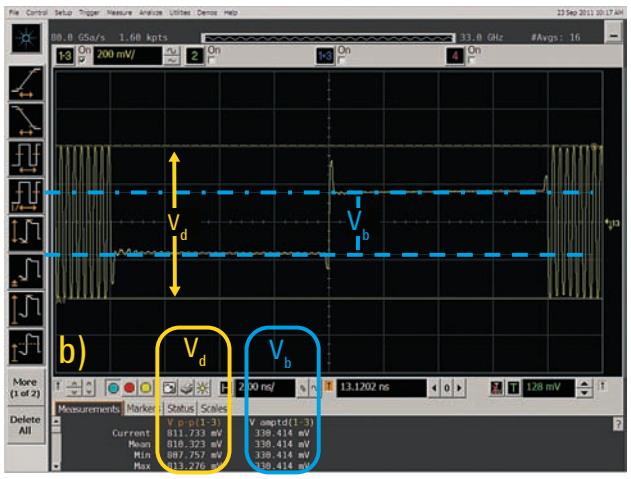
Amplitude readjustment is necessary because, per the rev. 3.0 definition, the amplitude relates to the maximum signal (the HF portion) while the LF signal is decreased, or de-emphasized. The Post-Cur1$_{de\text{-}embed}$ and Vampt$_{de\text{-}embed}$ values resulting from the above adjustment are recorded for later use. A summary of all relevant J-BERT settings is given in Table 1 at the end of Section 4.

3.4. Calibration of BERT PG equalization

During the RX tests several TX equalizations are emulated by the BERT PG. These are the presets P0, P7 and P8 and possibly an additional setting preferred by the DUT (see Section 5.4). The presets can easily be achieved with sufficient accuracy by relying on the N4916B's factory calibration and linearity. (See 2 below.) However, since the SEG recommends calibration of the BERT PG's EQ, the procedure is briefly described below [5]:

1. Configure the BERT PG to generate a suitable pattern, such as the one used for de-embedding of the test setup: 128 bits of clock/128 pattern followed by 64 bits of clock/2 pattern (see Figure 6).
2. Set the BERT PG to the specified values according to Table 5 taking the de-embedding value of PostCurs1$_{de\text{-}embed}$ into account:
   Pre-Cur = Pre-shoot, Post-Cur1 = De-emphasis + Post-Cur1$_{de\text{-}embed}$
3. Measure the voltages V_a, V_b, V_c, and V_d using oscilloscope measurements $V_{ampliude}$ for V_b and $V_{p\text{-}p}$ for V_d, and manual marker measurements for V_a and V_c as shown in Figure 11.
4. Determine the actual values for Pre-shoot and De-emphasis according to the following equations: De-emphasis = $20\log_{10} V_b/V_a$, Preshoot = $20\log_{10} V_c/V_b$, (Boost = $20\log_{10} V_d/V_b$).
5. Adjust the J-BERT's Pre-Cur and Post-Cur1 EQ settings until the desired De-emphasis and Pre-shoot is achieved.
6. If the amplitude is outside the specified window (see Table 3), re-adjust the maximum amplitude (V_d) to the specified value (800 $mV_{diff,pp}$) by varying V_{ampt} on the J-BERT and record all values determined above for later usage (see Table 1).





V_a [mV]	V_b [mV]	V_c [mV]	V_d [mV]
658	332	494	810
Pre-shoot de-emphasis boost			
Measured [dB]	3.45	-5.94	7.75
Ideal [dB]	3.5	-6.0	7.0

d)

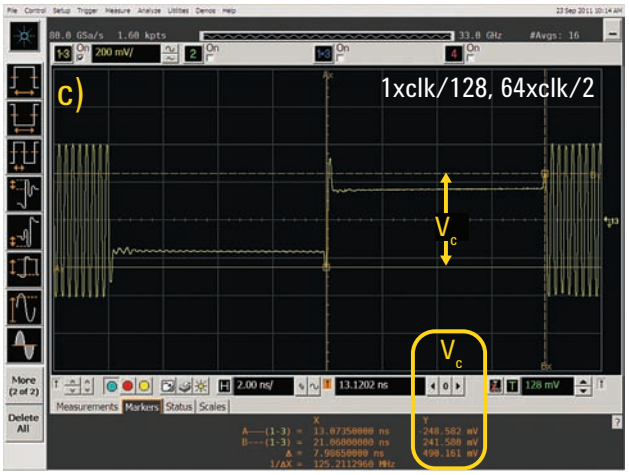


Figure 11. Screen captures showing waveforms measured to achieve desired BERT PG EQ for P7: a) marker setting and reading for V_c and b) V_a; c) automatic measurements for V_b and V_e; D) measurement results compared to desired/ideal setting

All possible PCIe rev 3.0 equalization settings and presets, as specified in the PCIe rev. 3.0 Base Specification, are listed in Table 4 and Table 5 respectively (see Section 7.3).

Note: It is important to use an oscilloscope with 20 to 25 GHz bandwidth (BW) to prevent artifacts caused by steep filters from making it difficult, if not impossible, to obtain a precise level measurement. A sampling oscilloscope typically does not present this difficulty.

4. Stress Signal Calibration

After calibration of the pattern generator's (PG) EQ has been achieved, the RJ, SJ and DM-SI need to be calibrated. The two jitter impairments are used to close the EW. EH closure is achieved by adding DM-SI, instead of reducing the BERT PG's amplitude. This method was chosen to emulate high frequency crosstalk from other lanes, which is amplified by the RX's CTLE relative to the low frequency signal content, degrading the HF-signal-to-noise ratio (SNR). The DM-SI frequency is therefore specified at 2.1 GHz, right in the pass-band of the CTLE.

For jitter decomposition and measurement the SEG provides the SigTest software tool to rule out discrepancies arising from proprietary jitter separation algorithms implemented in the oscilloscopes of different vendors. Stress signal calibration is done in two steps:

1. While the RJ and SJ parameters are (pre-) calibrated individually *before* the channel, the DM-SI amplitude is pre-calibrated *after* the channel, as the signal with its 2.1 GHz frequency is attenuated significantly (by approximately 10 dB) depending on the actual component- and channel-characteristics.
2. Next, fine adjustment of RJ and DM-SI is performed after the channel to achieve the desired eye opening at TP6 for a fully-stressed compliance pattern.

Calibration procedures for AIC and MB are identical, except for the use of a different channel configuration and SigTest template (see Table 3).

4.1. Calibration of RJ

RJ is calibrated using a 1010 (clock/2) pattern. (For J-BERT pattern set-up, see Figure 6). The RJ value on the J-BERT is set to a starting value slightly below the specified RJ value (see Table 3) with the appropriate 10 MHz high-pass filter turned on (see Figure 12).

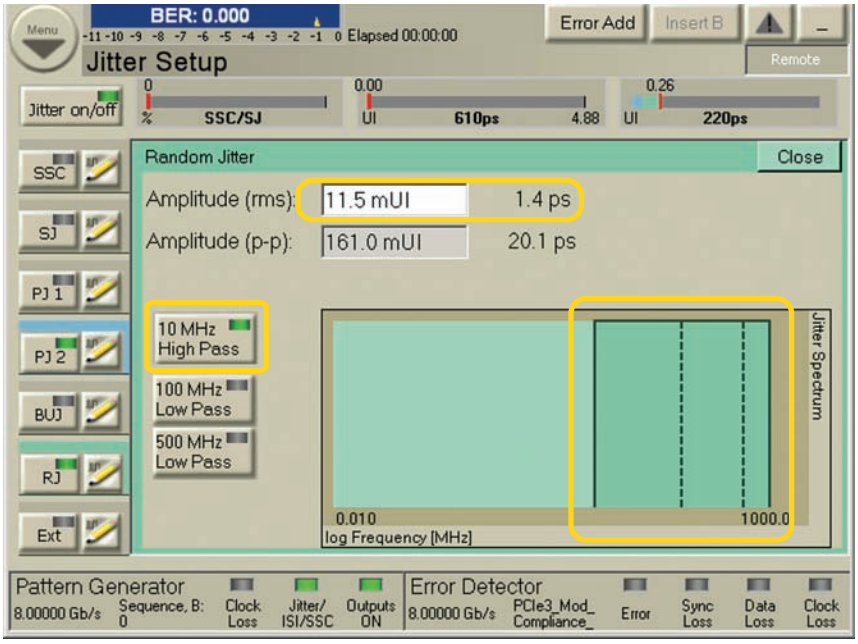


Figure 12. J-BERT jitter setup page, shown with detail for setup of RJ-BW

The waveform is recorded (10 million samples) and stored in .bin format, allowing it to be loaded into the SigTest software and the RJ to be calculated using the technology and template listed in Table 3. When using this template no equalization or embedding of any channel is performed. Therefore only the jitter results are relevant (see Figure 13).

This procedure is repeated with appropriate adjustments of the RJ value on the J-BERT until the RJ value calculated by SigTest is within the desired tolerance window (see Table 3). The last RJ value adjusted on the J-BERT has to be recorded manually as $RJ_{pre\text{-}adj}$ for later use (see Table 1).

Note: As the waveform files are relatively large it is advantageous to install the SigTest software on the oscilloscope's PC to avoid the time-consuming transfer of the waveform to another PC.

input panel

result panel

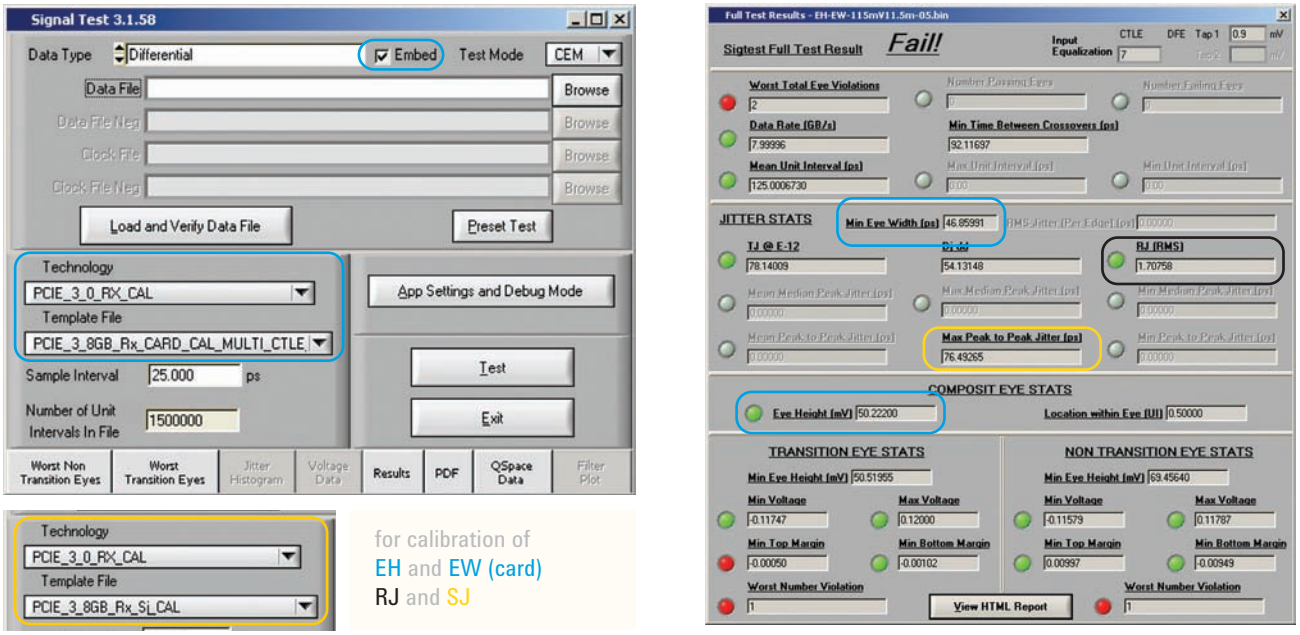
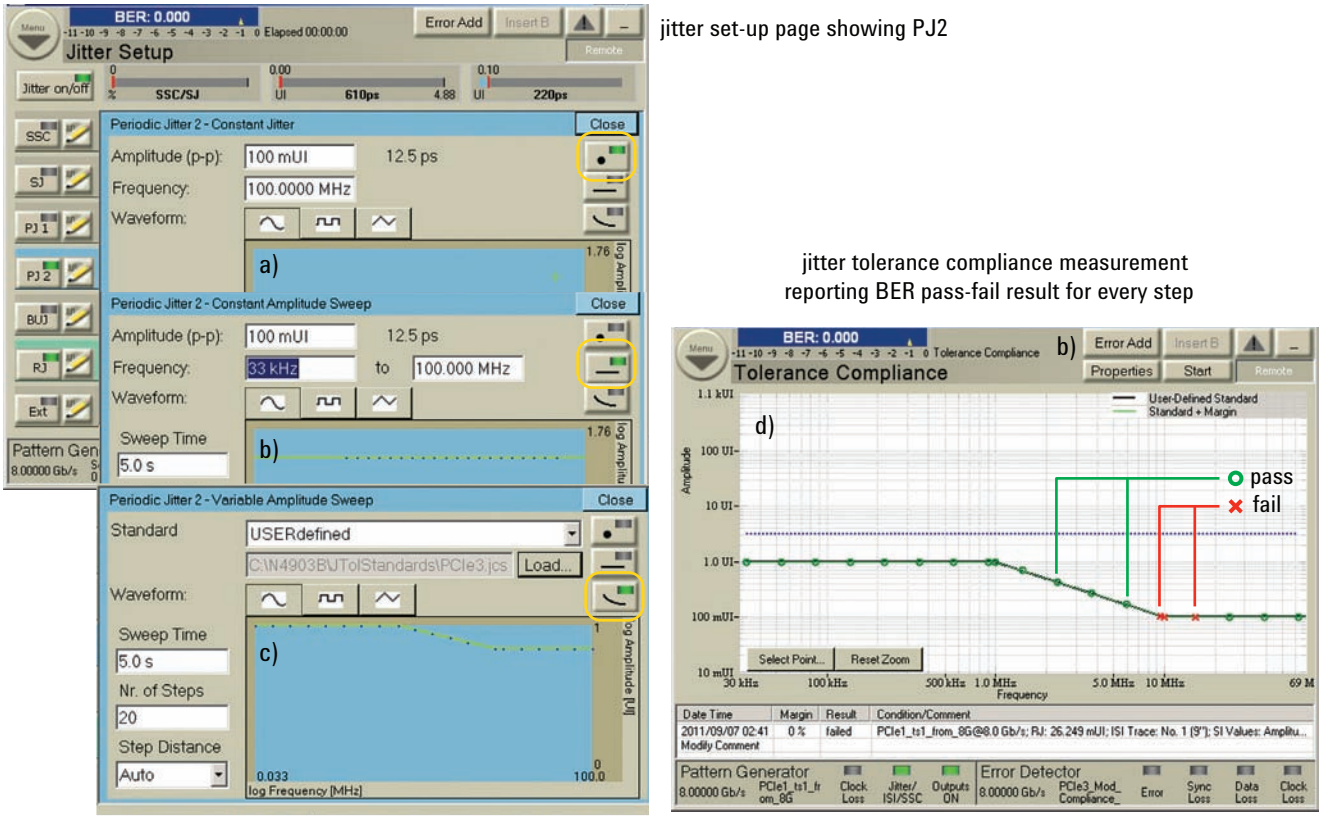


Figure 13. SigTest input panel upper left); technology and template shown on input panel used for final calibration (section 4.4); breakout on lower left shows alternative settings for jitter calibration (RJ and SJ); result screen (right); blue rectangle showing EH and EW results, black rectangle showing RJ results, orange rectangle showing peak-peak jitter results used for SJ calibration

4.2. Calibration of SJ

For the calibration of SJ the compliance pattern[1] is used (see Figure 6). The total intrinsic jitter (TJ) is measured for reference. For this purpose all jitter sources of the J-BERT as well as the DM-SI are turned on and set to zero. The waveform is then captured, stored in .bin format, loaded into the SigTest software, and used to determine TJ_0 ("Max Peak to Peak Jitter2", as shown in Figure 13). For the generation of SJ, either J-BERT's PJ1 or PJ2 can be used. Selecting PJ2 is advantageous if characterization beyond compliance test using a frequency sweep similar to the base specification is desired (see Figure 14).

For calibration, PJ2 is set to 0.1 UI at 100 MHz (see Figure 14). Next the waveform is captured and SigTest calculates the jitter values. The difference in TJ between the reference measurement (TJ0) with all jitter sources set to zero and the current measurement, is equivalent to the injected SJ. If the SJ is not within the specified window (see Table 3), then the amount of periodic jitter (PJ) on the J-BERT is adjusted and the procedure is repeated until a suitable setting for PJ_{cal} is obtained (see Table 1).



jitter set-up page showing PJ2

jitter tolerance compliance measurement reporting BER pass-fail result for every step

Figure 14. Screen captures from the J-BERT graphical user interface (GUI) showing set-up of a) PJ2 with constant value or b) linear background sweep and c) sweep according to predefined curve; d) the jitter tolerance compliance measurement

1. *Compliance pattern and modified compliance pattern are available with J-BERT software revision 7.1 or higher.*

4.3. Calibration of DM-SI

The last impairment to be (pre-) calibrated is the DM-SI, which is used to adjust the EH. This parameter is measured after the channel at TP6 (see Figure 8). For this purpose the CLB is inserted into the CBB main board, and the SMP connectors of cable ① are removed from the oscilloscope and connected to the RX connectors on the CBB-riser card for AIC tests, or on the CLB for MB tests. The additional pair of matched SMP-SMA cables ② (see Figure 8 and Table 2) is connected from the TX connectors of the CLB for AIC tests, or the CBB-main board for MB tests, to the input of the oscilloscope, removing the SMP-SMA adapters.

The BERT PG is set to generate a pattern of constant zeroes, which is easily achieved with J-BERT's pattern sequencer using a "Pause" segment (see Figure 6). The DM-SI is set to a frequency of 2.1 GHz and its amplitude is varied until the peak-peak amplitude measured on the oscilloscope is within the tolerance window specified in Table 3. The DM-SI$_{pre\text{-}cal}$ value is found and recorded for later use (see Figure 15 and Table 1).

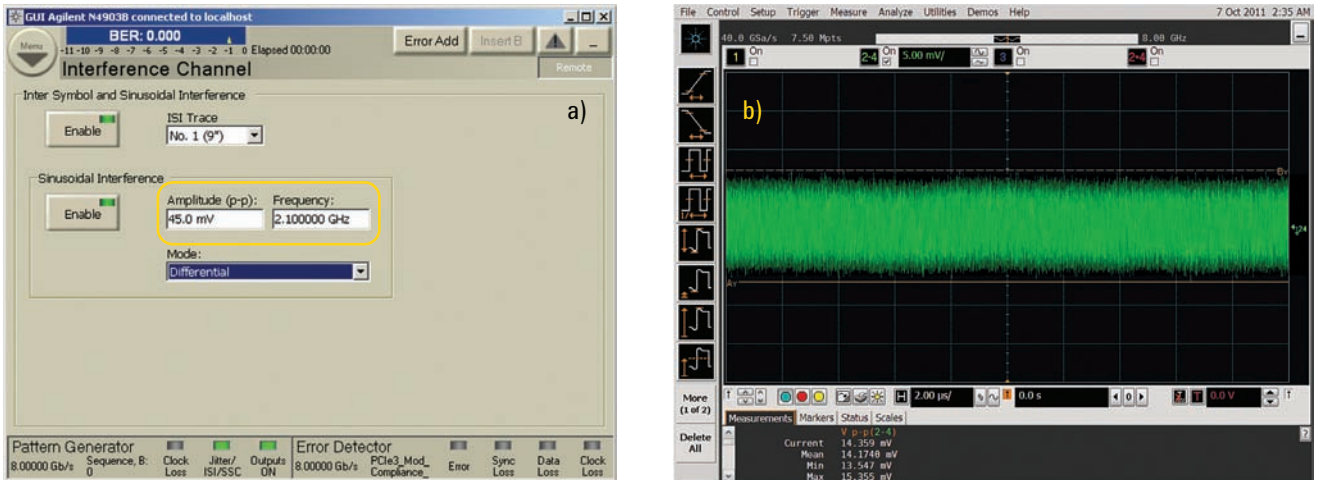


Figure 15. J-BERT a) setup screen for DM-SI and b) screen capture showing waveform

4.4. Final stress signal calibration, EH and EW

Now that all impairments and presets have been (pre-) adjusted, the final stress signal adjustment must be achieved. For this purpose P7 (see Table 5) and the compliance pattern is selected, and all relevant J-BERT parameters (amplitude, and voltage and timing impairments) are set to the values recorded above. The waveform is captured after the channel using an oscilloscope and then loaded into the SigTest software. The calculations are done using the SigTest technology and template listed in Table 3. Using these templates, SigTest embeds the remaining portion of the channel ("Embed" must be checked on the SigTest input panel before pressing "Upload and Verify Data", see Figure 13) and optimizes the reference equalization for the CTLE and the DFE. This optimization is necessary since the eye opening is specified inside the ASIC (see TP2-P Figure 3 and Figure 8). If the calculated values for EH and EW are not within the limits specified in Table 3, RJ and DM-SI should be changed accordingly:

1. Adjust RJ to meet specified EW
2. Adjust DM-SI to meet specified EH
3. Re-check EW and if necessary re-adjust RJ
4. Record the final calibration values RJ_{cal} and $DM\text{-}SI_{cal}$ for later use

Typical values of all relevant parameters for AIC calibration are listed in Table 1. Nevertheless in-situ adjustments are necessary since the J-BERT settings depend on the properties of passive components and instruments used in the actual test setup.

	De-embed	P7	P8
Vampt/mV	604	604	604
Pre-curs/dB	0	4.1	4.1
Post-cur1/dB	-0.7	-4.5	-7.1
	Pre-adjust	Final adjust (EW/EH)	
RJ/mUI (ps)	11.5 (1.44)	11.5 (1.44)	
PJ2	110 (13.8)	110 (13.8)	
DM-SI/mV	45	110	

Table 1. Typical J-BERT settings to achieve a calibrated RX stress signal. Values in the actual setup may vary because of differences created by the actual components used.

4.5. Agilent N5990A-101

To achieve proper calibration, a number of parameters have to be adjusted, some of them iteratively. Automation of this process is easily done using the Agilent Technologies N5990A automated compliance and device characterization test software with Option 101 PCI EXPRESS®. The latest version of the N5990A will include the calibration procedure for revision 3.0 CEM tests according to the PHY test specification. The calibration achieved with the N59990A-101 is valid for a much wider range than just the compliance point. This enables users to run a test at the specified compliance point, do characterization finding DUT margins, and analyze specific problems.

Summary of the calibration procedure

The relatively high transfer rate of 8 GT/s and the way the PCI-SIG boards are designed (emulating the TX package) has several impacts on stress signal calibration:

- The test setup's frequency response (up to TP3) has to be de-embedded to eliminate major differences between test equipment from different vendors.
- All signal parameters including amplitude, EQ, jitter, and voltage noise, have to be calibrated in-situ.
- Jitter values are extracted from captured waveforms using the SigTest software to eliminate the subtle differences between proprietary extraction algorithms of different oscilloscopes.
- The stress signal cannot be defined by individually calibrated ingredients – most of them are only pre-calibrated individually, while the final calibration of the stress signal is done varying RJ and DM-SI to achieve the desired EH and EW.
- The SigTest software is used to determine EH and EW, providing equalization as the stress signal is defined inside the RX behind the reference EQ.
- A practical setup with the Agilent J-BERT has been discussed.
- Use of Agilent N5990 automation software Option 101 is recommended.

5. RX Tests

In this section the two test setups and a tool for training the DUT into loopback are described. Some generic aspects of the nature of BER measurements and statistics are also discussed.

5.1. Test setup for AICs

The source output cables ① (see Figure 8 and Figure 16) are connected to the SMP RX connectors on the CBB riser card. The AIC under test is inserted into the PCIe connector of the CBB main board. J-BERT's trigger output is set to divide by 80 in order to generate a 100 MHz reference clock. The output is connected to the SMP-Ref-Clk input connectors and the error detector (ED) input is connected via cables ② to the SMP-TX connectors of the CBB main board as shown in Figure 16.

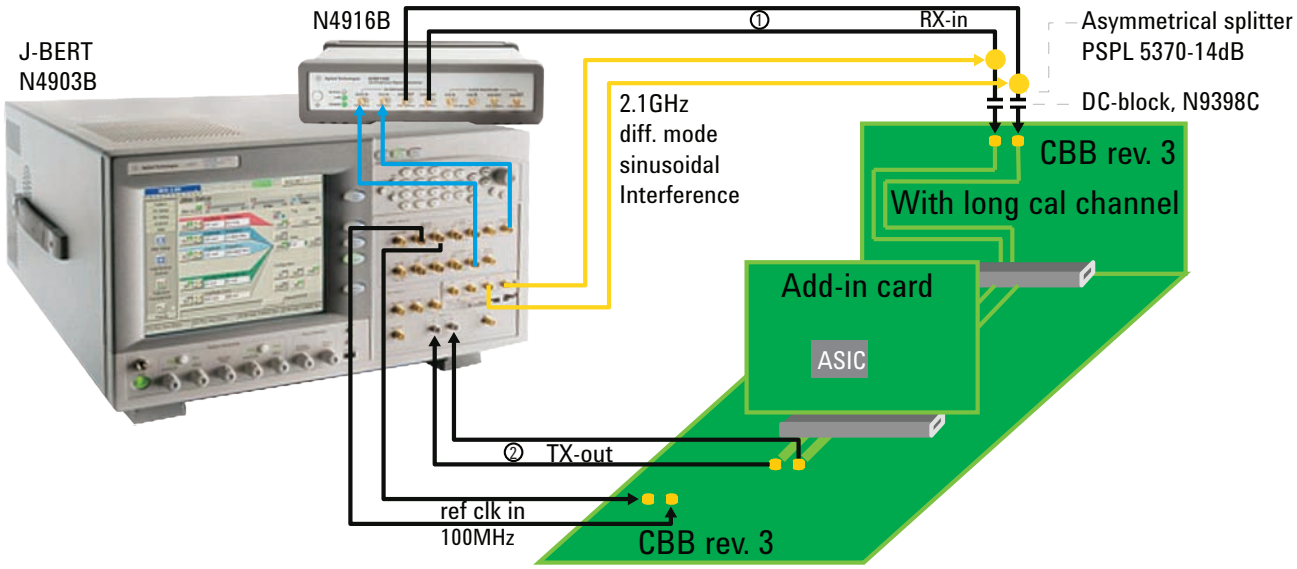


Figure 16. Test setup for AIC using the Agilent J-BERT N4903B and N4916B de-emphasis signal converter plus CBB riser card

5.2. Test setup for MBs

For MB test the source output cables ① (see Figure 8 and Figure 17) are connected to the SMP-RX connectors and the ED input to the SMP-TX connectors of the CLB. Most MB's cannot run on an external 100 MHz reference clock. Therefore J-BERT's PG is set to external clock mode. The clock input is driven by the N4880A reference clock multiplier phase-locked loop (PLL), which converts the 100 MHz reference clock into an 8 GHz clock for J-BERT's external clock input, while conserving all in-band jitter according to PCIe specification, especially spread spectrum clocking (SSC) modulation.

As shown in Figure 17 and listed in Table 2 a signal repeater for eye-opening is necessary, to open up the signal eye of the MB's backchannel TX. This can be the case even when suitable TX equalization was requested by J-BERT during link training (see Section 5.3).

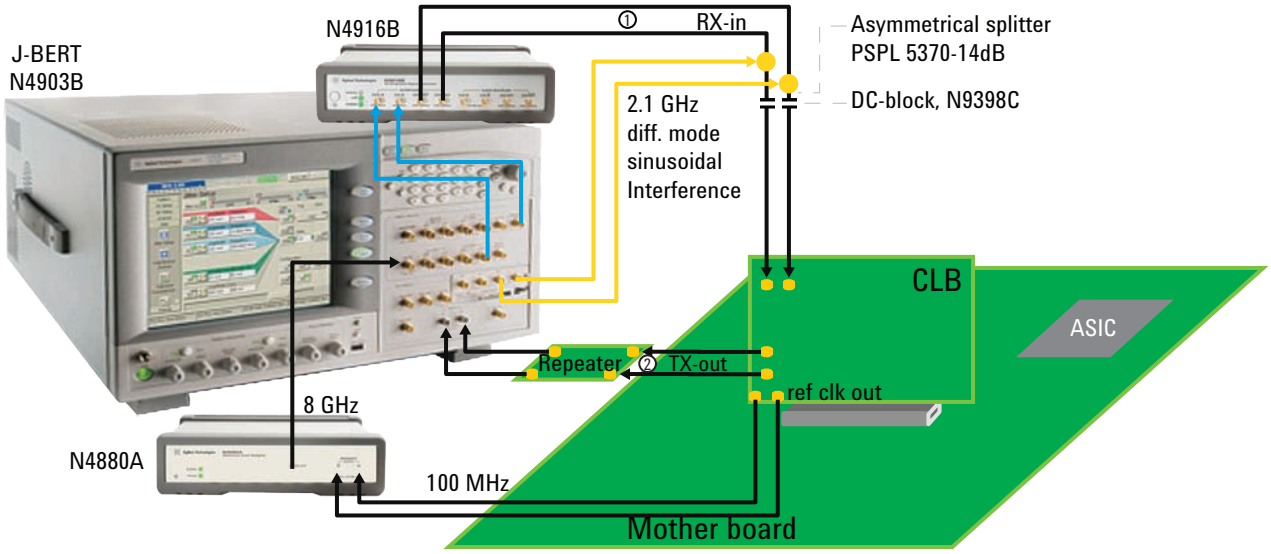


Figure 17. Test setup for MB with J-BERT N4903B, N4916B de-emphasis signal converter, and the N4880A reference clock multiplier plus CLB

5.3. Setting the DUT into loopback

In order to perform the RX test it is necessary to train the DUT into loopback (see Section 2.1). To achieve this, J-BERT has to steer the DUT through the states of the link training status state machine (LTSSM) as depicted in Figure 18. The minimum speed that any PCIe device can handle is 2.5 GT/s. Therefore the initial communication between the link partners is performed at a transfer rate of 2.5 GT/s stepping through <Polling> to <Configuration> (marked with the yellow arrow in Figure 18). Both devices then go into electrical idle and perform the speed change to 8 GT/s (highlighted by yellow/black arrow in Figure 18, and described in the sidebar). Just from now on after entering the loopback state does J-BERT send out the specified pattern at 8 GT/s, which moves the DUT from the "<loopback-entry> state to <loopback>.

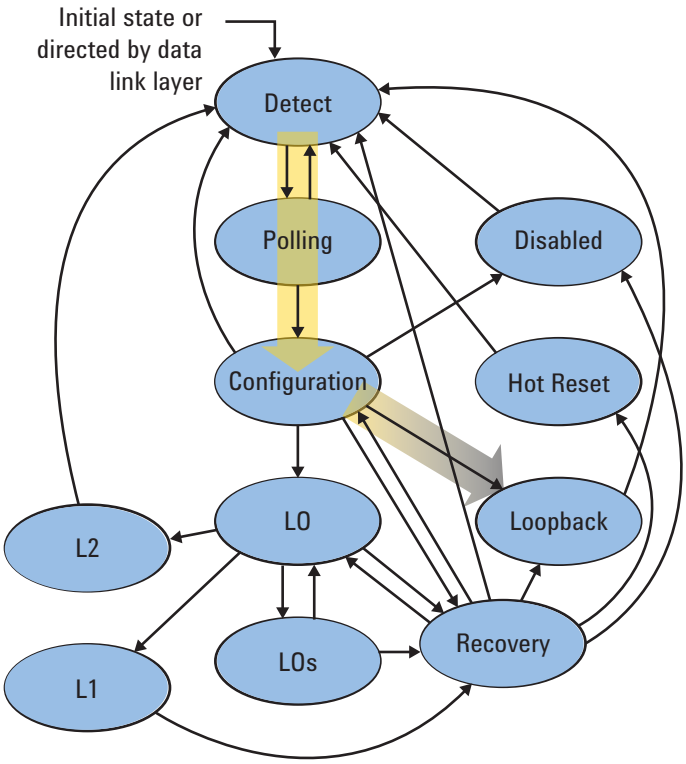
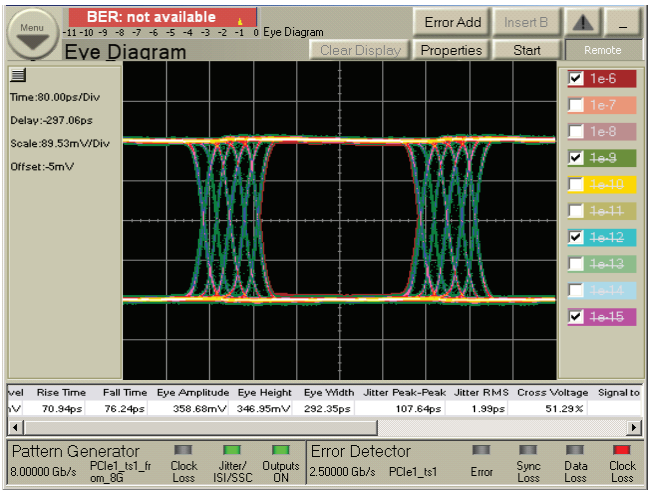


Figure 18. LTSSM and path to loopback

Bit multiplication is used to generate a 2.5 GT/s pattern while the BERT is running at 8 GT/s speed. As there is no integer divider between the two rates an asymmetric scheme is used: four times 3 bits and one time 4 bits are transmitted achieving the ratio of 16 bits / 5 bits = 8 GT/s / 2.5 GT/s. This asymmetrical bit multiplication inevitably generates jitter in 2.5 GT/s mode. However this jitter only occurs during link training and is below the PCIe 1.0 specification limits leaving a safe margin.



8 GT/s signal

Ratio 8/2.5 = 16/5 = 3.2

2.5 GT/s signal

Emulating a 2.5 GT/s signal

of 8 GT/s bits / 2.5 GT/s bit

Specified eye opening for 2.5 GT/s

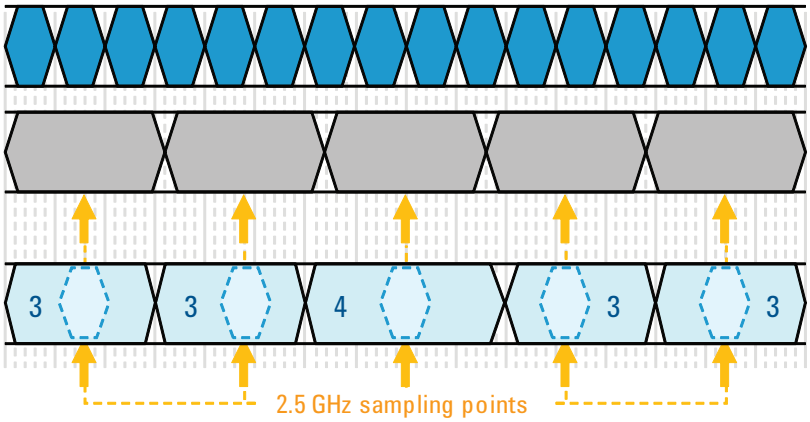


Figure 19. 2.5 GHz pattern

The standard conformance pattern sequence that sets the device into loopback with effectively two different transfer rates, 8B/10B coding for 2.5 GT/s and 128B/130B coding, and partial scrambling at 8 GT/s, is relatively complex. This pattern is provided with the Agilent J-BERT software revision 7.1 or higher. However, with the CEM and PHY test specifications still under development, not all pre-release devices have a standard-conformant LTSSM. The sequence provided with J-BERT although fully compliant with the base specification, might not always work. Therefore Agilent provides the N5990A Option 301 link training suite (LTS), which allows the sequence to be edited on a user-selectable abstraction level as shown in Figure 20. After setting up the link training sequence and its parameters, the bit patterns and sequence created by the LTS, including the selectable repeating test pattern for loopback, can be downloaded to J-BERT PG and ED.

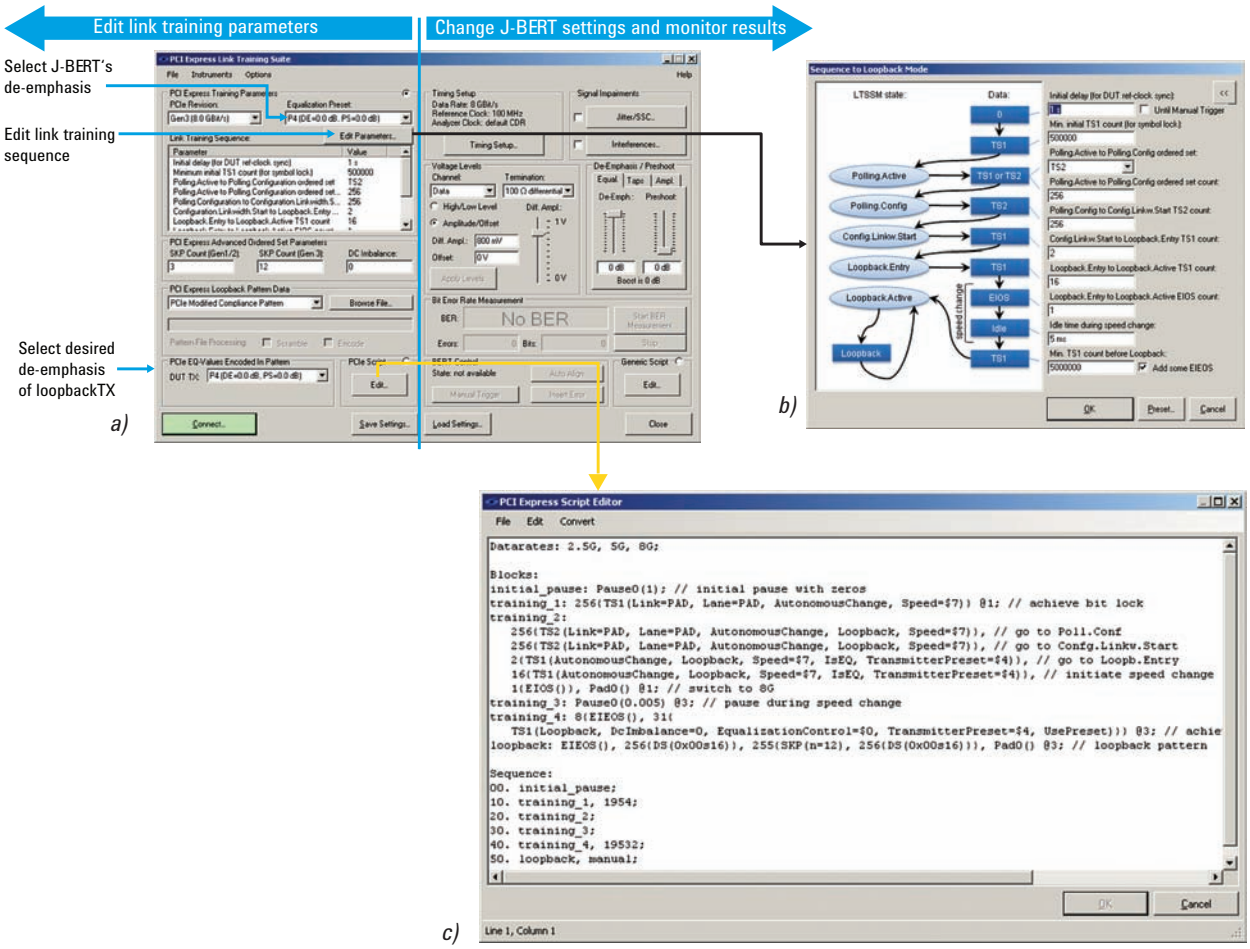


Figure 20. Different GUIs of the Agilent link training suite allow editing of the sequence and patterns on a user-selectable level. a) main GUI with J-BERT parameter editor, b) high-level editor for pattern sequence, c) script language editor

5.4. Actual RX tests and measurement time

There are two types of tests. The first type is used to verify that in final system the TX-RX pairs can establish a minimum communication in order to exchange their properties. It is also used to verify that when running at maximum common speed the devices can train each other for optimal BER performance. This makes it necessary to verify that for the specified TX EQ presets P0, P7 and P8 the BER is better than 10^{-4} (see Table 5). The second test is the RX jitter tolerance test. It is used to verify RX operation with BER better than 10^{-12}. For this test the EQ of J-BERT PG is set to that preset, or any of the defined EQ settings as specified in Table 4, which is required by the DUT.

Note: This PG EQ is not necessarily the same EQ that would result from an interactive link training in recovery state; the PG EQ mentioned here is a setting that has been predetermined by the designers or test engineers of the PCIe-ASIC or card under test.

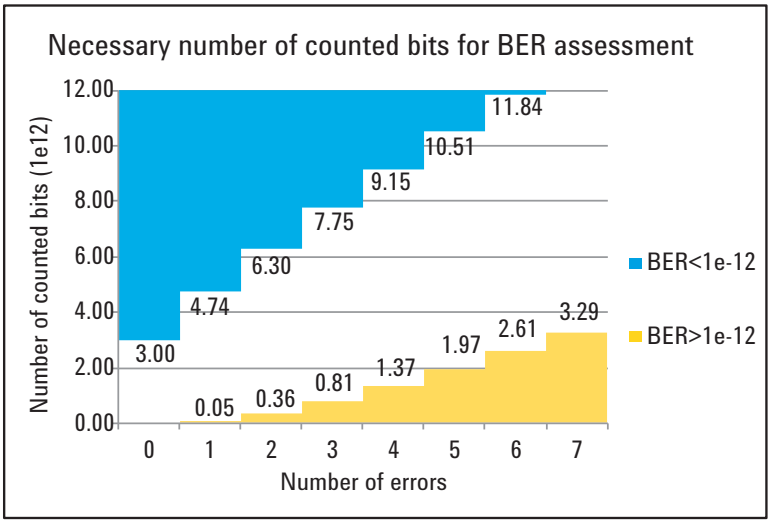
For both types of test the DUT is stimulated with the calibrated stress pattern and the BERT-ED counts received bits and errors to determine the BER.

A question that arises is what is the necessary measurement time or how many bits have to be observed to achieve a BER-measurement with a sufficient confidence level (CL). For the usual CL = 95% the necessary number of bits is shown in Figure 21. By the laws of statistics it is not possible to determine the DUT's BER to a precise value; with a given CL it can only be determined that the BER is above or below a certain threshold [6]; the latter is exactly what we are trying to determine.

For the first type of test it would only be necessary to measure a very small number of bits (such as 3 x 10^4 for zero errors or 10^5 bits for up to 5 errors) to achieve a confidence level of 95% for the target BER, see Figure 21A, but for practical reasons such as the update frequency of BER measurement of common BERTs, bits in the order of 10^9 will be measured.

The observed number of bits and errors to achieve the desired confidence level in the BER result is much more important for the second type of test. The minimum measurement time for the transfer rate of 8 GT/s verifying the BER < 10^{-12} with CL = 95% is 6' 15" without an error occurring during this test period.

a)



b)

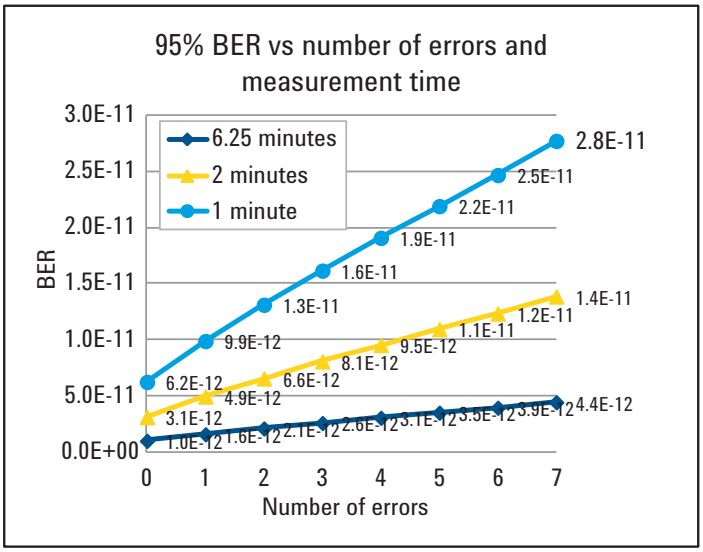
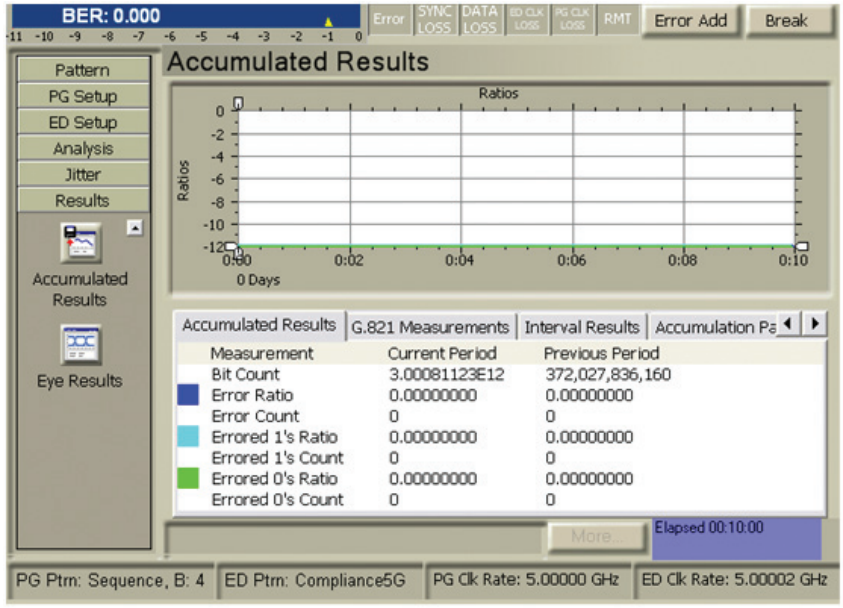


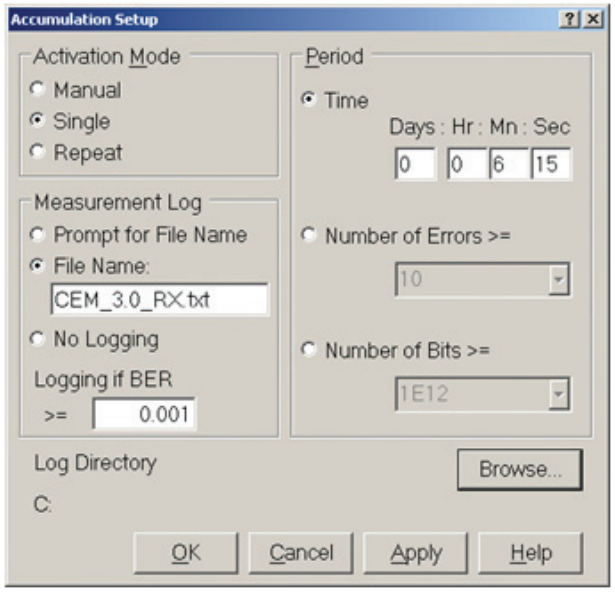
Figure 21. a) BER versus the number of errors and number of measured bits; b) achievable BER at a given measurement time

Figure 22 shows the J-BERT screen capture of the accumulated BER results on the J-BERT GUI, which is handy for performing RX testing. When a BER < 10^{-12} must be achieved, it is not possible to determine the measurement time up front since it depends on the number of errors that occur (Figure 20a). When software automation is not used, this screen allows the accumulated number of errors to be checked occasionally only after meaningful timeframes (6'15", 10', 13', 16', ...), and eliminates the need to continuously watch the current BER results and identify any errors.

Alternatively, it is possible to predefine the measurement time and determine the DUT's BER depending on the number of accumulated errors (see Figure 21b).



(a)



(b)

Figure 22. a) J-BERT accumulated bit errors result and b) setup screen

6. Summary

The calibration procedure for the RX stress signal has been discussed. A practical, complete, and workshop-proven test setup using Agilent equipment has been shown to adhere to the CEM Specification. The advantages of the Agilent offering have been demonstrated:

- J-BERT's pattern sequencer makes it convenient to setup and switch between the different patterns required during the calibration
- N5990A Option 301 link training suite allows the setup of the pattern sequence on a user-selectable abstraction layer to steer the DUT through the LTSSM into loopback on a user-selectable abstraction layer
- N5990A Option 101 automation software performs calibration beyond the compliance point for a wide range of stress signal parameters, allowing characterization measurements to determine the DUT's margin
- Overall, using the Agilent equipment saves setup time, allows deeper insight and is PCI-SIG workshop-proven. Beyond the methods and setup for CEM testing described in this application note, Agilent offers complete setup and automation software for calibration and test according to the Base Specification [4].

Note: This application note is based on preliminary versions of the CEM and PHY Test Specification. Parameter values and test procedures are subject to change.

7. Appendix

7.1. Equipment

The required instruments and accessories for building the test setups are listed in Table 1.

Description	Number/Option	Qty
J-BERT high-performance serial BERT	N4903B	1
12.5 Gb/s BERT	N4903B-C13	1
PJ, SJ, BUJ, RJ, s-RJ injection	N4903B-J10	1
SSC generation	N4903B-J11	1
Interference channel (ISI, S.I.)	N4903B-J20	1
Jitter tolerance compliance suite	N4903B-J12	1 (R[1])
AUX DATA output with PRBS and pattern	N4903B-002	1 (R[1])
Bit recovery mode	N4903B-A01	1 (R[1])
De-emphasis signal converter	N4916B-STD	1
Matched cable kit for connecting N4916B with N4903B	N49156-010	1
Reference clock multiplier	N4880A	1
Digital signal analyzer with 13 GHz or higher bandwidth	DSAX91604A or higher	1
Test automation software platform core product	N5990A- 010	1
PCIe receiver test, includes SEASIM software	N5990A- 101	1
Link training suite	N5990A Option 301	1
Accessories		
Pair of SMA cables, matched ±25 ps	15443A	1
PICKOFF TEE, 14 dB (5X), SMA J-P-J	PSPL 5372-112 14dB	2
DC block, 50 kHz to 26.5 GHz	N9398C	2
SMA-SMP cable pairs	N4235-61602	3
SMP ➔ SMA adapter	Pastenack PE9511	2
PCI-SIG CBB (main and riser card) + CLB	PCI-SIG	1
Repeater	National Semiconductor DS80PCI800EVK	1 (MB[2])

1. *R: Item not required to perform the basic measurements as described within this application note, but recommended because they are helpful during day-to-day work.*
2. *MB: Only necessary for motherboard test*

Table 2. Equipment for Figure 8 test setup

7.3 Specifications for RX-stress signal according to CEM 0.9 and PHY test specification version. 0.5

Parameter	Min	Max	Unit	Sig test	
				Technology	Template
Vpp		800	mV	N/A	N/A
$V_{RX-EH-BG}$ eye height		50	mV	PCI_3_CARD	PCI_3_8GB_MULTI_CTLE_DFE_80ps_50mV
$T_{RX\ BH\ 8C}$ eye width		0.36 (45)	UI (ps)	PCI_3_CARD	PCI_3_8GB_MULTI_CTLE_DFE_80ps_50mV
R_j (random jitter)	1.5	1.6	ps RMS	PCI_3__0_RX_CAL	PCIE_3_8G_Rx_Sj_CAL
S_j (sinusoidal jitter) 100 MHz	12.5	14.5	ps PP	PCI_3__0_RX_CAL	PCIE_3_8G_Rx_Sj_CAL
Differential mode sinusoidal interference at 2.1 GHz	14	15	mV PP	N/A	N/A

Table 3. PHY test specification for RX test

7.4 TX equalization and presets

PS	DE	C_{+1}																	
	Boost	0/24		1/24		2/24		3/24		4/24		5/24		6/24		7/24		8/24	
C_{-1}	0/24	0.0	0.0	0.0	-0.8	0.0	-1.6	0.0	-2.5	0.0	-3.5	0.0	-4.7	0.0	-6.0	0.0	-7.6	0.0	-9.5
		0.0		0.8		1.6		2.5		3.5		4.7		6.0		7.6		9.5	
	1/24	0.8	0.0	0.8	-0.8	0.9	-1.7	1.0	-2.3	1.2	-3.9	1.3	-5.3	1.6	-6.8	1.9	-8.8		
		0.8		1.6		2.5		3.5		4.7		6.0		7.6		9.5			
	2/24	1.6	0.0	1.7	-0.9	1.9	-1.9	2.2	-3.1	2.5	-4.4	2.9	-6.0	3.5	-8.0				
		1.6		2.5		3.5		4.7		6.0		7.6		9.5					
	3/24	2.5	0.0	2.8	-1.0	3.1	-2.2	3.5	-3.5	4.1	-5.1	4.9	-7.0						
		2.5		3.5		4.7		6.0		7.6		9.5							
	4/24	3.5	0.0	3.9	-1.2	4.4	-2.5	5.1	-4.1	6.0	-6.0								
		3.5		4.7		6.0		7.6		9.5									
	5/24	4.7	0.0	5.3	-1.3	6.0	-2.9	7.0	-4.9										
		4.7		6.0		7.6		9.5											
	6/24	6.0	0.0	6.8	-1.6	8.0	-3.5												
		6.0		7.6		9.5													

Min reduced swing limit

Full swing limit or max reduced swing limit

Table 4. List of all specified TX equalization settings

Preset number	Preshoot		De-emphasis		Va/mV	Vb/mV	Vc/mV
	(dB)	Tol: ± dB	(dB)	Tol: ± dB	@ Vd = 800 mV		
P4	0		0		800	800	800
P1	0		-3.5	1	800	534	534
P0	0		-6	1.5	800	400	400
P9	3.5	1	0		534	534	800
P8	3.5	1	-3.5	1	600	400	600
P7	3.5	1	-6	1.5	640	320	480
P5	1.9	1	0		640	640	800
P6	2.5	1	0		600	600	800
P3	0		-2.5	1	800	600	600
P2	0		-4.4	1.5	800	480	480

Table 5. List of presets

7.5 References

[1] PCIe Base Specification rev. 3

[2] PCIe CEM Specification rev. 3

[3] PCIe PHY Test Specification rev. 3

[4] Accurate Calibration of Receiver Stress Test Signals for PCI Express® rev. 3.0 , Application Note, literature number 5990-6599EN (http://cp.literature.agilent.com/litweb/pdf/5990-6599EN.pdf)

[5] Digital Communications Test and Measurement; Dennis Derickson-Marcus Mueller; Prentice Hall

[6] Total Jitter Measurement at Low Probability Levels, Using Optimized BERT Scan Method, literature number 5989-2933EN (http://cp.literature.agilent.com/litweb/pdf/5989-2933EN.pdf)

7.6. Glossary

AIC	Add-in card
ASIC	Application-specific integrated circuit
BER	Bit error ratio
BERT	Bit error ratio tester
BERT PG	Bit error ratio tester pattern generator
BUJ	Bounded uncorrelated jitter
BW	Bandwidth
CBB	Compliance base board
CEM	Card electro-mechanical (the PCI-SIG standard which describes the specifications for add-in cards and motherboards using PCIe interfaces)
CL	Confidence level
CLB	Compliance load board
CR	Clock recovery
CTLE	Continuous time linear equalizer
DDJ	Data dependant jitter
DFE	Decision feedback equalizer
DM-SI	Differential mode sinusoidal interference
DUT	Device under test
ED	Error detector
EH	Eye height
EQ	Equalizer
EW	Eye-width
EWG	Electrical Work Group
GUI	Graphical user interface
HF	High frequency
ISI	Inter-symbol interference
LF	Low frequency
LTS	Link training suite
LTSSM	Link training and status state machine
MOI	Method of implementation
MB	Motherboard
PCI	Peripheral component interconnect
PCIe	PCI-EXPRESS
PCI-SIG	PCI Special Interest Group
PG	Pattern generator
PHY	Physical layer or Physical layer device
PLL	Phased-locked loop
PJ	Periodic jitter
RJ	Random jitter
RX	Receiver
Seasim	Statistical eye analysis simulator
SEG	Serial enabling group
SIG	Special interest group
SNR	Signal-to-noise ratio
SigTest	Signal test (software provided by PCI-SIG to members for signal analysis of TX output signals or calibration of RX test signals)
SJ	Sinusoidal jitter
TJ	Total jitter
TX	Transmitter
UI	User interface

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