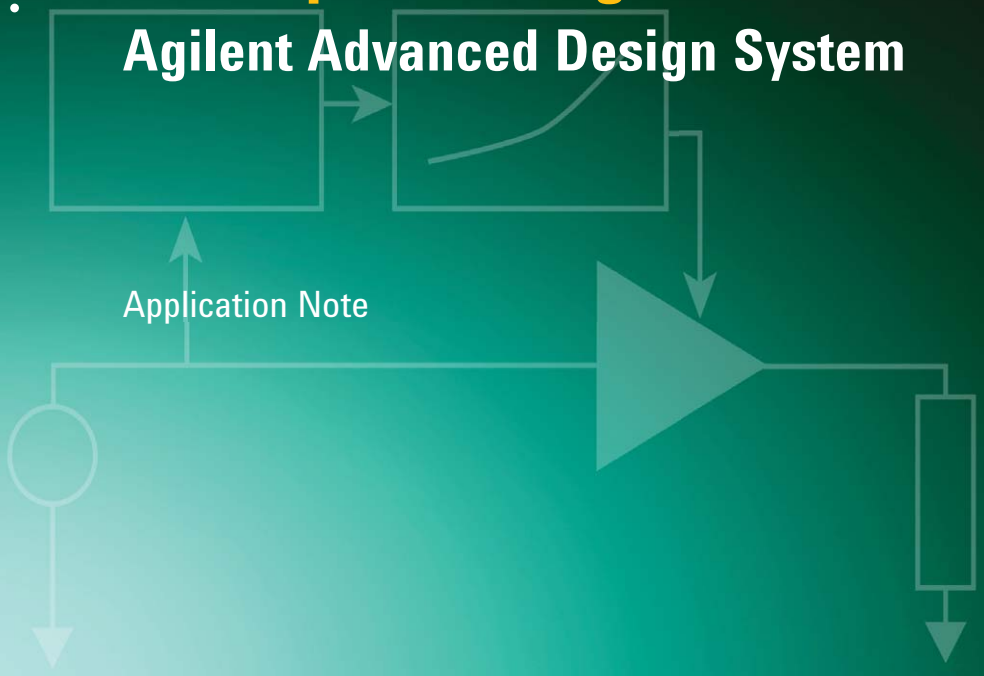
Simulating Envelope Tracking with Agilent Advanced Design System

Application Note



1.0 Introduction

Modern modulated signals often have high peak-to-average power ratios (PAPR). Use of such high PAPR signals results in power amplifiers (PAs) having to operate at a large back-off when stringent linearity requirements must be satisfied. Operating a PA at relatively high output power back-off ensures the signal is not greatly distorted when its envelope excursion is near its peak. However, the greater the amount of back-off, the lower the PA's efficiency.

A power amplifier with a fixed drain bias may have high power-added efficiency (PAE), but only at a high output power (the red trace in Figure 1.) The power amplifier with the PAE-versus-output power characteristic shown in this figure would have to be operated in back off (thus with low PAE) to avoid distorting the signal.

One way to bolster low efficiency in the back-off region is to use Envelope Tracking (ET), a technique that allows the amplifier's drain bias to track the magnitude of the input signal envelope. When the input signal envelope is low, the drain bias can be reduced so the amplifier operates closer to its optimal efficiency point.

If we could dynamically adjust the drain bias to lower values when the input signal is lower, we can operate the power amplifier at a higher level of efficiency (Param1 is the drain bias), as shown if Figure 2.

More information about Envelope Tracking is available at: ***www.open-et.org***

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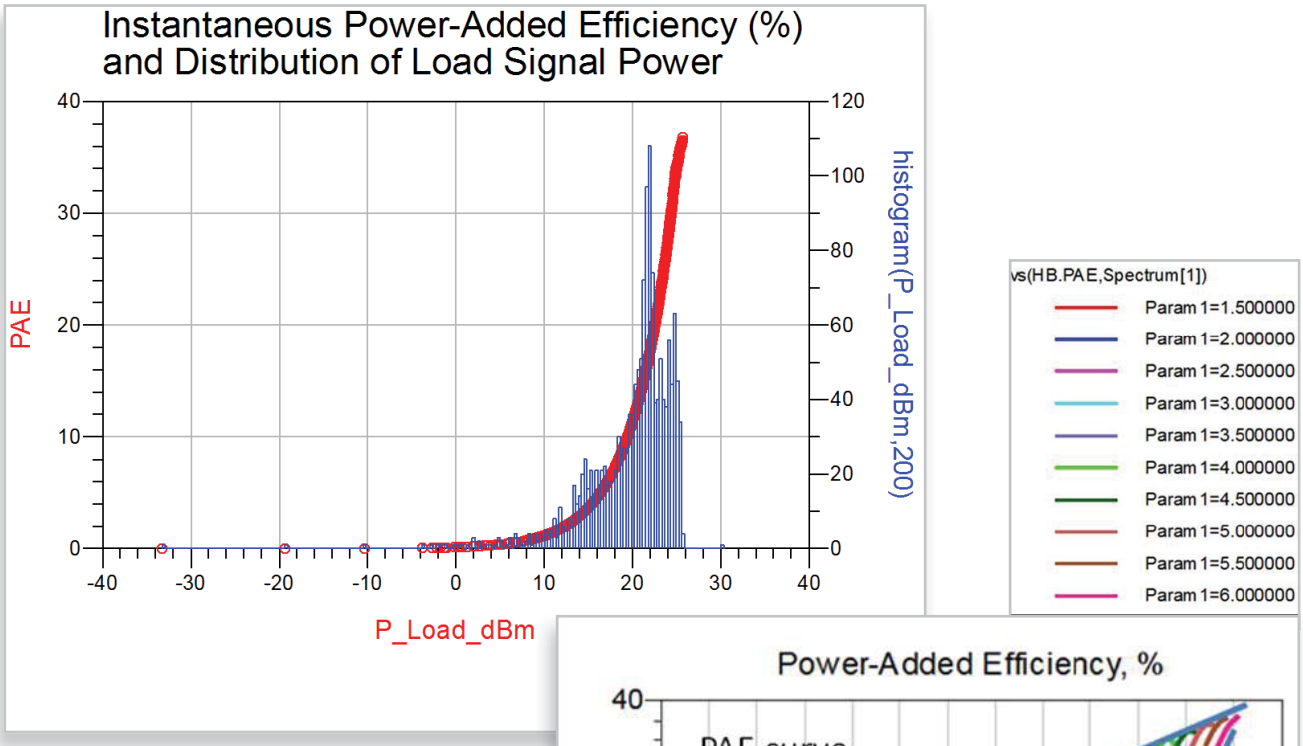

Figure 1. This power amplifier must be operated in back off (where PAE is low) to avoid compressing and distorting a high-PAPR signal.

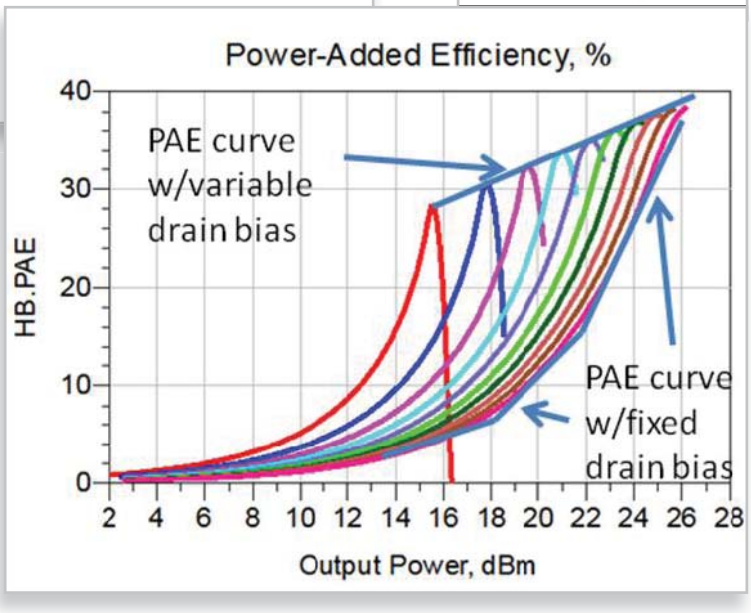

Figure 2. Higher PAE can be attained if the PA's drain bias can be adjusted dynamically along with the input signal magnitude.

This application note details a method for applying ET to a PA. The method employs Agilent's Advanced Design System (ADS) software to perform the necessary simulations. Agilent's 89600 Vector Signal Analysis (VSA) software can be used to display the simulation results. This example, along with another one highlighting the application of ET to a PA specifically designed for narrow-band modulation, is available on the Agilent EEsof Knowledge Center at: ***http://edocs.soco.agilent.com/display/eesofkcads/Applying+envelope+tracking+to+Improve+Efficiency***. In the latter example, the presence of wideband modulation causes the PA to exhibit memory effects likely due to the bias network. The simulation setups in these examples don't show or necessarily correspond to how you would implement an envelope tracking system. They do show different techniques to efficiently simulate such systems if you have a model of the power amplifier, however. The model could be a transistor-level schematic or some sort of behavioral model, including X-parameters*.

Figure 3 shows the basic block diagram for modeling an envelope tracking system used in the examples. The shaping is applied to keep the amplifier operating at a constant gain or gain compression even though its drain bias is being modulated.

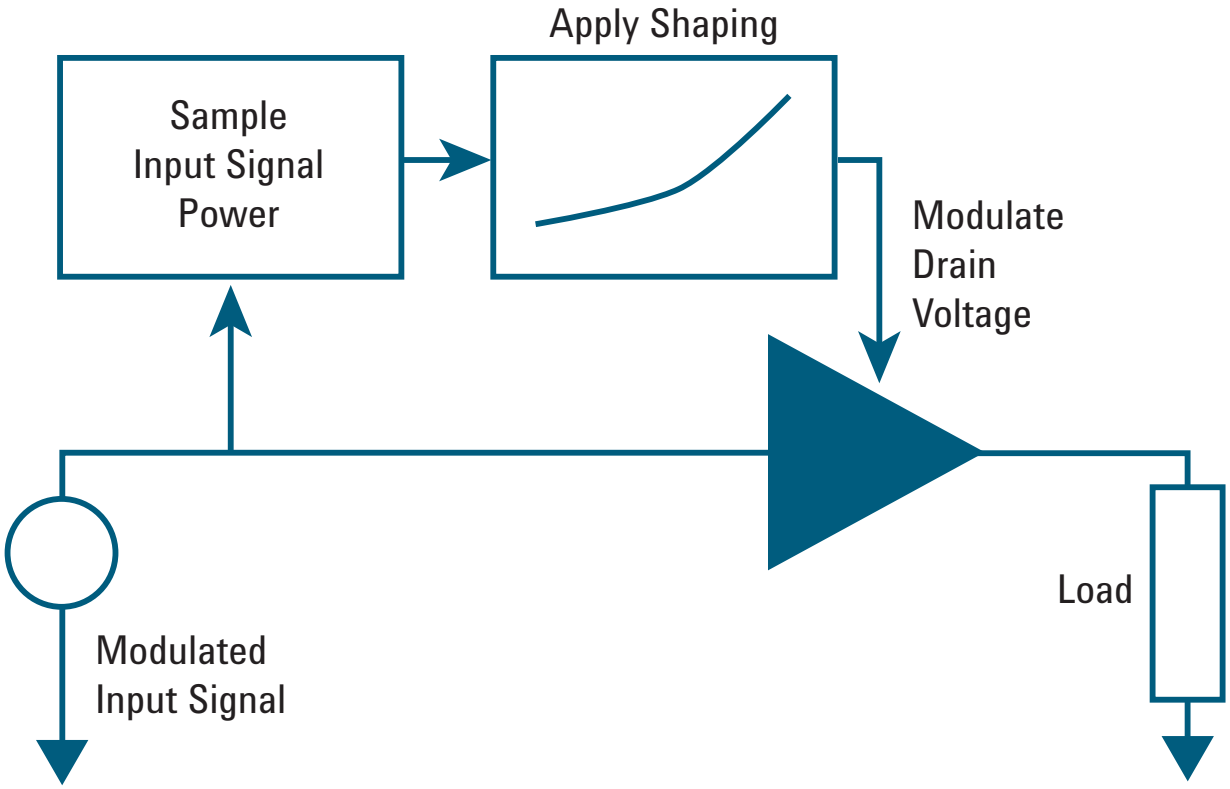

Figure 3. A block diagram for simulating Envelope Tracking.

2.0 Characterizing the Power Amplifier

2.1 Testing the Power Amplifier for Memory Effects

Prior to simulating ET on an amplifier, you should check for memory effects (assuming the model you are using would show them) and run simulations to generate the shaping functions.

Before applying ET, it is first useful to test the PA for memory effects that may be caused by the behavior of the active device(s) or by the bias network. This can be done using the harmonic balance test available in the **1. Memory Effect Testing** folder of the example. If an amplifier has memory effects, its output is not just a function of its input at the current instant in time. It will also depend on what the input was previously.

The easiest way to test for memory effects is to run a two-tone harmonic balance simulation (**MemoryEffectTest_Freq_Delta_Sweep_HB**) in which the frequency spacing is swept between the input tones (Figure 4). If the amplitudes of the lower and upper third-order intermodulation distortion sidebands are not equal then the amplifier is exhibiting memory effects.

In this case, the example of a PA designed for wideband modulation, the simulation results shown in Figure 5 indicate that memory effects are minimal. This is true even when the frequency spacing between the two input signals is 5 MHz. Consequently, the amplifier should behave fairly well (even with the modulation bandwidth of the input signal at 5 MHz).

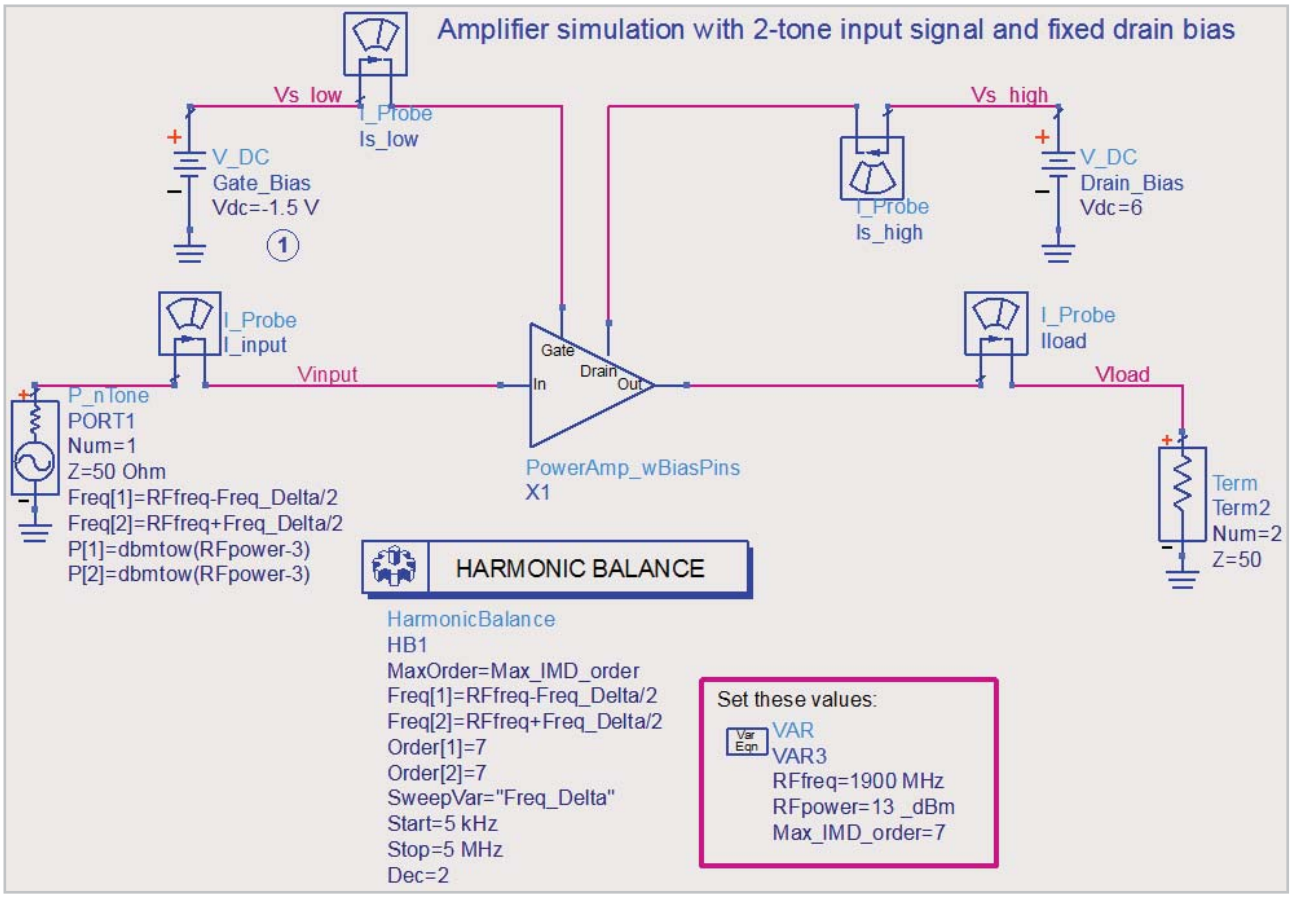

Figure 4. Simulation setup for a two-tone harmonic balance simulation.

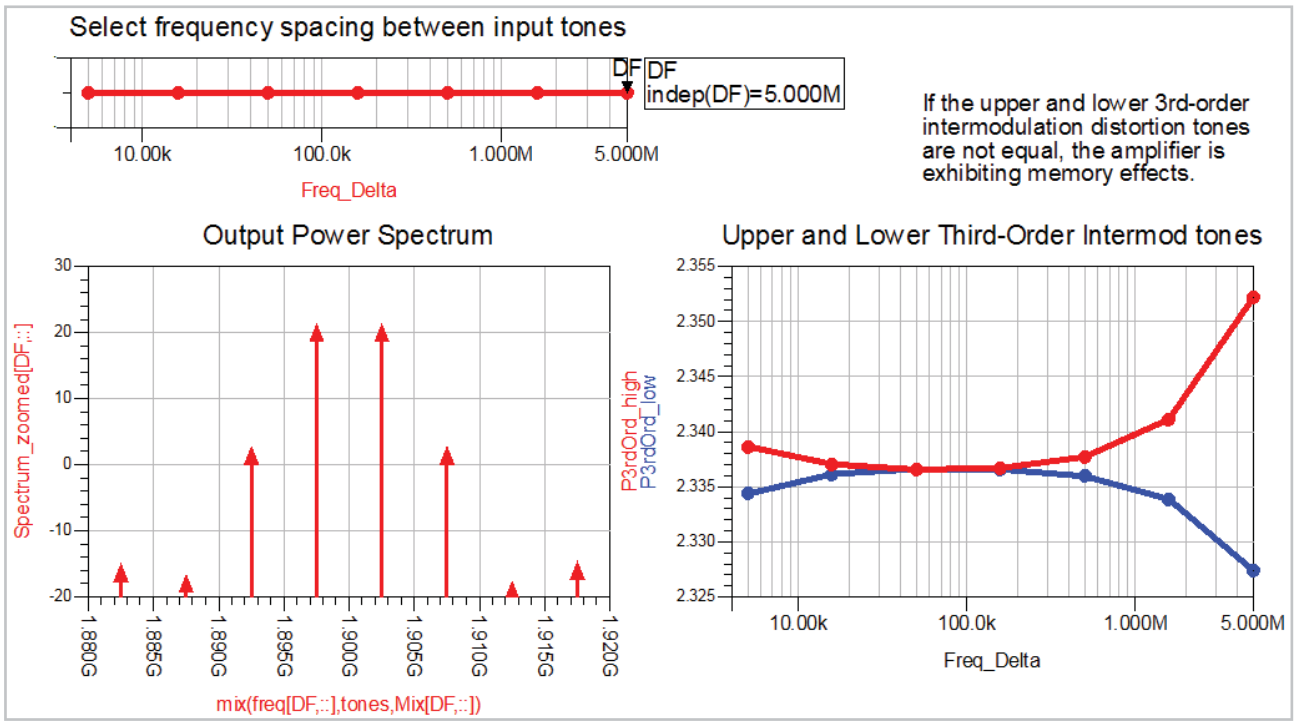

Figure 5. Simulation results for the example of a PA designed for wideband modulation.

2.2 Generating Data for a Shaping Table to Maintain Constant Gain

While not absolutely necessary, it should be useful to see how a PA's power-added efficiency (PAE) varies with output power, with the drain bias voltage swept as a parameter, prior to applying ET. This should give you an idea of the potential performance improvement you can attain. The **HB1ToneGComp1swp** schematic in the **2. Simulations to Generate Shaping Functions** folder is used to simulate the PA as a function of drain bias voltage. This schematic and data display came from an updated ADS Amplifier DesignGuide available at ***http://edocs.soco.agilent.com/pages/viewpage.action?pageId=161047818***. (This updated Amplifier DesignGuide will be in ADS 2012.)

The setup for this simulation is shown in Figure 6. It was generated by selecting, from any schematic, **DesignGuide>Amplifier>1-Tone Nonlinear Simulations>Spectrum, Gain, Harmonic Distortion at X-dB Gain Compression (w/PAE) vs. 1 Param**. Here, the drain bias voltage is being swept to see how gain and gain compression vary. The gate bias voltage has been set to -1.5 V. Looking at the simulation in the **0. Device I-V Curves** folder provides input on exactly how the gate bias affects the PA's performance.

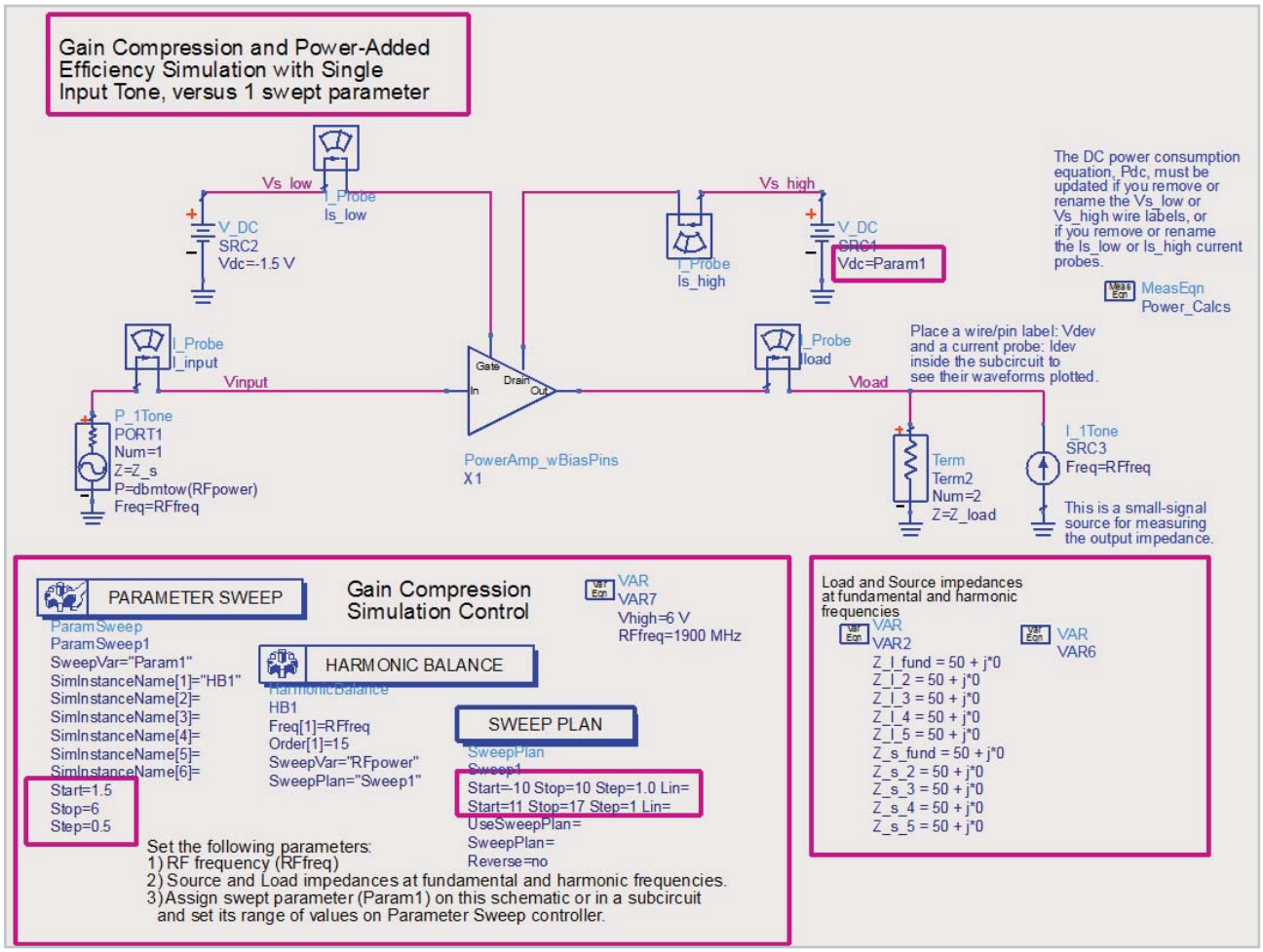

Figure 6. Simulation setup for characterizing the PA.

The **HB1ToneGComp1swp** data display, **Spectrum, Gain, Harmonics** tab shows, among other things, a PAE versus fundamental output power plot (Figure 7). As evidenced by the plot curves, for lower output powers the PAE increases as the drain bias is decreased. Consider, for example, the fourth curve from the left (drain bias 3 V) in the plot (for the gray curves from left to right, the drain bias increases from 1.5 V to 6 V in 0.5 V steps.) It indicates that if a bias of 3 V is used when the output power is near 21 dBm, the PAE would be about 34 % versus about 14% with a fixed drain bias of 6 V.

The ADS Gain and Gain Compression plot (Figure 8) shows how these parameters vary as a function of output power and drain bias. An example of this plot, with equations and listing columns added to the **HB1ToneGComp1swp** data display in the example, is shown in Figure 9. The plot shows what the drain bias (**HB.Param1**, the swept parameter in the simulation) should be for a particular available source power to maintain a constant gain (specified by **Desired_Gain**). A new feature for this plot that's available in ADS 2012 is the **interpolate_y_vs_x()** function (Figure 9). This function is found in the **utility_fun.ael** file inside the example PA's workspace. (If using a release prior to ADS 2012, you will have to place this .ael file in your $HOME/hpeesof/expressions/ael directory and re-start ADS.)

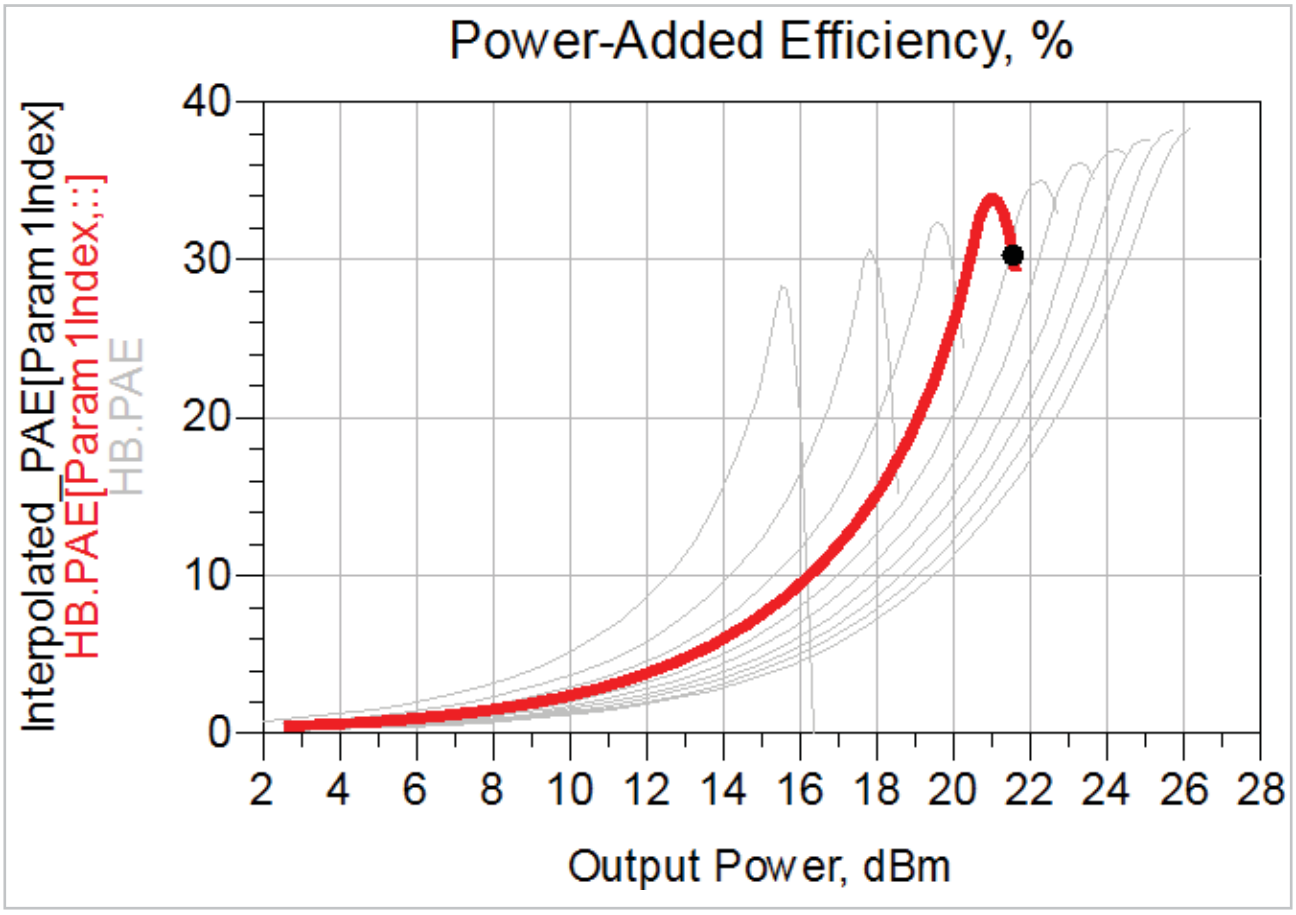

Figure 7. Plot of PAE versus output power, showing increasing drain bias from left to right.

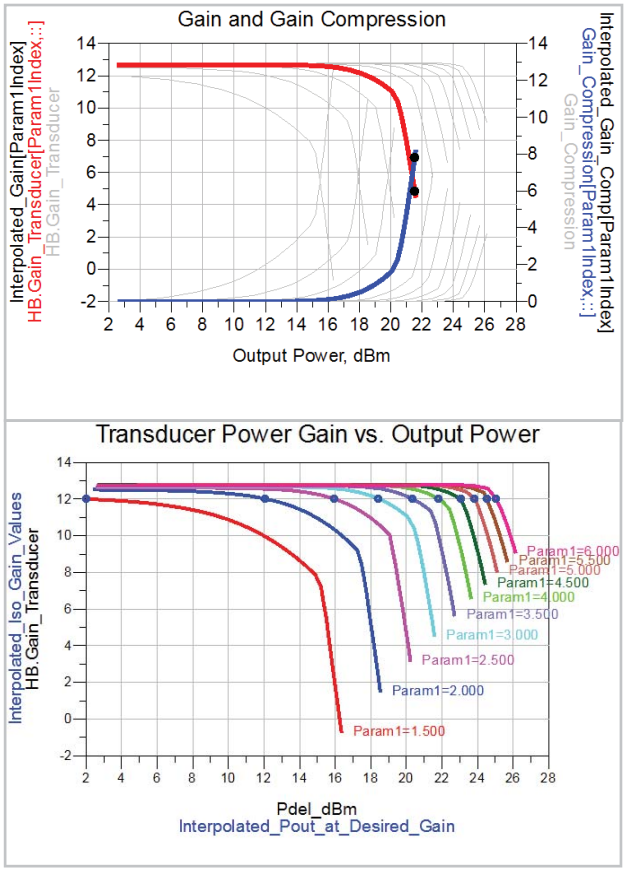

Figure 8. Plot of gain and gain compression.

As an example, consider that when the drain bias (**HB.Param1**) is 2 V, at 12 dB gain the output power (**Interpolated_Pout_at_Desired_Gain**) is 12.068 dBm. The available source power (**Interpolated_Pavs_dBm_at_Desired_Gain**) is 0.05 dBm. The data from the listing columns can be typed into a GMDIF file (figure 10), which then becomes the shaping table when running an ET simulation. Note that a shaping table may be generated for a different gain just by setting **Desired_Gain** to a different value.

```
BEGIN GMDIF
% pin_dBm(1)      voltage(1)
-10.0                 1.5
0.05                  2
3.90                  2.5
6.40                  3
8.30                  3.5
9.80                  4.0
11.05                 4.5
11.80                 5.0
12.50                 5.5
13.05                 6.0
END
```

Figure 10. Shaping table as a GMDIF file.

```
Eqn Desired_Gain=12
Eqn Interpolated_Pout_at_Desired_Gain=interpolate_y_vs_x(HB.Pdel_dBm,HB.Gain_Transducer,Desired_Gain,0.05,"linear")
Eqn Interpolated_Pavs_dBm_at_Desired_Gain=Interpolated_Pout_at_Desired_Gain-indep(Interpolated_Pout_at_Desired_Gain)
Eqn Interpolated_Iso_Gain_Values=indep(Interpolated_Pout_at_Desired_Gain)
```

HB.Param1	Interpolated_Pout_at_Desired_Gain	Interpolated_Pavs_dBm_at_Desired_Gain
1.500	2.001	-10.000
2.000	12.068	0.050
2.500	15.919	3.900
3.000	18.420	6.400
3.500	20.316	8.300
4.000	21.816	9.800
4.500	23.052	11.050
5.000	23.808	11.800
5.500	24.508	12.500
6.000	25.050	13.050

Figure 9. Using the interpolate_y_vs_x() function to obtain constant gain data.

2.3 Generating Data for a Shaping Table to Maintain Constant Gain Compression

In the same **HB1ToneGComp1swp** data display file, the **X-dB Gain Compression Data** tab shows the gain and gain compression data, but also presents the data at a specified level of gain compression. In Figure 11, for example, 1.5 dB of gain compression (relative to the maximum gain point) has been specified.

The gain values at the 1.5 dB gain compression points (the pink dots in Figure 11) can be used to shape the amplifier's drain bias voltage. Figure 12 shows the data that would be used in the shaping table.

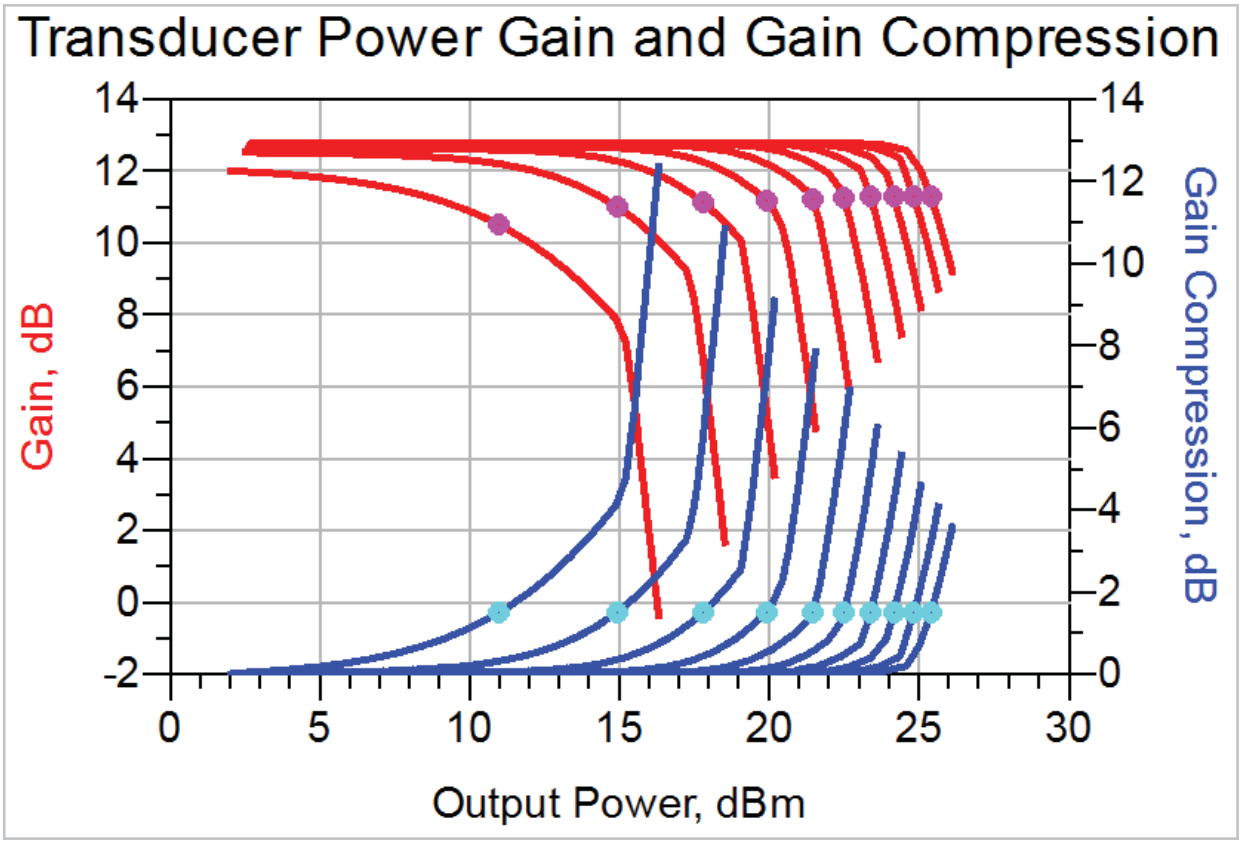

Figure 11: Interpolated values at 1.5 dB of gain compression.

Swept Parameter Value	Interpolated Available Source Power at Gain Comp. Point
1.500	0.480
2.000	3.900
2.500	6.660
3.000	8.730
3.500	10.230
4.000	11.250
4.500	12.105
5.000	12.865
5.500	13.520
6.000	14.115

Figure 12. Shaping table data to maintain constant gain compression.

3.0 Examining the Modulated RF Signal

One final task that may be useful to perform prior to simulating an amplifier with ET is to examine the test signal. The source used in all the ADS Ptolemy co-simulations in this example is shown in the L**TE_Source_Test schematic** in the **3. Testing the LTE Signal folder** (Figure 13).

The setup employed to simulate the test signal comes from the ADS example: **LTE/LTE_FDD_UL_Tx_wrk/ LTE_UL_TxEVM**. Many other modulated signals are available in ADS's Wireless Libraries, so a signal from a different example could also be used. Note that the schematic in Figure 13 has been modified from the original example. In this case, the behavioral model amplifier was removed, the **RLoad** parameter on the EVM sink was set to **DefaultRLoad** (1e18) instead of 50 ohms, and a TimedSink was added to record the voltage across the 50-ohm load resistor so the power from the source could be observed as a function of time. Additionally, the **FramesToMeasure** variable was reduced to 1, which is the lowest number allowed by the EVM sink.

Figure 14 shows part of the **LTE_Source_Test** data display.

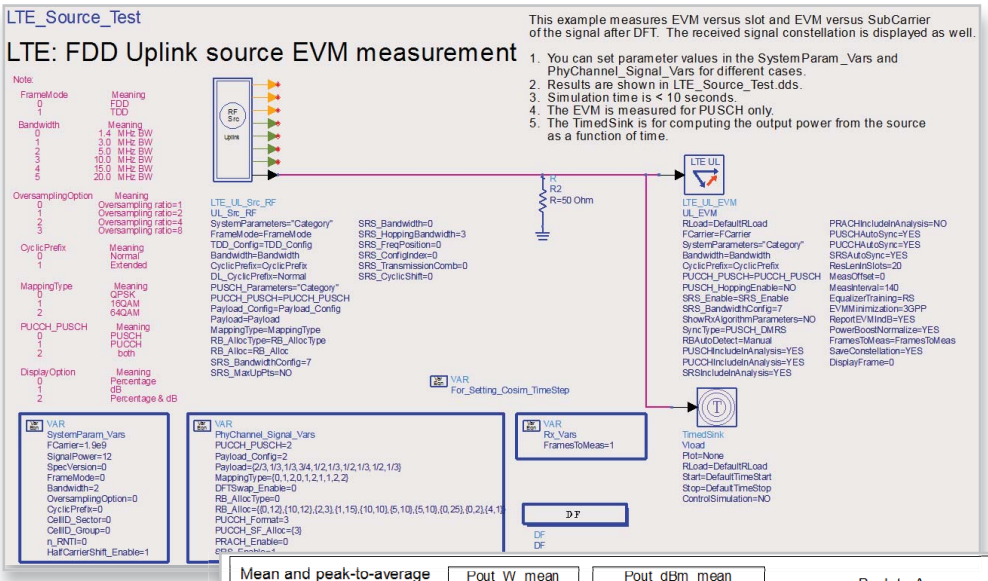

Figure 13. Setup for examining the ADS Ptolemy co-simulation source.

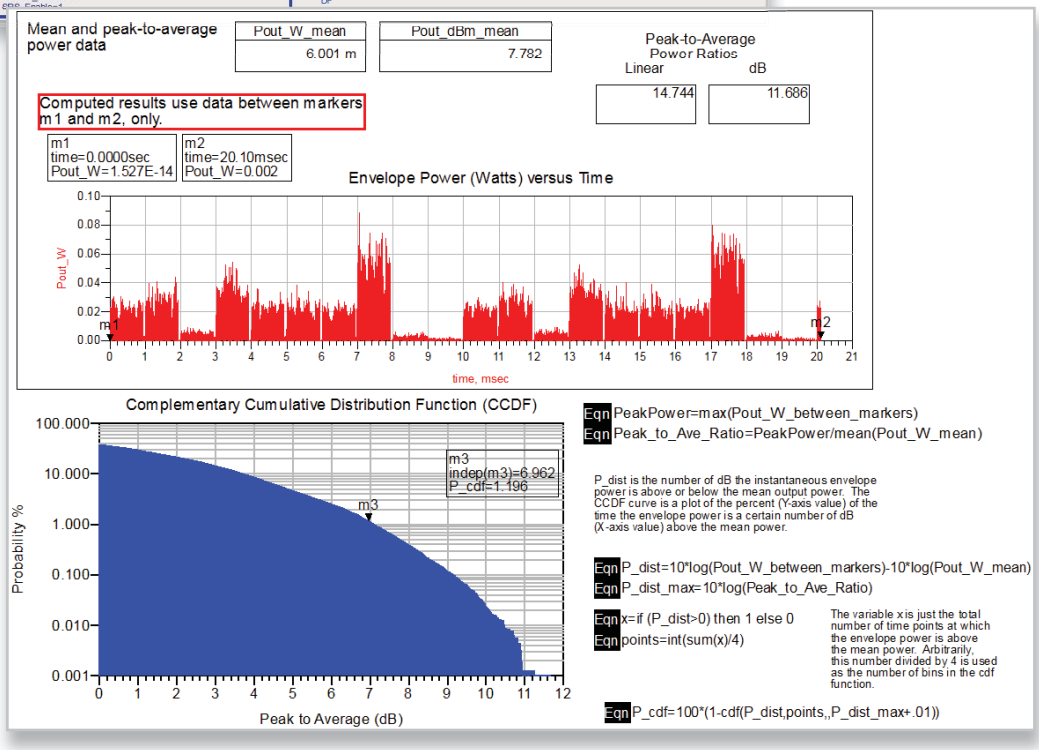

Figure 14. The LTE_ Source_Test data display.

The test signal has bursts of different power levels, leading to a high PAPR. Moving the markers on the display shows power data within a particular burst. Alternatively, the markers can be moved to their locations by setting time=7msec on one marker readout and time=8msec on the other, as shown in Figure 15.

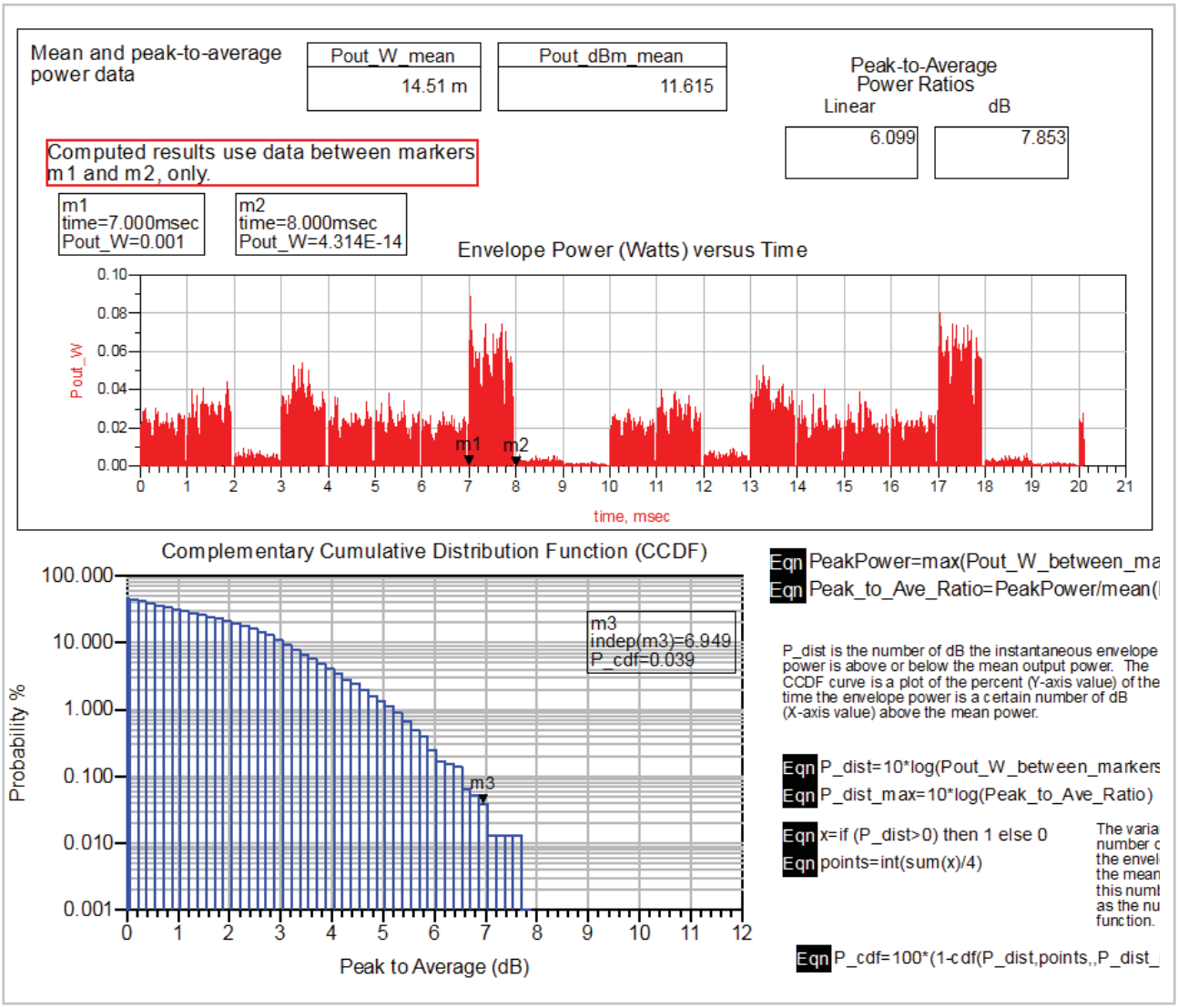

Figure 15. Setting marker locations is one way to see power data within a particular burst.

4.0 Simulating the Power Amplifier with a Fixed Drain Bias

There are a number of different ways to set up and run simulations of the PA with a fixed drain bias. One way is to employ a source that uses data generated from a different Ptolemy simulation, such as the one shown above. The advantage of this technique is that simulations can be run for as long or as short as desired, without the user having to know anything about setting up and running Ptolemy co-simulations. Another method employs Ptolemy co-simulation. While this technique has the advantage of providing specification-compliant measurement results, the overall simulation time may be longer. One other technique involves simulation with the Agilent 89600 VSA software being used to post-process the results. Here, users can view simulation results using the same 89600 VSA software that is used to make physical measurements.

As an example, the **LTE_Signal_w_Fixed_Bias** schematic in the **4. Simulations with Fixed Bias** folder is used to simulate the PA with an LTE signal and a fixed drain bias (Figure 16). This is the simplest simulation setup, however; the modulated signal must be either generated separately or obtained from another source (e.g., someone else). It is also possible to use I and Q data. In this case, the signal was generated from an ADS LTE example, as described in the **Envelope_Tracking_Sim** document found at ***http://edocs.soco.agilent.com/display/eesofkcads/Applying+envelope+tracking+to+Improve+Efficiency***. When generating the modulated signal, users can specify QPSK, 16QAM, 64QAM, or some combination of these modulation schemes. Note that the statistics of this source signal are shown in the **LTE_UL_TxSpectrum** data display file in the **3. Testing the LTE Signal, Statistics of a short LTE signal** folder.

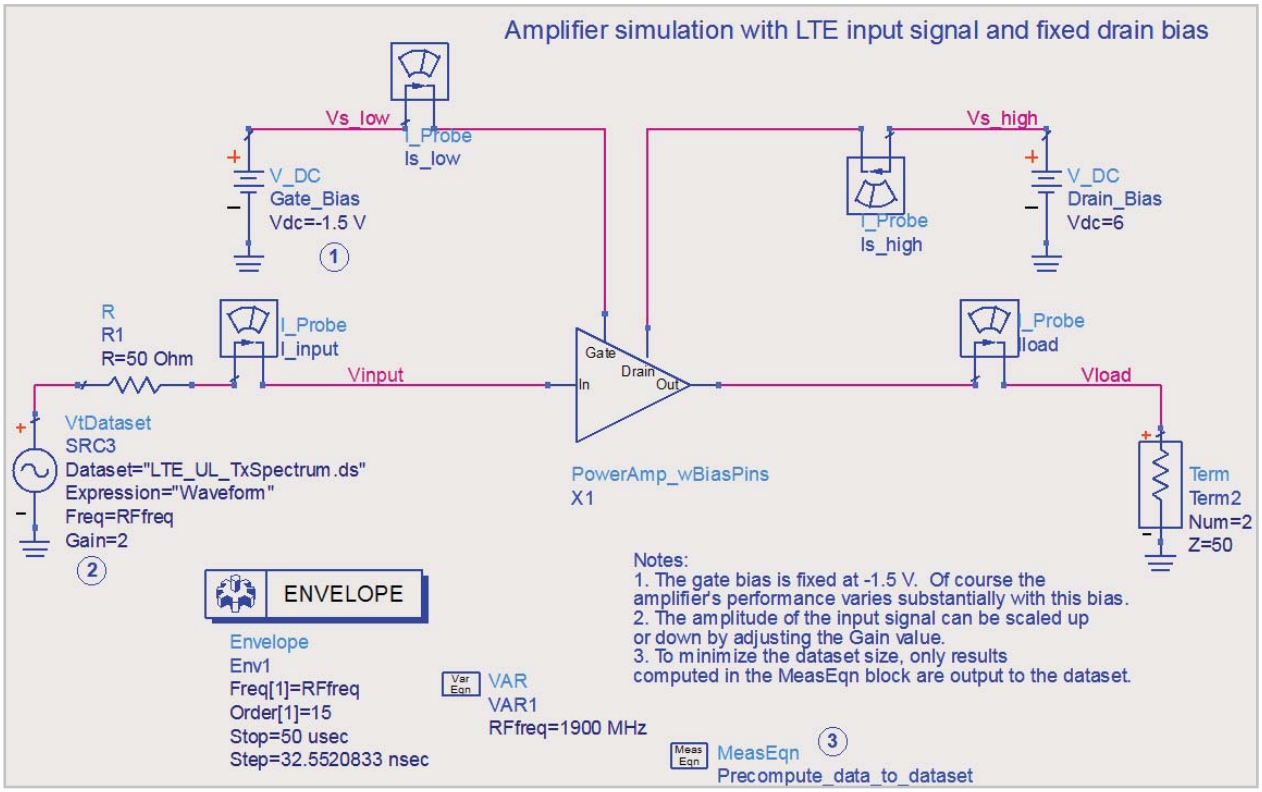

Figure 16. Simulating the power amplifier with a fixed drain bias.

The simulation runs in about 8 seconds. However, since the simulation can be as long or short as the user wants, the actual run time will differ depending on the set stop time. Figure 17 shows the simulation results and indicates a pretty low mean PAE (only 15.7 %), which signals the need for ET. Notice that the AM-to-AM and AM-to-PM distortion curves look a little "fuzzy." This is because the amplifier is exhibiting slight memory effects.

The above simulation could be re-run with the **VtDataset** source reading data from the **LTE_Source_Test** dataset. This dataset may have been removed from the example to save space, in which case it can be re-created by re-running a simulation from the **LTE_Source_Test** schematic. The time point in the dataset where the data starts can be changed via the $\mathbf{T_{offset}}$ parameter.

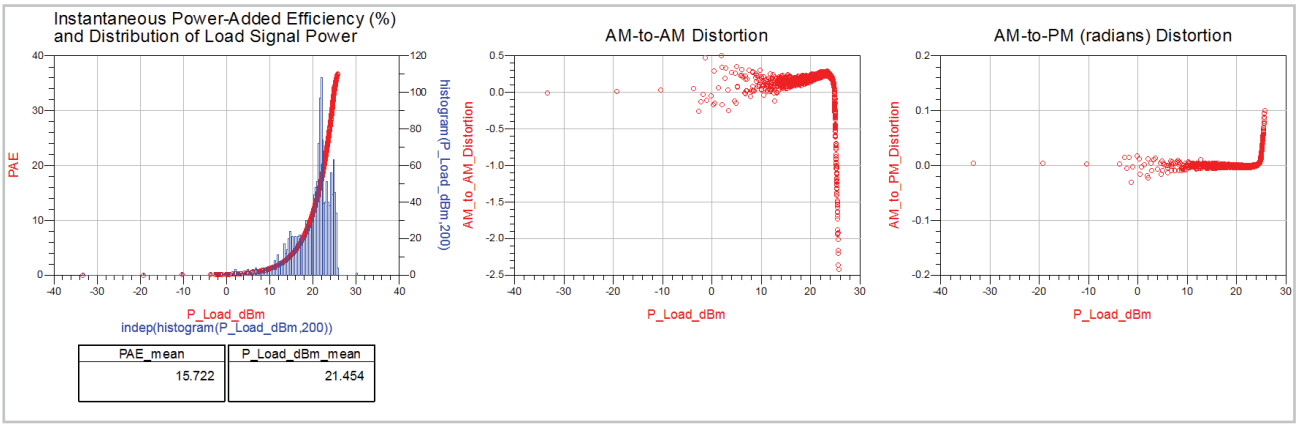

Figure 17. Simulation results.

5.0 Implementing Envelope Tracking Using Behavioral Model Components

For a clearer understanding of how ET is implemented in ADS, begin by downloading and reviewing the **Envelope_Tracking_Sim** document.

http://edocs.soco.agilent.com/display/eesofkcads/Applying+envelope+tracking+to+Improve+Efficiency.

5.1 Applying Envelope Tracking to the Amplifier

To apply ET to the same amplifier used in Section 4.0, the **LTE_Signal_w_ET_Bias_12_dB_Gain** schematic in the **5. Envelope Tracking with Constant Gain** folder is used (Figure 18). Doing so improves the PAE by 4.9%, raising it from 15.7% to 20.6 %, as shown in Figure 19. The black curve in the figure represents the PAE with a fixed drain bias.

The above fixed bias and ET simulations were re-run with Gain=2.5 on the LTE source. The results with fixed bias are shown in Figure 20. The results with ET are shown in Figure 21.

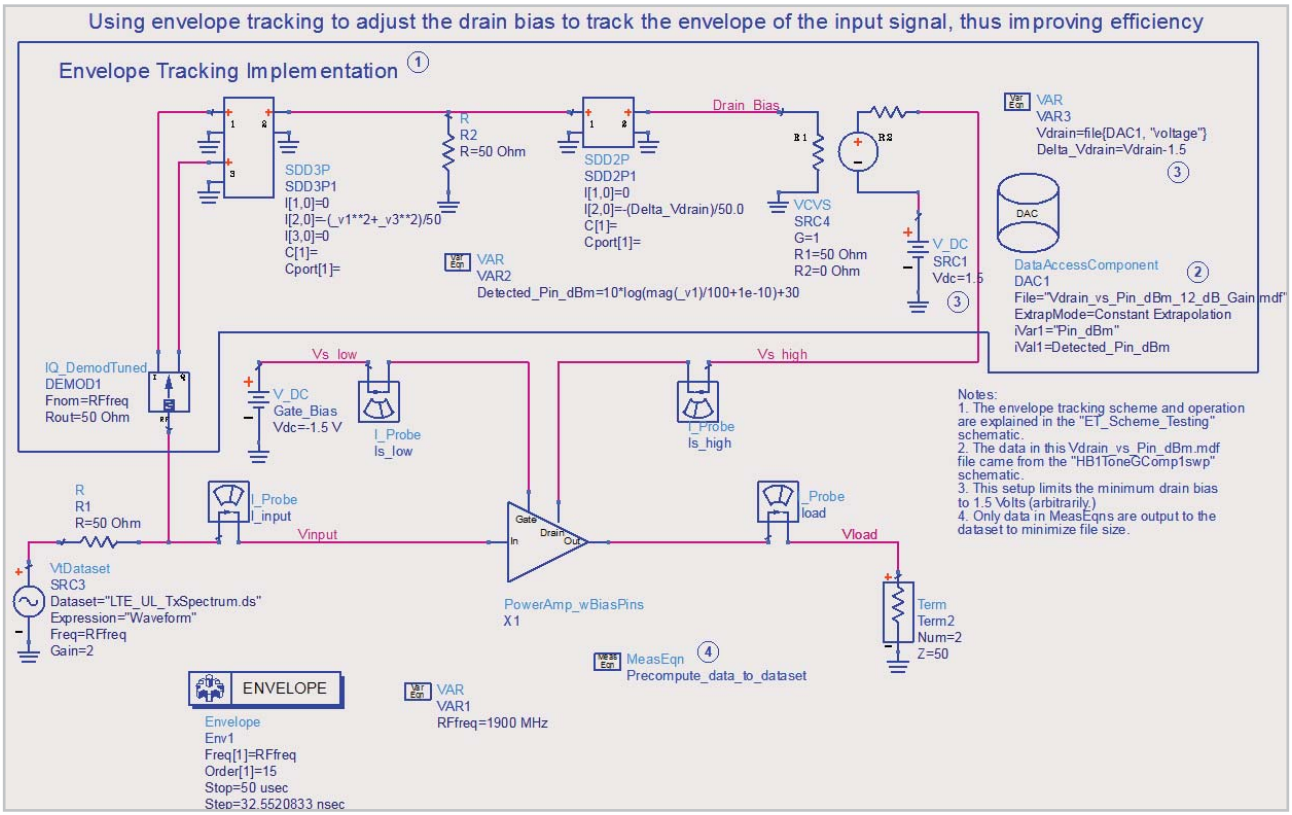

Figure 18. Schematic for using ET to adjust the drain bias.

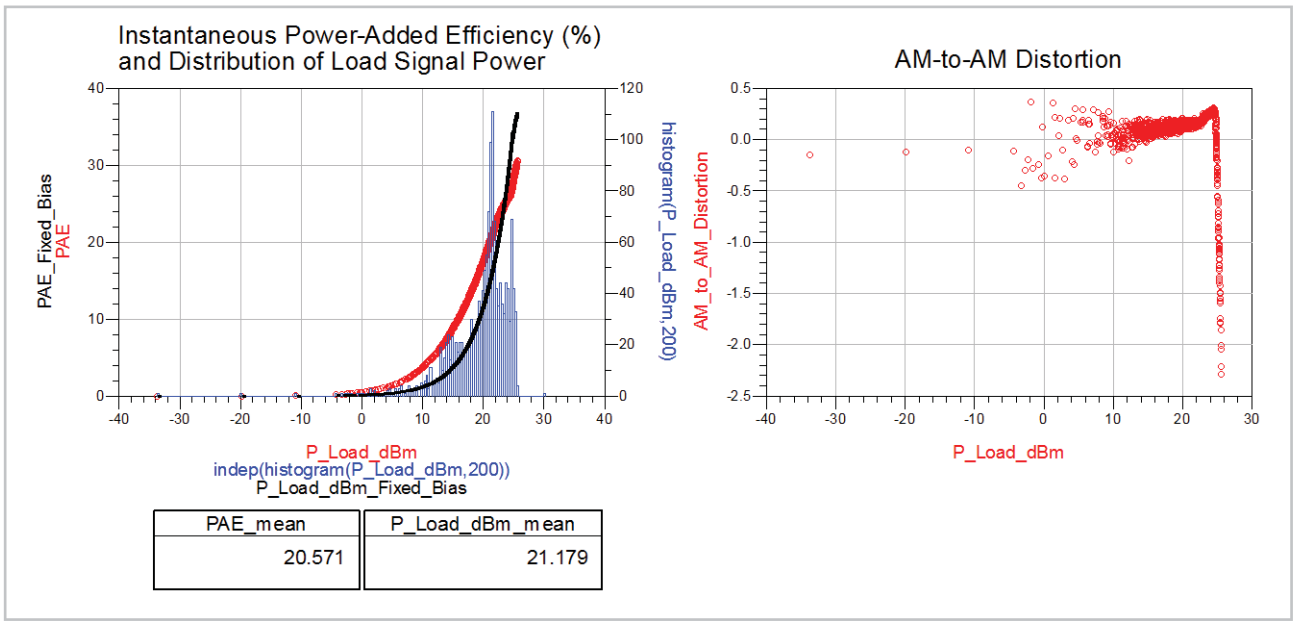

Figure 19. Simulation results after applying ET.

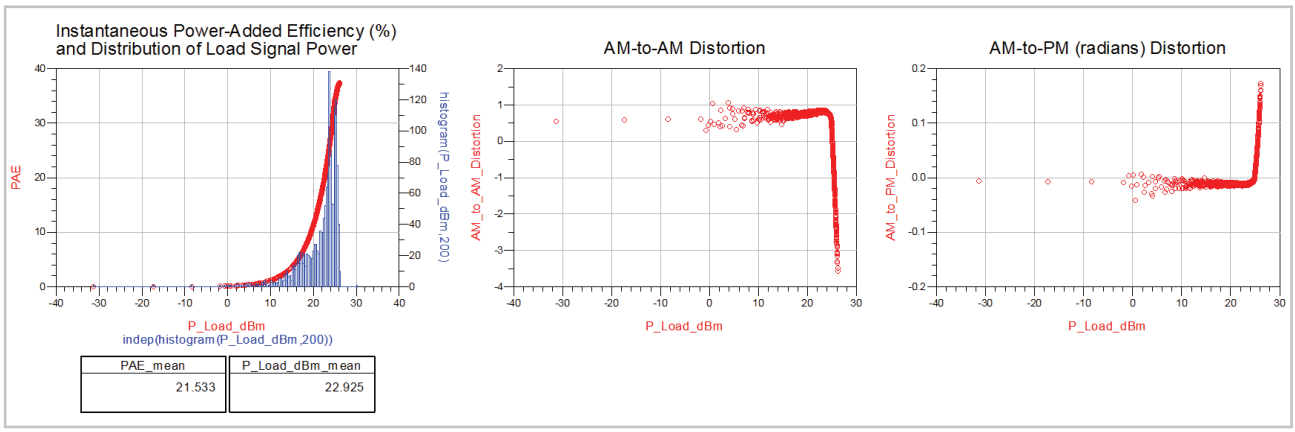

Figure 20. Fixed bias simulation with Gain=2.5 on the LTE source.

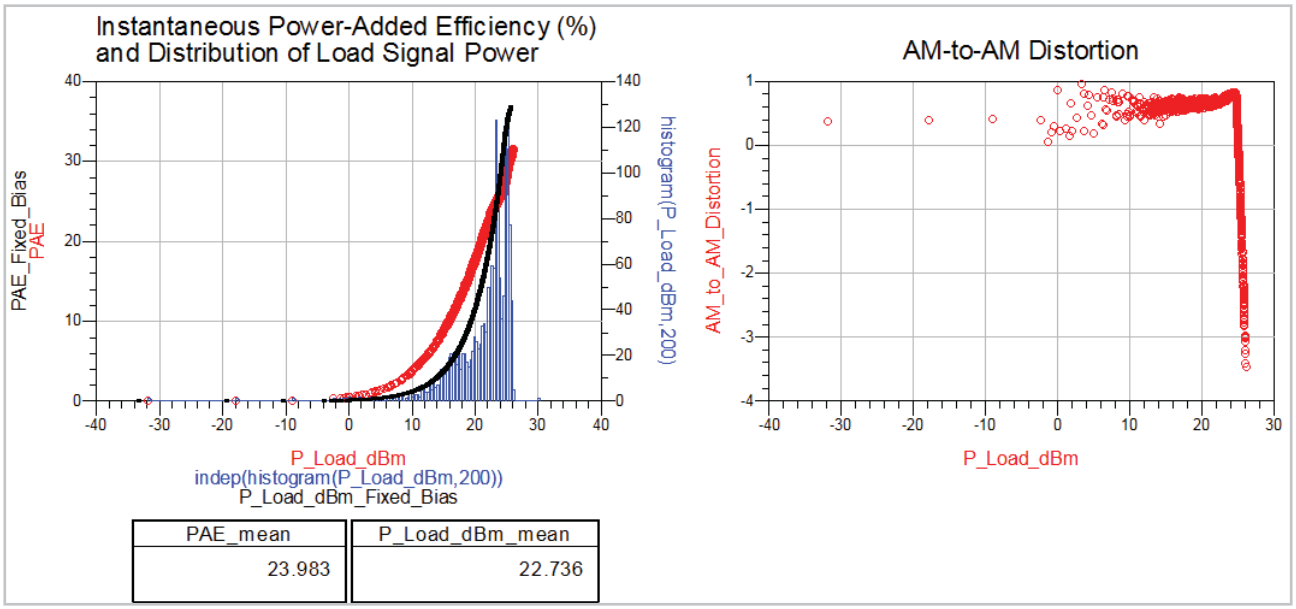

Figure 21. ET simulation with Gain=2.5 on the LTE source.

Notice that when using ET, there is only a slight improvement in PAE, about 24% versus 21.5%. As shown in Figure 22, that improvement increases further (about 22.5% versus 15.7%), when an 11-dB constant gain shaping table is used instead of a 12-dB constant gain (the gain parameter on the source was set back to 2.)

As the below data indicates, different simulation results are obtained depending on the amplitude of the input signal and the shaping table. Although not shown here, how the amplifier is biased will also affect the performance.

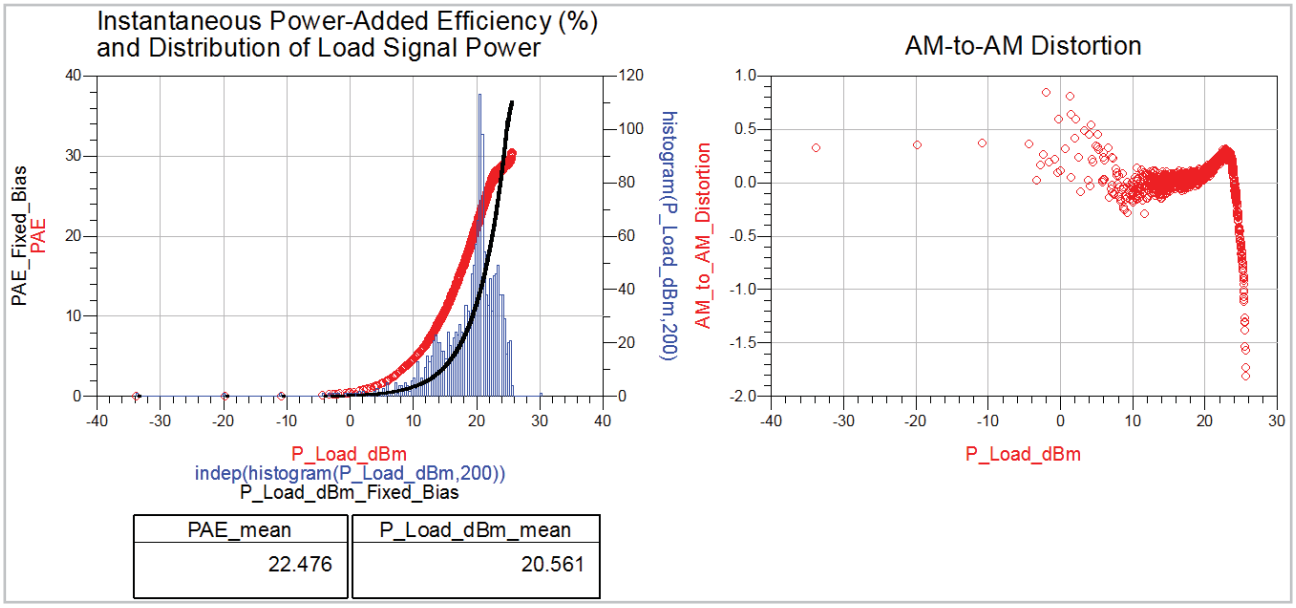

Figure 22. ET simulation using a shaping table to maintain 11 dB constant gain.

6.0 Using Ptolemy Sources and Sinks to Simulate EVM and Drain Efficiency

Using Ptolemy co-simulation, it is possible to obtain specification-compliant error-vector-magnitude (EVM) data and drain efficiency data.

6.1 Simulations with a fixed bias

As an example, the **LTE_Cosim_Fixed_Bias_EVM** schematic in the **4. Simulations with Fixed Bias** folder shows a Ptolemy co-simulation of the amplifier with a fixed bias (Figure 23). The setup for this co-simulation came from the ADS example, **$HPEESOF_DIR/examples/LTE/LTE_FDD_UL_Tx_wrk**.

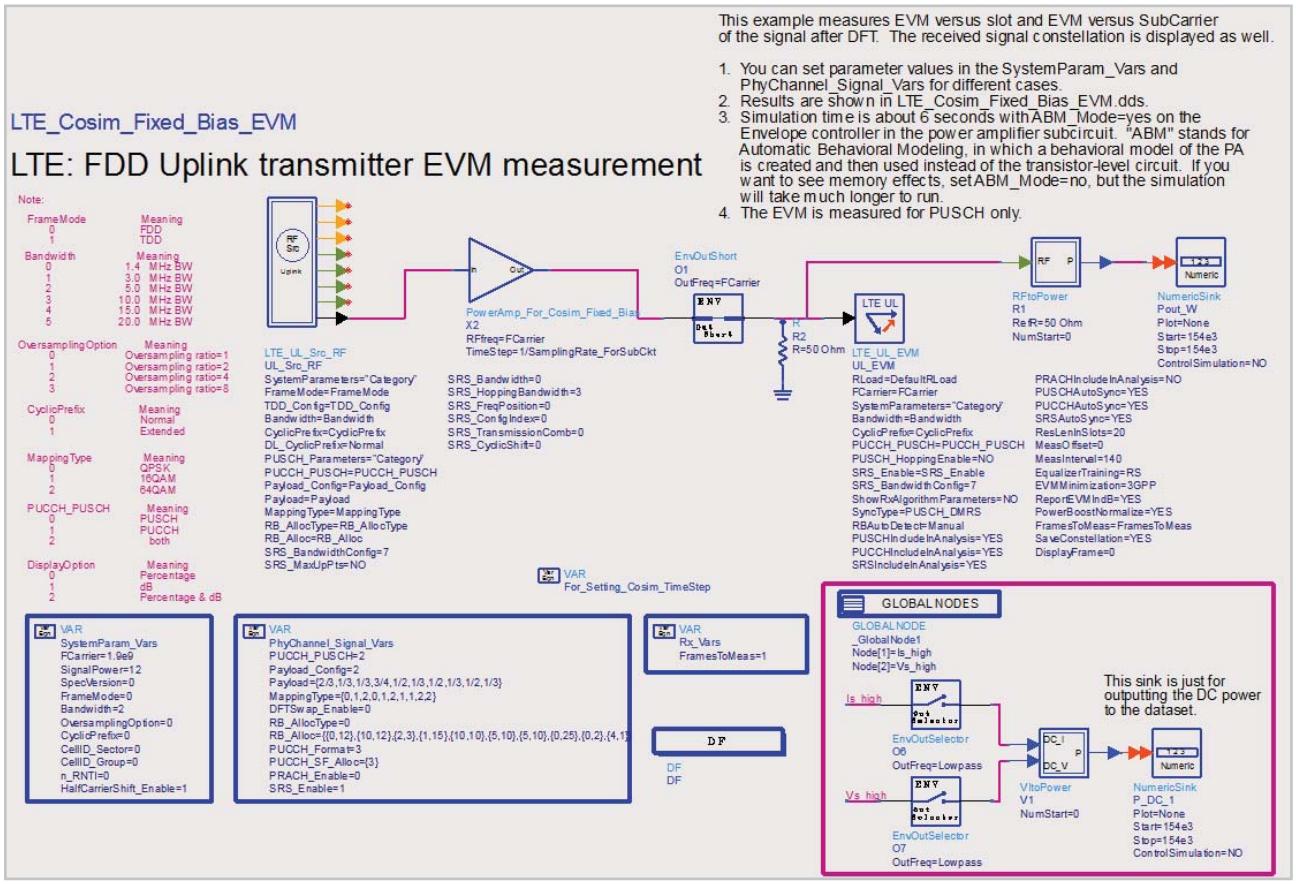

Figure 23. Ptolemy co-simulation schematic.

Some important things to note about this simulation setup.

- The **FramesToMeas** is set to 1 to minimize the simulation time.
- The PA subcircuit, **PowerAmp_For_Cosim_Fixed_Bias**, has an Envelope simulation controller and there are two passed parameters: **RFfreq and TimeStep. RFfreq** is the center frequency of the analysis and is set so that it's equal to the carrier frequency of the LTE source, FCarrier, while **TimeStep** is the simulation time step. It is set so that it is equal to the same value as the time step in the LTE source. Doing so allows the simulation time steps in both the source and subcircuit to remain equal to each other even if the signal bandwidth or oversampling ratio is changed. This is done using equations (**SamplingFreq_ForSubCkt** and **SamplingRate_ForSubCkt**) in the VAR block **For_Setting_Cosim_TimeStep**. These equations have the same right-hand side as the **SamplingFreq** and **SamplingRate** equations in the **LTE_UL_Src_RF** source subcircuit.
- The amplifier subcircuit does not contain a load. Instead a 50-Ohm resistor is placed to ground in the top-level schematic. With this explicit 50-Ohm resistor on the schematic, it is necessary to make sure that all sinks at the top level do not load the output of the amplifier, also. In this case, the **LTE_UL_EVM sink**, **RLoad=DefaultRLoad** specified in the **DF controller**, **Resistors** tab is set to 1.0e18.
- For drain efficiency calculations, the DC power consumption and average power delivered to the load need to be computed. When running Ptolemy co-simulations, the voltages and currents in the subcircuit are not output directly. In the amplifier subcircuit, a current-controlled voltage source is used to convert the drain current to a node voltage of the same value. This node voltage and the drain voltage are made available at the top level for DC power calculation via the Global Nodes component.
- The RF power delivered to the load is computed using the **RFtoPower** signal converter. The **Pout_W and P_DC_1** numeric sinks compute running averages of the RF output power and DC power consumption, respectively. Their start and stop values are set to minimize the amount of data collected. Ideally, you just want the last data point from these two sinks. However, the sinks start collecting data when the numeric start value is reached and keep collecting data until the simulation ends (controlled by the **LTE_UL_EVM** sink). There is no easy way to determine what values to use for start and stop. In this case, a separate simulation was run with **Start=DefaultNumericStart** and **Stop=DefaultNumericStop**. The length of the data from these two sinks was observed and the start and stop values were then set to values slightly less than this length.
- "Enable fast co-simulation" is checked on the **Fast Cosim** tab for the Envelope controller in the amplifier subcircuit. This is also known as automatic behavioral modeling (ABM), a technique in which a behavioral model of the amplifier subcircuit is generated and then simulated instead of the transistor-level circuit. ABM leads to a much faster simulation, but does not include memory effects.

The **LTE_Cosim_Fixed_Bias_EVM** data display file shows the simulation results, including various EVM calculations, constellation diagrams, power, and efficiency (Figure 24).

Note that the values for output power and drain efficiency are not very close to the simulated values obtained using a **VtDataset** source and a much shorter time record. This is to be expected, since the statistics of the much shorter input waveform are significantly different from the much longer input waveform used in this simulation.

The LTE signal has multiple bursts, each with very different power levels. Consequently, just calculating an overall average drain efficiency may be misleading since the amplifier may be operating way into compression during some bursts, but linearly during other bursts. However, it is possible to examine the PA's performance during different, arbitrary time intervals.

As an example, consider the **LTE_Cosim_Fixed_Bias_EVM_alt** schematic found in the **4. Simulations with Fixed Bias** folder (Figure 25). The schematic is similar to **LTE_Cosim_Fixed_Bias_EVM** except that it includes timed sinks for recording the RF voltages and currents at the amplifier input, voltage at the load, and bias voltage and current.

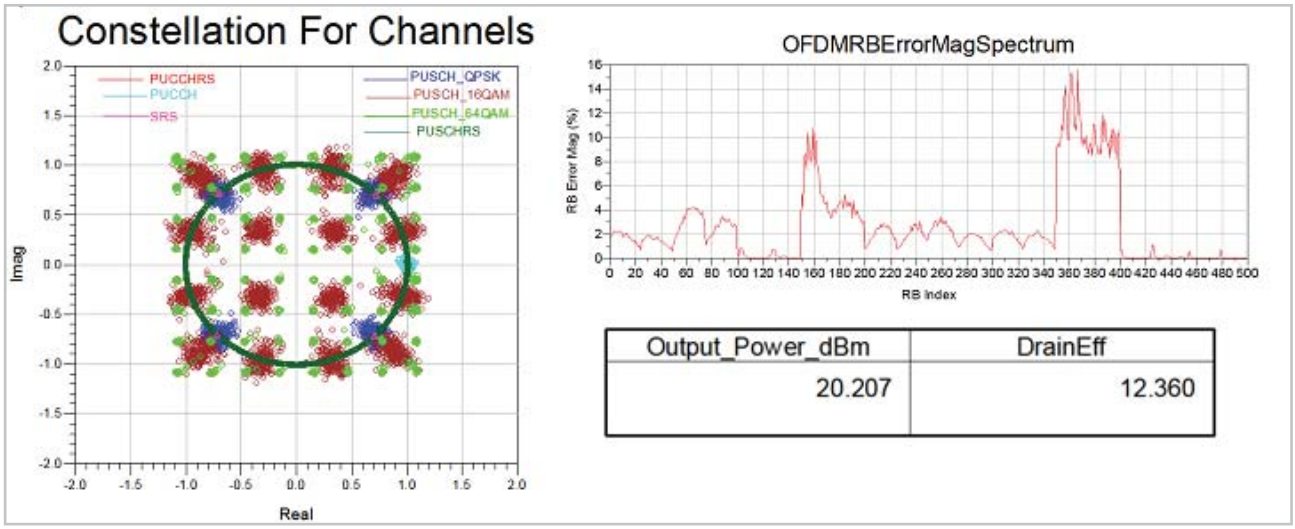

Figure 24. Ptolemy co-simulation results.

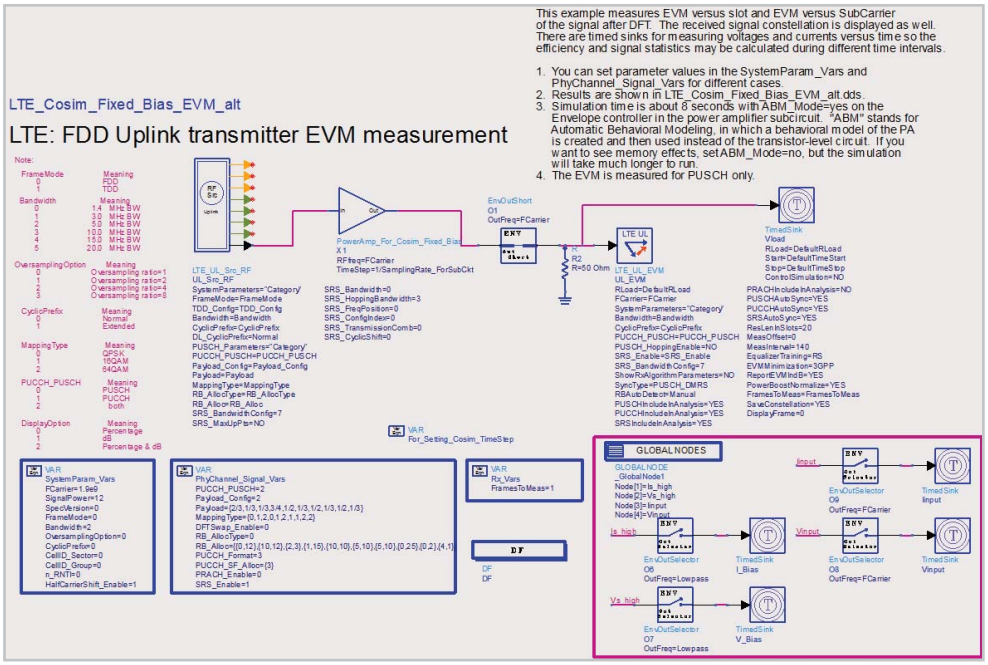

*Figure 25. **LTE_Cosim_Fixed_Bias_EVM_alt** co-simulation schematic.*

The corresponding **LTE_Cosim_Fixed_Bias_EVM_alt** data display shows the power, efficiency and gain data during an arbitrary time interval selected by markers m1 and m2 (Figure 26). Note that during the burst from 7 to 8 msec, the amplifier is somewhat compressed (Figure 27). However, during the burst from about 9 to 10 msec it operates quite linearly (Figure 28).

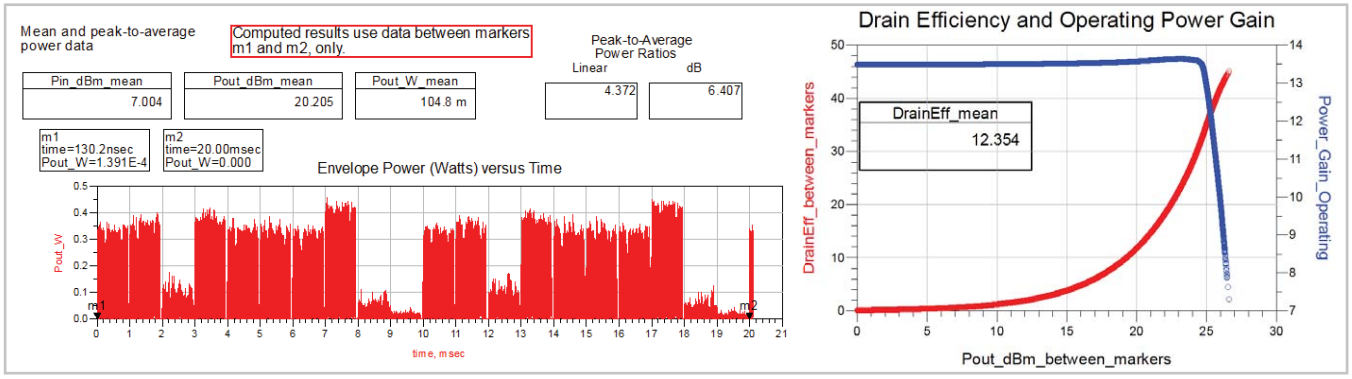

Figure 26. ***LTE_Cosim_Fixed_Bias_EVM_alt*** *co-simulation results.*

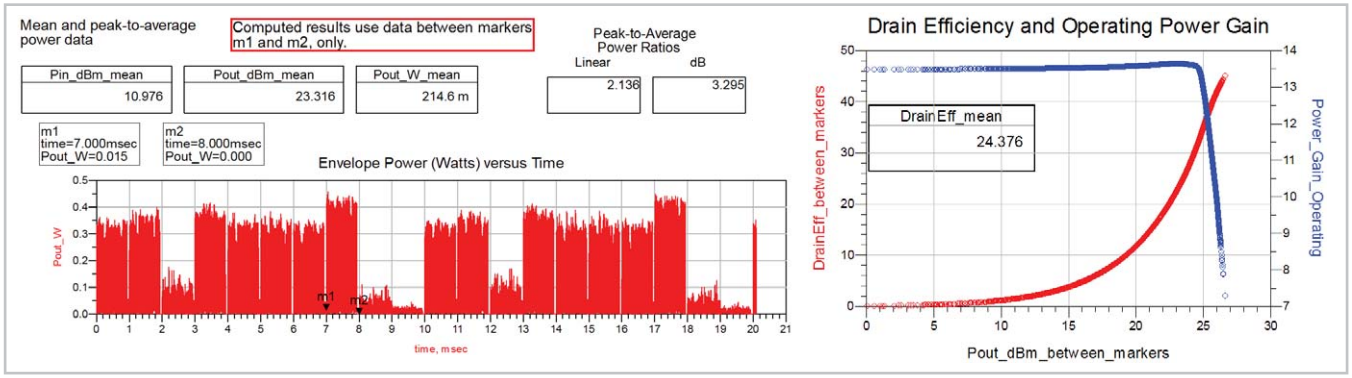

Figure 27. ***LTE_Cosim_Fixed_Bias_EVM_alt*** *co-simulation data from 7 to 8 msec.*

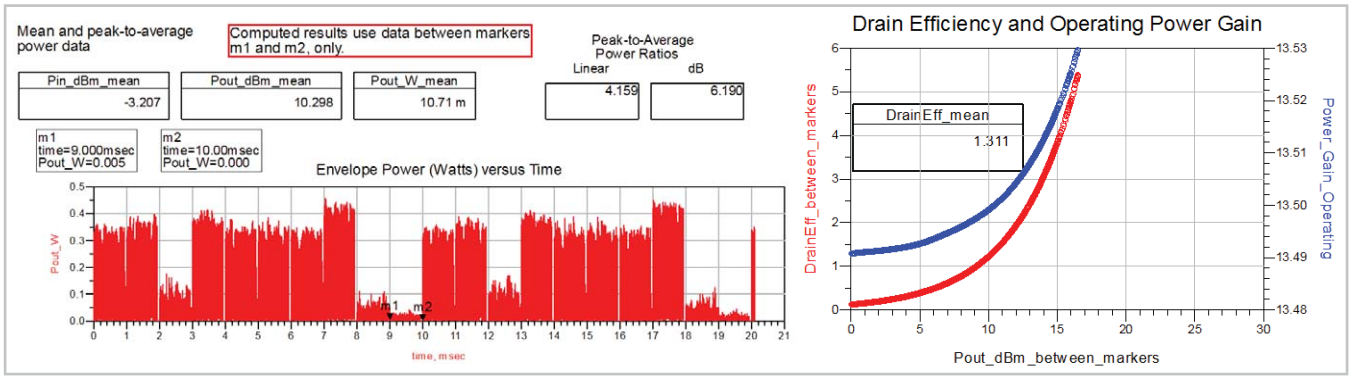

Figure 28. LTE_Cosim_Fixed_Bias_EVM_alt co-simulation data from 9 to 10 msec.

6.2 Simulations with Envelope Tracking

Now, consider the use of Ptolemy co-simulation with envelope tracking to obtain specification-compliant EVM data and drain efficiency data. As an example, the **LTE_Cosim_ET_Bias_11_dB_Gain_EVM** schematic in the **5. Envelope Tracking with Constant Gain** folder shows a Ptolemy co-simulation of the amplifier using an envelope tracking bias and shaping table to provide a constant gain of 11 dB. As in Section 6.1, the setup for this co-simulation came from the ADS example, **$HPEESOF_DIR/examples/LTE/LTE_FDD_UL_Tx_wrk**. The setup notes specified in Section 6.1 also apply to this simulation example.

From the **LTE_Cosim_ET_Bias_11_dB_Gain_EVM** data display in Figure 29, it's possible to see that there is a lower EVM with ET than with a fixed bias. Additionally, the mean output power is lower (19.39 dBm versus 20.21 dBm) and the drain efficiency is higher (23.29% versus 12.36%) with ET, as compared to using a fixed bias.

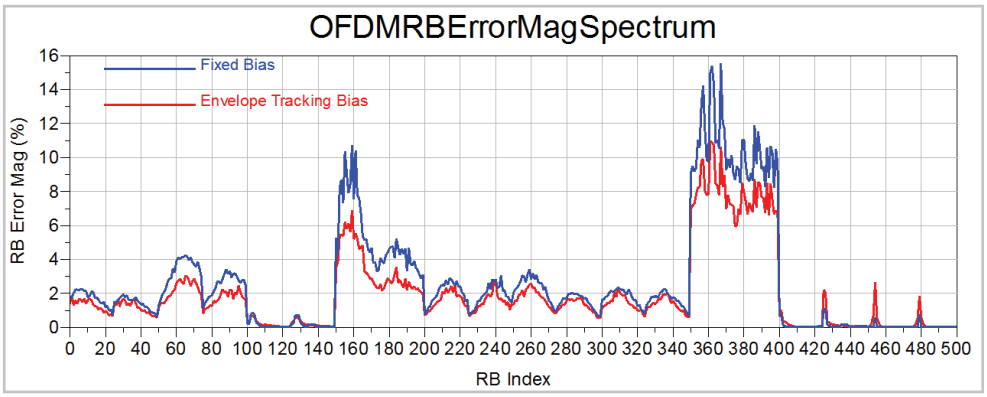

Figure 29. Ptolemy co-simulation results with ET employed.

The corresponding L**TE_Cosim_Fixed_Bias_EVM_alt** data display shows the power and efficiency performance of the amplifier during arbitrary time intervals from the simulation. During the burst from 7 to 8 msec, the drain efficiency and operating power gain with ET on are given by Figure 30. Notice that this is the same data as was shown in Figure 27 for a fixed drain bias.

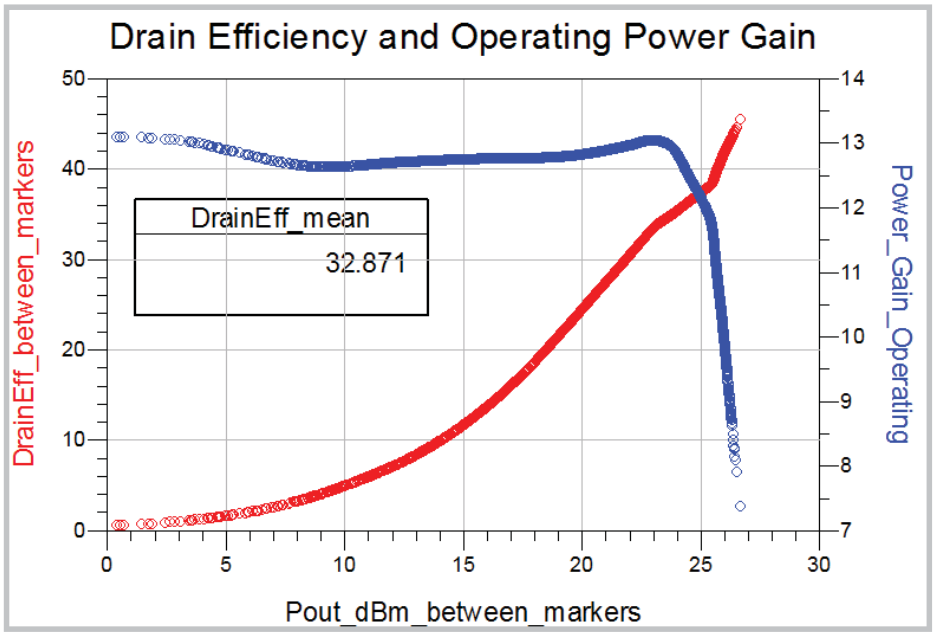

Figure 30. Drain efficiency and operating power gain during the 7 to 8 msec. burst, with ET on.

7.0 Using the 89600 VSA Software to Display Results

One final method for simulating a PA with a fixed drain bias uses the 89600 VSA software (installed on a PC running ADS) to post-process and display the simulation results. This method is especially useful to those familiar with the VSA. Note that ADS 2011.10 requires a version of the VSA software that's earlier than 15.0.

The **LTE_Cosim_Fixed_Bias_VSA** schematic in the **4. Simulations with Fixed Bias** folder simulates the amplifier with a fixed bias and displays the results as shown in Figure 31.

The results are recorded on the VSA sink, with **TclTkMode=NO and RecordMode=YES**. The results can be saved on the VSA display window by selecting **File>Save>Recording** (Figure 32). In this case, the results were saved in the data directory of this workspace. They can be recalled by selecting **File>Recall>Recall Recording**, selecting the file desired, and then hitting the Play button to see the results. Comparing the **Fixed_Bias_12dBm.sdf and ET_Bias_11_dB_Gain_12dBm.sdf** files shows less distortion when ET is active.

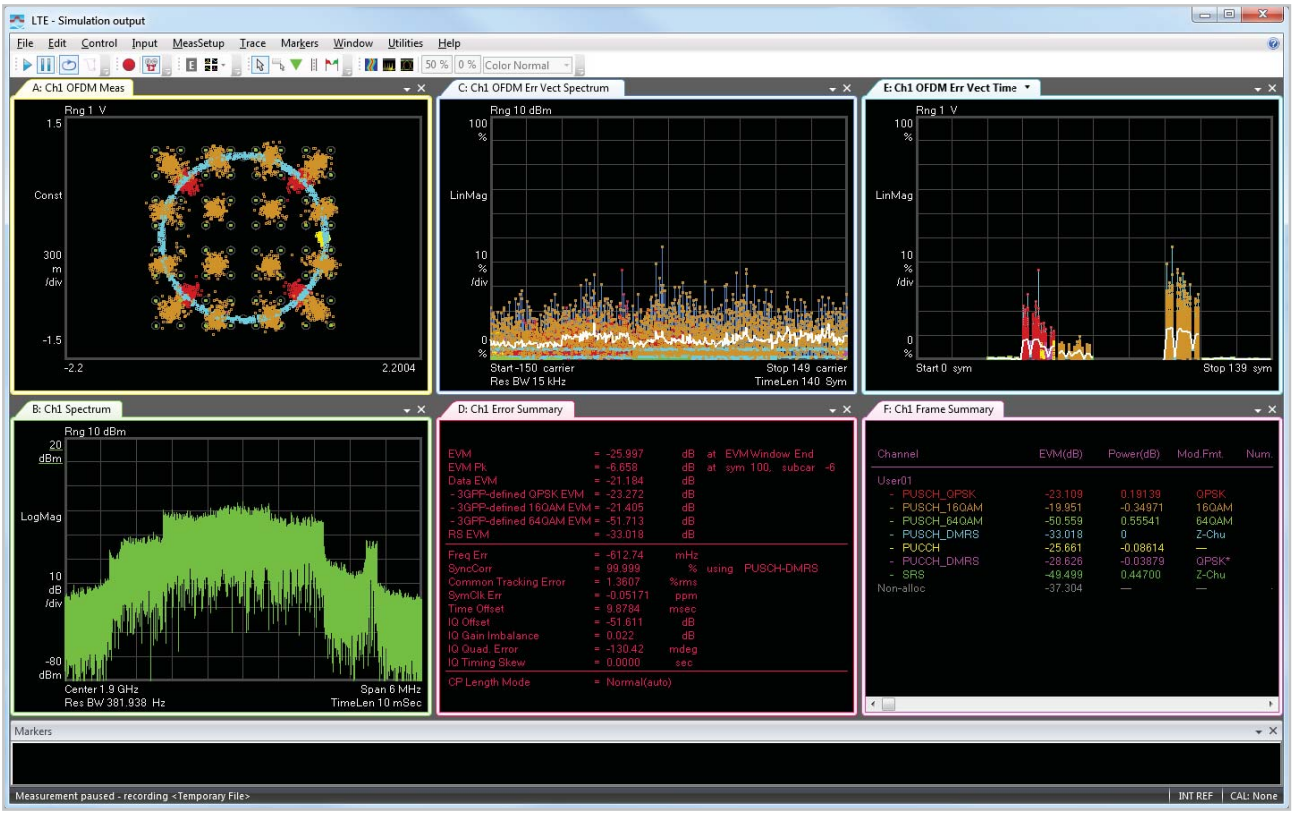

Figure 31. Simulation results for an amplifier with a fixed bias.

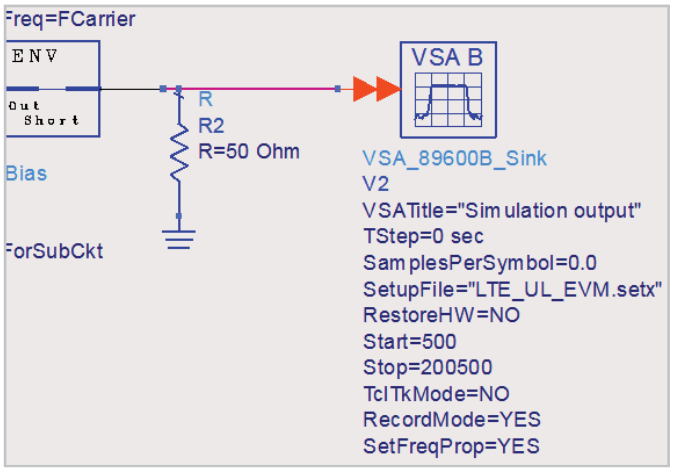

Figure 32. Simulation results are recorded on the VSA sink.

8.0 Modeling Effects That Influence Distortion

In simulation, it is easy to introduce non-idealities that cause distortion. These effects include the finite slew rate in the bias modulator, the timing skew between the RF signal path and bias modulation signal path, and the finite bandwidth of the circuitry used to implement the bias modulator. Each of these effects can be modeled using ADS.

8.1 Modeling the Effects of a Finite Slew Rate in the Bias Modulator

The **5. Envelope Tracking with Constant Gain, Modeling a Finite Slew Rate in the Bias Modulator** folder contains a schematic (**LTE_Signal_w_ET_Bias_11_dB_Gain_Finite_Slew_Rate**) that can be used to model the effects that occur when the bias modulator does not slew as quickly as the modulation signal during ET. As shown in Figure 33, the schematic is similar to earlier ones presented in this Application Note, however in this case an OpAmp model with a finite slew rate is included in the drain bias line.

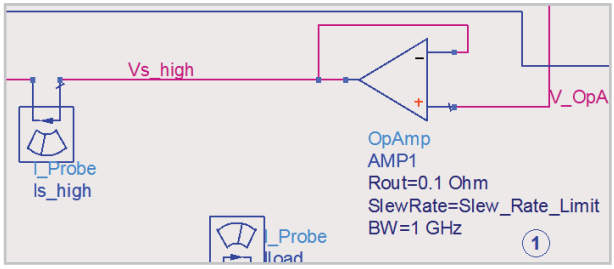

Figure 33. Schematic for modeling effects of a finite slew rate in the bias modulator.

This OpAmp model has many parameters for modeling different non-idealities. Here, the SlewRate parameter is set to dominate the behavior.

The **Slew_Rate_Limit** parameter is swept from 1e7 to 1e8 V/sec. The plot in Figure 34 shows the slew rates of the drain bias voltage with **Slew_Rate_Limit** set to both 1e7 V/sec and 1e8 V/sec. The diff() function computes the finite-difference derivative of a trace. The plot in Figure 35 (upper image) shows the voltages at the input and output of the OpAmp. When the **Slew_Rate_Limit**=1e7, the AM-to-AM distortion is large (Figure 35, lower image).

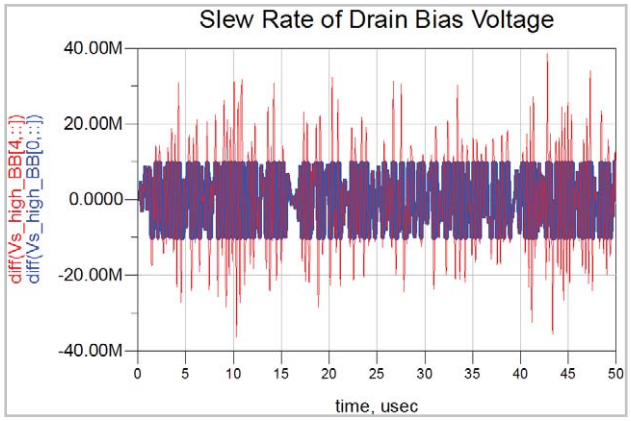

Figure 34. Plot showing slew rates of the drain bias voltage.

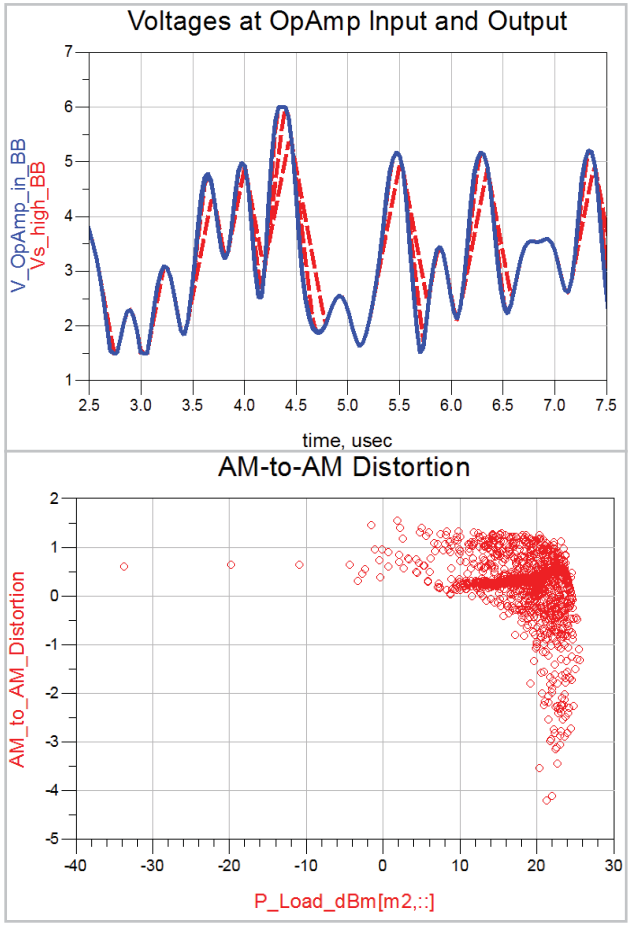

Figure 35. The upper plot shows the voltages at the input and output of the OpAmp, while the lower image shows a large AM-to-AM distortion.

8.2 Modeling the Effects of a Time Delay Difference between the RF and Bias Modulation Signal Paths

The **5. Envelope Tracking with Constant Gain, Modeling a Time Delay Difference Between the RF Input and the Bias Modulator** folder offers a schematic (**LTE_Signal_w_ET_Bias_11_dB_Gain_Delay**) to simulate the effects of a timing skew between the RF signal patch and bias modulation signal path. This schematic is similar to the other schematics presented in this Application Note, with one exception—time delay subcircuits have been added in the RF and bias signal paths (Figure 36).

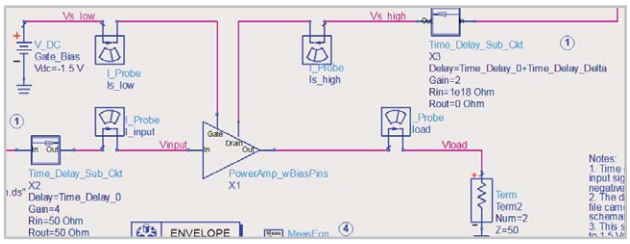

Figure 36. Schematic for modeling timing skew effects

Notice that the time delay subcircuits have **TimeDelay** blocks with voltage-controlled voltage source (VCVS) components (Figure 37). This ensures the time delay is well behaved, regardless of the impedances connected at its inputs and outputs.

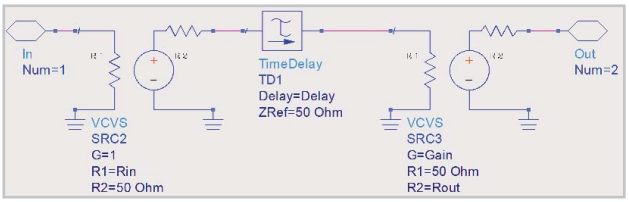

Figure 37. Time-delay subcircuit schematic.

The plot in Figure 38 (upper image) shows the timing skew when the bias modulation waveform lags the RF input signal magnitude by 20 nsec. Also shown is a graph of the raw EVM versus time delay difference data (lower image). Notice that the AM-to-AM distortion is quite severe when the delay is ±20 nsec (Figure 39).

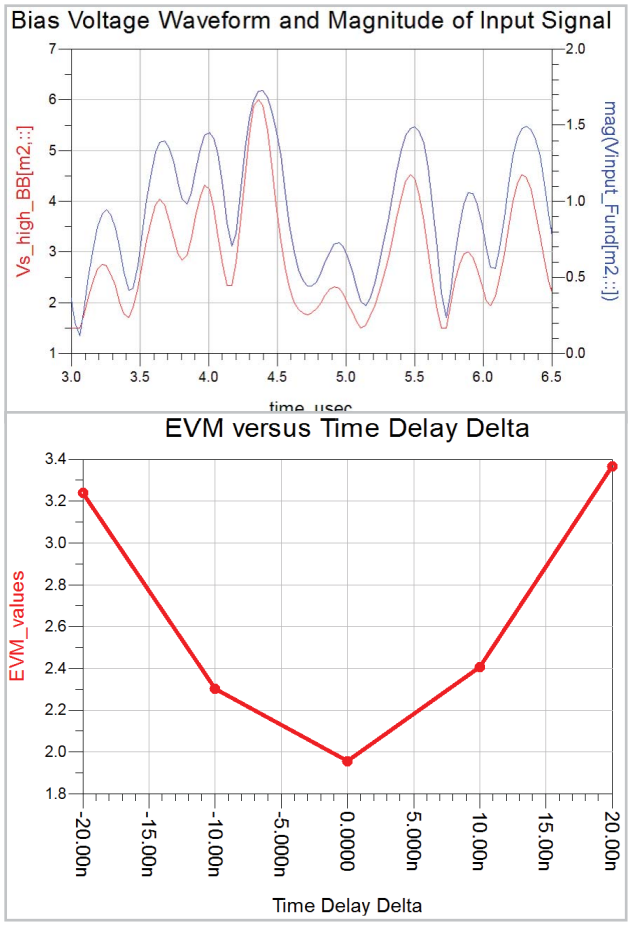

Figure 38. The left-most image plots timing skew, while the right-most image plots the raw EVM versus time delay difference.

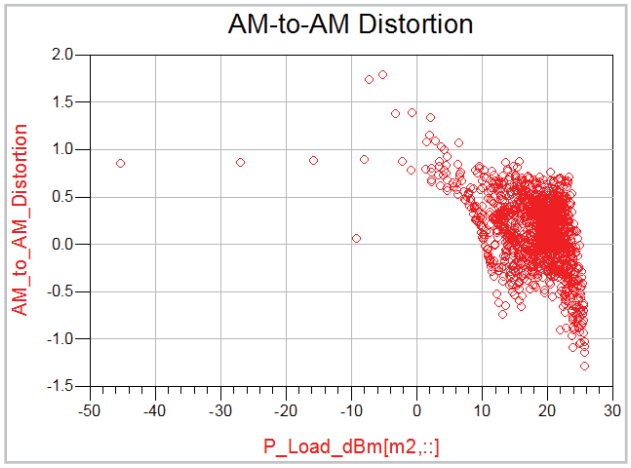

Figure 39. Plot of AM-to-AM distortion with a bias modulation waveform lag of 20 nsec.

8.3 Modeling the Effect of Finite Bandwidth in the Bias Modulation Signal Path

The **5. Envelope Tracking with Constant Gain, Modeling Finite Bandwidth in the Bias Modulator** folder has a schematic (**LTE_Signal_w_ET_Bias_11_dB_Gain_BW_Limit**) for simulating the effect of a finite bandwidth in the circuitry used to implement the bias modulator. This schematic is similar to those previously shown, except that a 1-pole RC low-pass filter has been added in the bias signal path (Figure 40).

In this case, the 3-dB bandwidth **f_3dB** of the filter is swept during a simulation that uses the short **VtDataset** input source. A plot of the raw EVM data as a function of this bandwidth is shown in Figure 41. The plot indicates that as long as the filter bandwidth is greater than 2-3x the bandwidth of the RF input signal—in this case, 5 MHz—the degradation in EVM will be small.

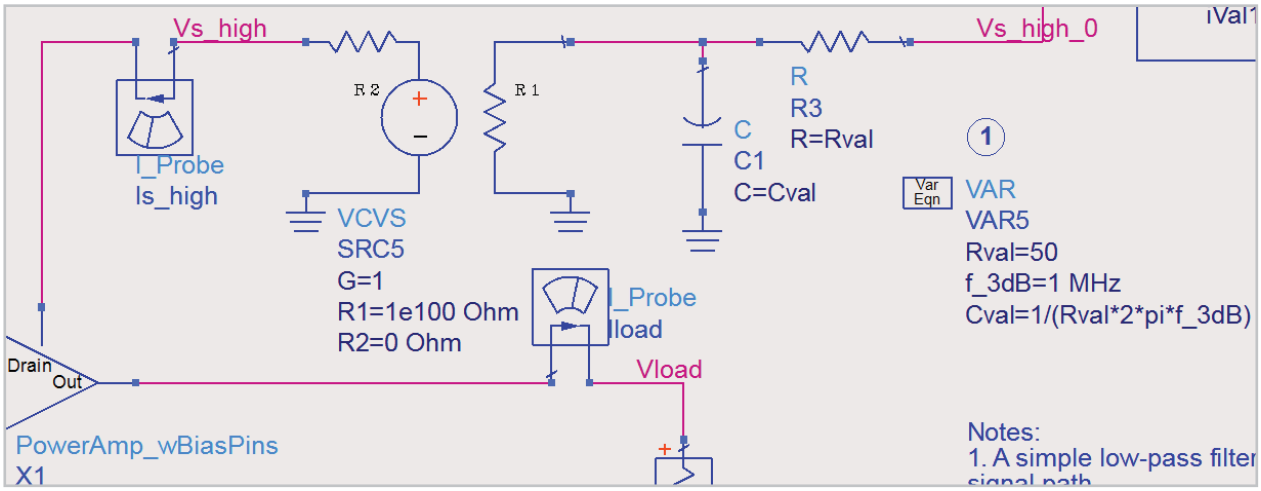

Figure 40. Schematic for simulating finite bandwidth in the bias modulation signal path.

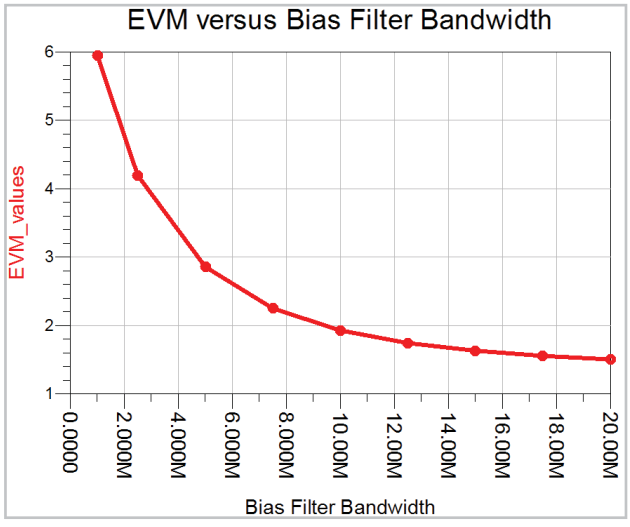

Figure 41. Plot of raw EVM data versus bias filter bandwidth.

9.0 Summary

Envelope Tracking offers a way to bolster low-efficiency in a power amplifier's back-off region. Agilent's ADS platform is well suited to quickly and accurately simulate ET, and model the various factors that may introduce distortion in a real system. There are three different ways to setup and run simulations: using data generated from a different Ptolemy simulation, using Ptolemy co-simulation or using the 89600 VSA to post-process simulation results. Using ADS with the 89600 VSA software provides users an alternate means of displaying simulation results. The viability and functionality of these solutions were successfully proven through their application to a simulation of ET applied to a transistor-level PA model. Most of the simulation setups used in this example are also applicable when simulating an X-parameter* model.

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