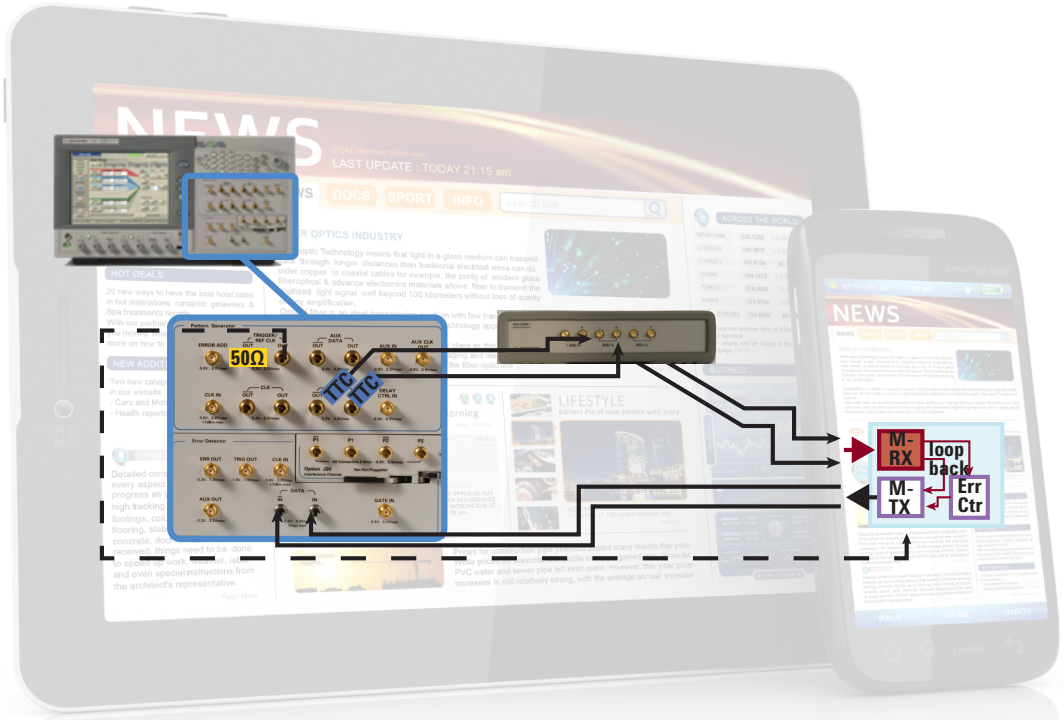
How to Test a MIPI M-PHY High-Speed Receiver

Challenges and Agilent Solutions

Application Note



Anticipate ___Accelerate ___Achieve

Agilent Technologies

Table of contents

1. Introduction 3
1.1. The MIPI alliance 3
2. The M-PHY interface 5
2.1 Data rates and tolerances 6
2.2. M-PHY RX state machine 7
2.3. M-PHY jitter specification for high-speed RXs 8
2.4. Specification of receiver eye opening and accumulated differential receiver input voltage 9
3. Setup and calibration procedure for TX test 10
3.1 MIPI M-PHY RX test 10
3.2 Set up used for HS_RX test and calibration of the high-speed stress signal 11
3.3. Verifying the test setup 11
3.4. The Jitter cocktail for HS_RX tolerancing 12
3.5. Realization of the RX-test stress signal with Agilent J-BERT N4903B 13
3.6. Excursion: PWM mode 17
4. The RX Test 19
4.1. DUT-RX clocking 19
4.2. RX test modes 19
4.3. Verifying BER $<10^{-10}$ 21
4.4. The Agilent N5990A-165 automation software for calibration and test 22
5. Summary: Testing MIPI M-PHY RXs with Agilent test solution 22
6. Appendix 23
6.1 Test equipment 23
6.2. Specifications for RX-stress signal 24
6.3. References 25
6.4. Glossary 26

Word of caution

At the time of issue of this document MIPI M-Phy rev. 3 was released, while the work on M-Phy rev. 4 got underway. Addressing Gear 3 data rates with rev. 3 generated new requirements and has resulted in new specifications and device capabilities. Addressing Gear 4 with rev.4 will probably result in new requirements as well, which are not reflected throughout this paper.

Conformance test suite (CTS) rev 1.0 was released only covering rev. 1 and 2 of the M-PHY specification. Changes and additions are to be expected.

The reader is therefore advised, before following all statements and procedures of this application note, to check the current version of the specification / the CTS for possible changes versus the versions mentioned above.

About this document

This application selectively describes critical parts of the MIPI M-Phy-specification and related receiver (RX) tests. It is not a so-called Method of Implementation (MOI) and therefore does not completely cover all aspects of the specification and the related testing. It describes the main properties of the M-Phy interface, especially the definition of the jitter stress signal, its calibration, and aspects of High Speed Receiver (HS_RX) testing.

Introduction

1.1. The MIPI alliance

The rapid spread of cell-phones from simple voice-capable devices to smartphones or even tablet PCs with the constant addition of capabilities and features came along with a proliferation of interfaces between ASICs and "sensors" or "terminal devices" such as microphones, cameras, loudspeakers, displays, and peripheral electrical devices as depicted in Figure 1, which made ASIC development and system integration an increasingly difficult task.

The MIPI organization was founded in 2003 (MIPI at that time stood for Mobile Industry Processor Interface) in order to structure the intestines of *"mobile devices ranging from smartphones, wireless-enabled tablets and netbooks"* and to *"benefit the entire mobile industry by establishing standards for hardware and software interfaces in these devices"* enabling reuse and compatibility in mobile devices making *"system integration less burdensome than in the past." "The distinctive requirements of mobile terminals drive the development of MIPI Specifications."*

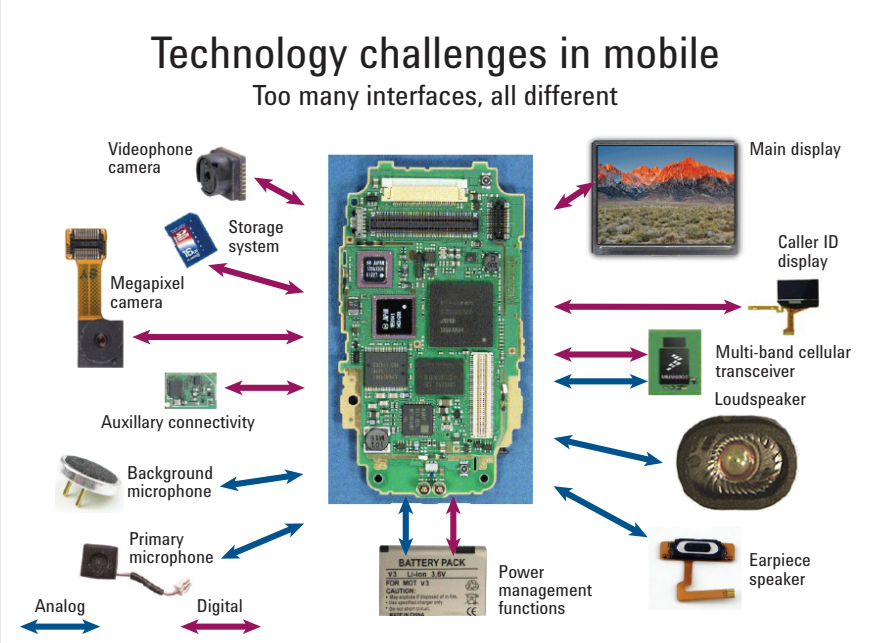


Figure 1. Smartphone with a variety of interfaces to sensors, terminal and electrical peripheral devices.

1. *Citations taken from MIPI website: http://mipi.org/*

This application note will focus on those interfaces that transport digital data with an aggregate BW in the multi Gb/s range, either per lane or on multiple lanes. In contrast to other digital standards, such as USB or PCIe, which are monolithic, i.e. contain both protocol as well as phy-layers, most of the high-speed MIPI standards are not, i.e. different protocols reside on the same common phy-layer (see Figure 3).

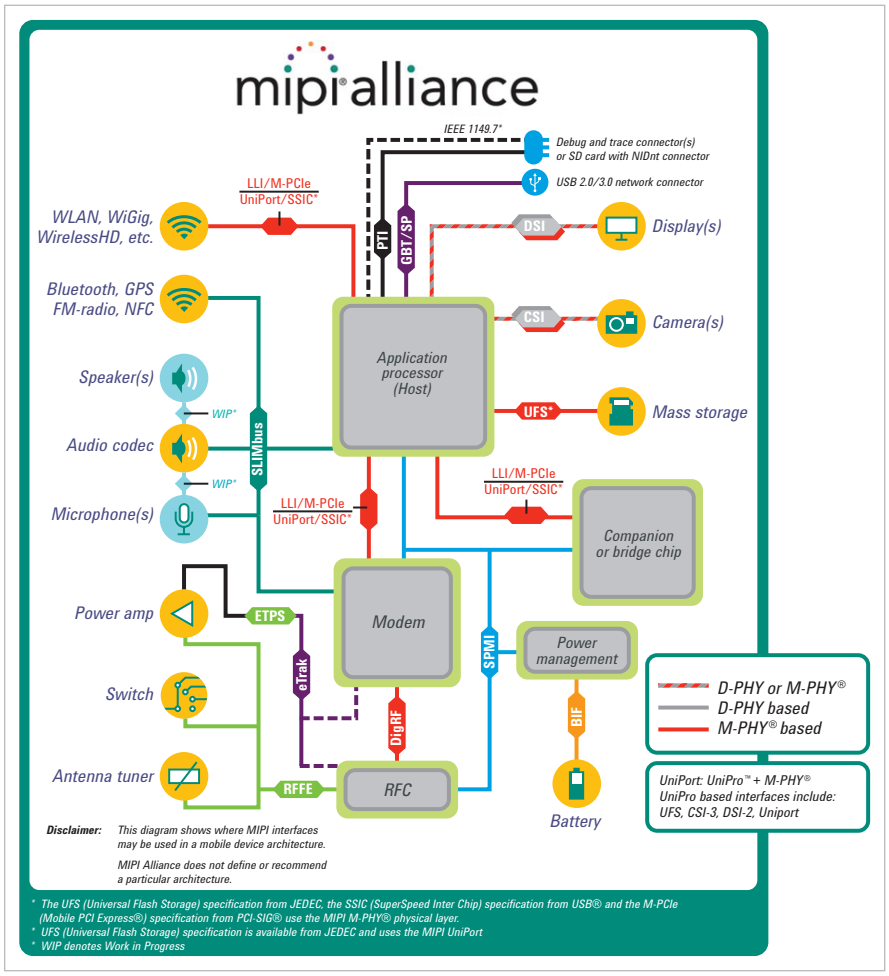


Figure 2. Block diagram of a mobile device such as a smartphone and the use of buses standardized through the MIPI alliance.

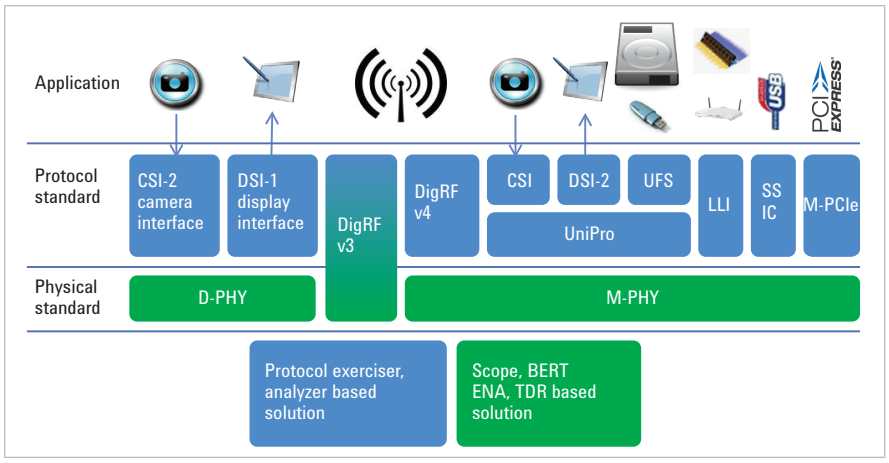


Figure 3. Structure of MIPI high-speed digital standards with separate protocol- and phy-layer.

2. The M-PHY interface

Throughout this application note we will focus on the high-speed receiver (HS_RX) test according to the M-PHY standard. Before doing this, some properties of the M-PHY specification shall be discussed.

Figure 4 shows an M-PHY *link,* which may consist of *sub-links* that are formed of a set of *lanes* combining an *M-PHY transmitter (M-TX)* and an *M-PHY receiver (M-RX)* connected through a differential *line.* All TXs and RXs respectively are combined in a *port.*

- MIPI M-PHY lines are differential, data is always transmitted differentially, 8B/10B coded
- MIPI M-PHY features a high speed and a lower speed, low power mode, same as in D-PHY
- High and low voltage swing operation can be commonly selected for both modes
- Terminated (100 Ohm differential) and not terminated operation (for power saving purposes) can be selected independently for high speed (default = terminated) and low power mode (default = not terminated)

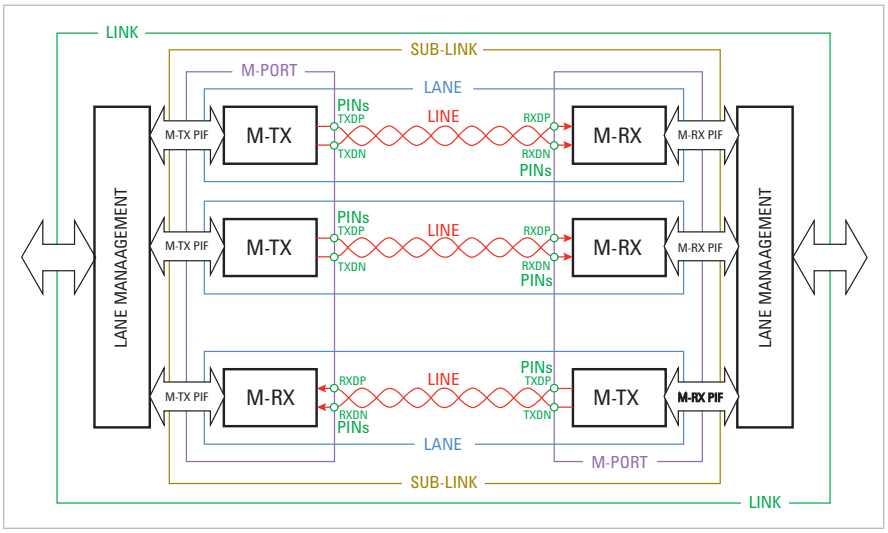


Figure 4. Example of an M-PHY link, visualizing the terms link, sub-link, port, lane, line, and pin. A link may consist of sub-links, that are formed of a set of lanes which combine an M-TX and an M-RX connected through a line. All TXs or RXs respectively are combined in a port.

2.1. Data rates and tolerances

For high speed transmission, 4 speed classes (so-called gears) have been defined / projected. The data rate always doubles from one gear to the next as shown in Figure 5.

- Two different so-called "module"-types have been defined, which differ in the realization of the low power mode:
  - Type I devices use pulse width modulation (PWM) in eight different speed classes (again, so-called gears), of which Gear 1 to Gear 7 are also spaced by a factor of two, but are overlapping, as each gear covers a range of 3:1 in allowable data rate. Gear 0 extends down to 10kb/s, see Figure 5. (Type-I devices also specify the optional use of an Optical Media Converter (OMC) as extension of M-PHY lines; the specification of optical TX, RX and fiber, however, are outside the scope of the M-PHY spec.)
  - Type II devices transmit data with the system clock rate and non-return to zero (NRZ) format.

"A" and "B" rates for high speed mode

The high speed data rates are derived with an integer multiplying phase locked loop (PLL) from one of the commonly used low frequency reference clocks of 19.2, 26, 38.4 or 52 MHz. The first common multiple of the two lower reference clocks in the GHz range is 1.248 Gb/s (see Table 1). This and the x2, x4, x8 data rates are the so-called "A"-rates of the respective gear.

In order to give system integrators some degree of freedom avoiding interference between different digital buses or with radio frequency bands for each gear, a second, slightly higher data rate (+10 to 20%), the "B"-rate, was desired. Unfortunately no common integer multiple of both reference clock frequencies exists in the target data-rate range. Frequencies closest to each other are 1.4592 Gb/s = 76*19.2 MHz and 1.456 Gb/s=56*26 MHz.

However, instead of defining these two rates (e.g. as a B1- and B2-rate), the geometrical average, which is about 1100 ppm larger / smaller (and which in practice will probably never occur), was defined as the nominal B-rate making a relatively large tolerance range necessary when taking a relatively relaxed tolerance of several hundred ppm of the reference clock itself into account: ±2000 ppm was finally chosen.

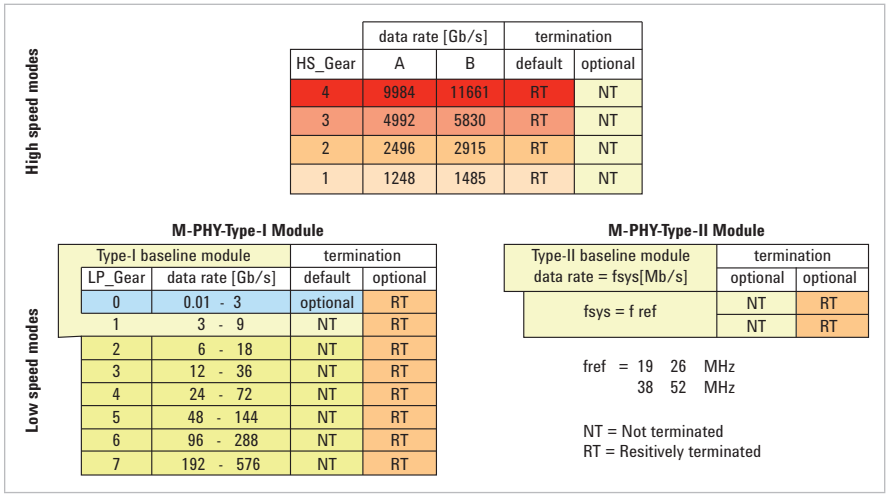


Figure 5. MIPI M-PHY data rates for high-speed Gears 1, 2, 3 and 4 (projected) A and B and low power data rates for type I modules (using pulse width modulation (PWM) format with Gears 1-7 data rates (Gear 0 is optional) and type II modules using NRZ format with system clock data rate).

Ref-clock / MHz	A		B		
	Multiplier	HS-rate/ Gb/s	Multiplier	HS-rate/ Gb/s	Deviation from avg / ppm
19.2	65	1.248	76	1.4592	+1098
				avg: 1.4576	
26.0	48	1.248	56	1.456	-1098

Table 1. Gear 1 data rates and relation to reference clock.

2.2. M-PHY RX state machine

From an end user's point of view, one of the most important aspects of mobile devices is battery life. MIPI interface standards are taking care of this topic being designed for power efficient data transmission in bursts with a high speed and a low power mode (lower speed, not terminated – see Figure 5) plus power saving idling states.

Figure 6 shows the state diagram for Type-I M-RX. Three different power saving idling states are shown.

1. Hibernate (Hibern8) is the "deepest" power saving state. The data line is kept open and no signal is driven (DIF-Z) while in this state. A transition into one of the other power saving states is possible (signalized by driving a "0" on the differential data line (within MIPI called "DIF-N"), but not directly into data transmission.
2. "Sleep" state; line is driven DIF-N; allows transition into low power PWM burst mode data transmission, signaled by a "1" on the differential data line (within MIPI called DIF-P).
3. "Stall" state; line is driven DIF-N; allows transition into High speed NRZ burst mode data transmission, signaled by a "1" on the differential data line (DIF-P).

When are the different modes and gears (of a type-I module) used?

There is no global answer to this question. For initialization, low power mode (Gear 1 for type-I modules) is used, which is generally fast enough to transmit commands. However, even high speed bursts carry commands at their end, e.g. signaling whether to stay in high speed mode (i.e. go to "stall" and stay there) or switch to low speed mode (i.e. go to "stall" and then initiate a re-configuration trigger (RCT) to move to "sleep"). While especially for type-I modules with their fastest PWM gear going up to >200 Mb/ data bandwidth (BW) would in some cases be sufficient to transport user data, from a systems designer's point of view it may be hard to predict how much data BW will be required next. So the optimum usage of the different high and low speed modes and gears in the end can determine end product features such as performance and battery life.

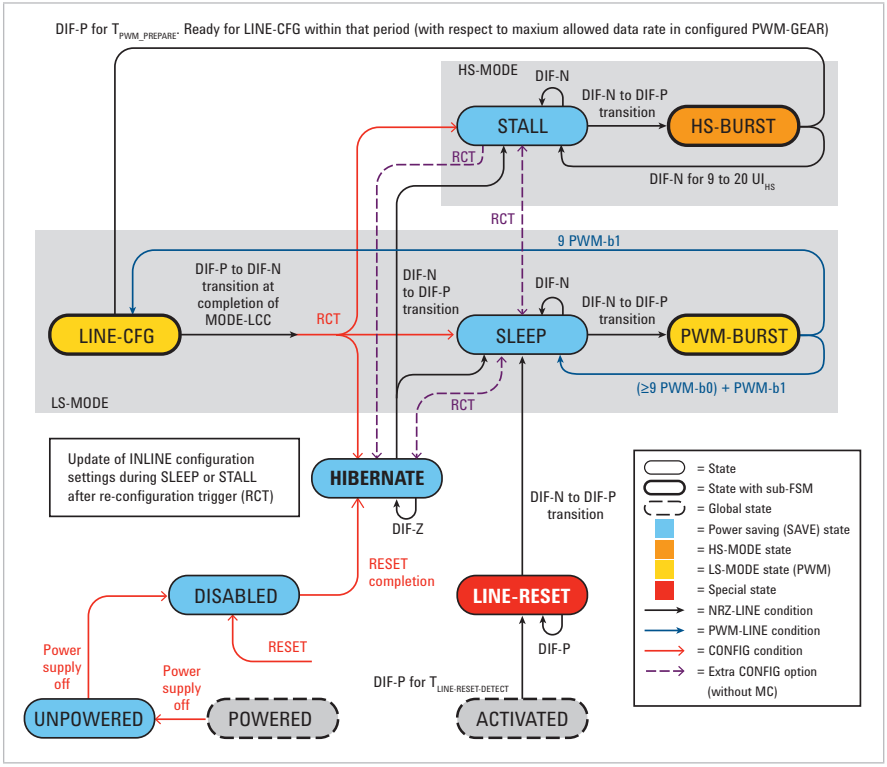


Figure 6. State diagram for Type-I M-RX.

2. $f_{L\_HS\_RX}$ is sometimes substituted with ($f_{C\_HS\_RX}$) with "C" standing for corner frequency of a filter function (or an RX CDR) below which RJ shall no more be taken into account.

2.3. M-PHY jitter specification for high-speed RXs

The MIPI M-PHY specification was derived from the phy layer of Dig_RF_v4 generalizing some of its specifics. Transmission from TX to RX under Dig_RF_v4 protocol uses clock forwarding and always operates with burst packets. Therefore serial alignment is required at the beginning of each burst. Dig_RF_v4 uses an uncritical pattern with low data dependent jitter (DDJ) for synchronization, so that the jitter for the first 30 bits (three 10B symbols) is lower than for the remaining burst.

This property of the Dig_RF_v4 interface was converted into a generic jitter specification: for frequencies above the equivalent of 30 UIs, i.e. for jitter components with $f_{jit} = f_{SJ4\_RX}$ >1/30 UI, tighter jitter limits for total- and deterministic jitter (TJ and DJ) were defined (see below) thus having converted the original "begin-of-burst" restriction into a "short-term" (=high frequency) restriction valid over the whole burst duration.

Furthermore, as Dig_RF_v4 transmission always operates with bursts requiring resynchronization at the beginning of each burst anyway, jitter frequencies below the equivalent to the burst length T_{burst} were not necessary to be specified. As M-PHY allows transmission in a so-called "continuous burst mode" and does not enforce clock forwarding but allows clock recovery on the RX side instead, it is necessary to specify (and test) TXs signal performance as well as RX's tolerance to jitter frequency components in the frequency range below $1/T_{burst} = f_{L\_HS\_RX}^2$ (this hole in the M-PHY specification was only recently closed with the rev. 3 and is therefore not yet contained in the current CTS).

Three jitter frequency bands:

1. The highest band (containing the so-called short term (ST) jitter) stretches from f_{SJ4_RX} = 1/30 UI to f_U=½ UI_{HS}.
2. The medium band jitter includes the ST-jitter completely and extends down to the so-called $f_{C\_HS\_RX}$ (which may be equivalent to the corner frequency of a respective RX-CR and which doubles with increasing gear (see Table 5)).
3. The lowest band (the jitter, which here shall be called the Long Term (LT) jitter), which is only defined since rev. 3 of the M-PHY spec, extends from $f_{C\_HS\_RX}$ downwards.

In the M-PHY spec Total Jitter (TJ) and Deterministic Jitter (DJ) are explicitly specified. Random Jitter (RJ) is only implicitly defined as the difference between both values, i.e. (ST)RJ=(ST)TJ-ST(DJ). This could lead to test conditions as extreme as DJ_{max}>DJ_{test}=0 and RJ=TJ_{max}. However, any condition other than DJ=DJ_{max} is neither described throughout this document nor in the CTS.

(Please note that for M-PHY (same as for D-PHY) the target bit error ratio is $BER_{target} = 10^{-10}$ and therefore: RJ_{pp} / RJ_{rms} = 2* CF = 2* 6.36 = 12.72 with CF standing for Crest Factor.)

It is furthermore noteworthy that the RX jitter tolerance values for TJ and DJ (per band) are higher than the maximum TX values, while the RJ values (i.e. the differences between TJ and DJ) are identical. The RX needs to tolerate a higher amount of DJ than what the TX already generates, as the channel (in PHY-terms the line) adds DDJ and crosstalk both resulting in DJ.

(In addition, when an OMC between TX and RX is present, the RX DJ (or the resulting TJ) tolerance has to be even higher, but this application note does not discuss this case).

Figure 7 shows the jitter specification according to M-PHY rev 3.0.

The amount of RJpp in the frequency range between $f_{L\_HS\_RX} = f_{C\_HS\_RX}$ and f_{SJ4_RX} = 1/30UI (let's call it medium term (MT)) can be calculated as MTRJ = sqrt ((TJ-DJ)^2-(STTJ-STDJ)^2) = sqrt (RJ^2-STRJ^2) = sqrt (0.17^2-0.1^2) = 0.14 UI.

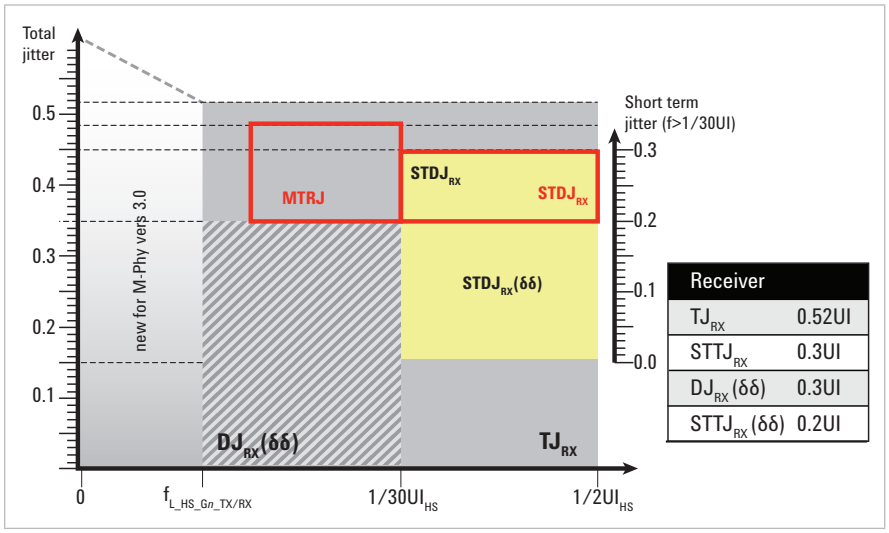


Figure 7. Jitter specification for MIPI M-PHY HS_RX, showing the three different frequency bands; please note the different vertical scales left and right of the diagram relating to total- and ST-jitter respectively.

2.4. Specification of receiver eye opening and accumulated differential receiver input voltage

In addition to the jitter of the RX input signal, the waveform of the RX input eye is specified too. This tends to be an over-determination, because test pattern (CJPat), ISI trace, and jitter completely define the waveform of the RX input eye except for a vertical scaling. The horizontal parameter, i.e. the eye width of the accumulated eye, defined as 1UI-TJ (=$T_{EYE\_HS\_G3\_RX}$) is already determined by the jitter cocktail / the TJ specification. The only degree of freedom is the vertical eye opening, i.e. the inner eye height or accumulated differential receiver input voltage ($V_{DIF\_ACC\_HS\_RX}$).

Furthermore, the dilemma of using a figure of merit which, by defining a keep out region, is well suited for TX characterization, but not for RX characterization, is solved in such a way that the specification allows the measured eye diagram to "just closely meet the keep-out region of the eye mask," shown in Figure 8, without demanding to achieve the exact shape.

- Basic terminology and parameters, such as data rate ranges, and more advanced features, such as the state diagram of the MIPI M-Phy RX, have been introduced
- Parameters of the most important high speed RX jitter and input waveform specification, such as different frequency bands, have been visualized and explained

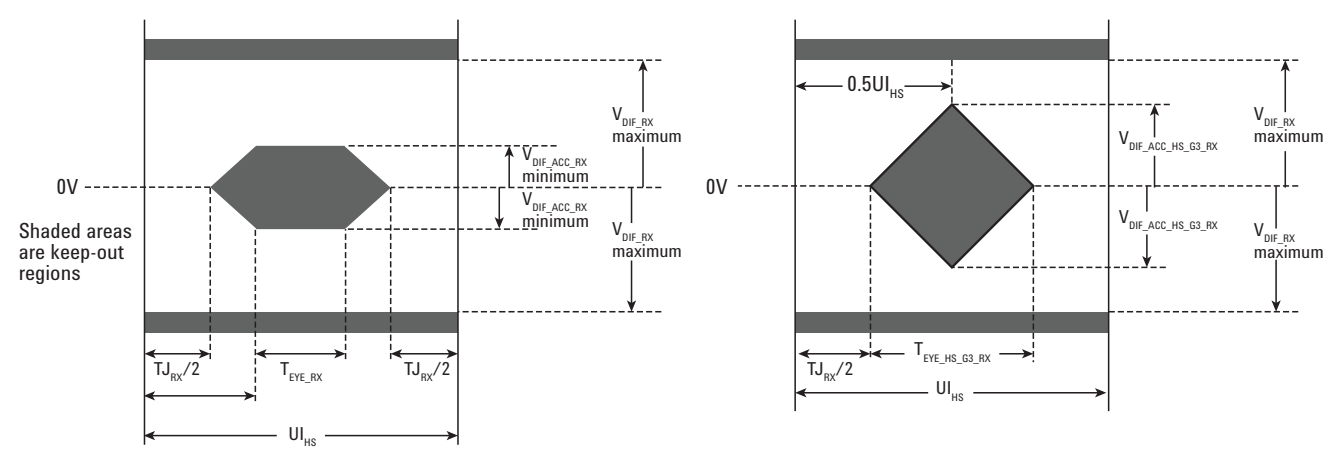


Figure 8. Receiver eye opening and accumulated differential receiver input voltage for M-PHY Gears 1 and 2 (left) and M-PHY Gear 3 (above).

3. Setup and calibration procedure for RX test

3.1. MIPI M-PHY RX test

An RX test is used to determine an RX's capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing, the input of the RX under test is stimulated with a calibrated stressed eye signal from a bit error ratio tester's pattern generator (BERT PG). This signal is composed (according to the applicable specification) of the impairments to be expected at the RX input when the RX is operating in a target system. Very often, testing a single RX is sufficient, even when the final link is composed of multiple lanes.

A simplified block diagram for an RX test is shown in Figure 9.

Proper detection of the digital content can be checked with the BERT's error detector (ED), after the RX output signal is looped back internally through a TX of the device under test DUT [3].

For the case described above the green loopback path would be utilized. The laptop computer would not be required. Details of this loopback path will be described in paragraph 4.

However, not all MIPI links are symmetrical, i.e. mode and gear settings for the involved M-RX and M-TX are not commonly supported. This would for example be the case for a display or an application processor's camera interface, as both have high speed RXs but not necessarily TXs.

Furthermore, applications (protocols) residing on M-PHY optimize their support for testing and therefore mandatory requirements for testing may not include a support for loopback mode.

In these cases, other means, such as an internal error counter / test pattern verifier (TPV) for pre-defined patterns, have to be utilized and the result has to be communicated to the external world either through a (low speed) TX (red path) or a (proprietary) programming interface of the DUT (dashed blue line) making the computer control necessary as shown in Figure 9.

The higher the data rates the more important is a thorough characterization of the related building blocks in order to guarantee interoperability. Their analog, parametric behavior, in the case of receivers, predominantly their voltage sensitivity and jitter tolerance, determines proper functionality. Design of test setup and method and careful calibration of the test signal are mandatory.

The wide range of burst mode and PWM parameters makes testing them necessary as well. The conformance test suite (CTS) dedicates a whole chapter to this operating mode and testing the related parameters; in depth description of these tests, however, is beyond the focus of this document.

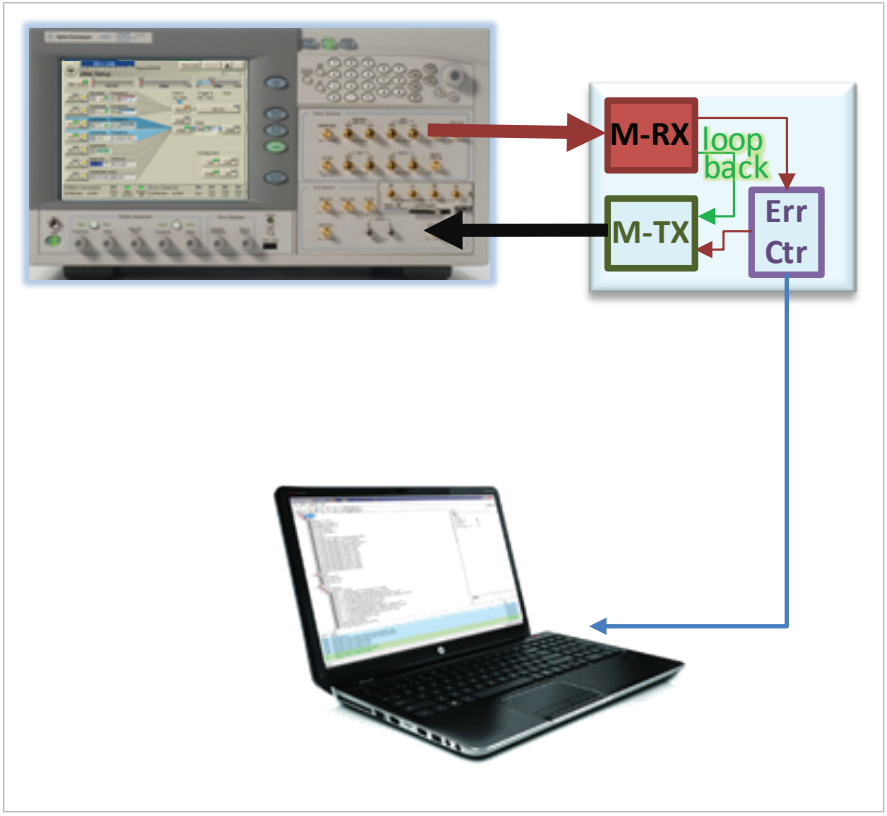


Figure 9. Simplified block diagram for an RX test.

3. *The TX is assumed to operate error free.*

3.2. Setup used for HS_RX test and calibration of the high-speed stress signal

Proper calibration of the stress signal is essential to achieve a valid and reproducible test result that eventually guarantees interoperability. For M-PHY the specifications refer to the ASIC pins (or balls) making direct measurement at that point difficult.

Searching for an easily reproducible solution for RX test and calibration of the RX stress signal, the CTS group came up with a structure as depicted in Figure 10 [2], which allows:

a. Measurement at TP, the equivalent of the RX pins after the signal passed through a replica of the breakout channel and thus suffered the same loss as the signal during test,

b. Embedding of the breakout channel into the calibration-measurement (e.g. using the InfiniiSim feature of applicable Agilent Oscilloscopes (see paragraph 6)),

c. Emulation of the layout and cabling situation in larger tablet PCs by means of the ISI conformance channel, where e.g. the display can be relatively far away (>20") from the application processor,

d. To check the total loss of the test setup including ISI conformance channel [2].

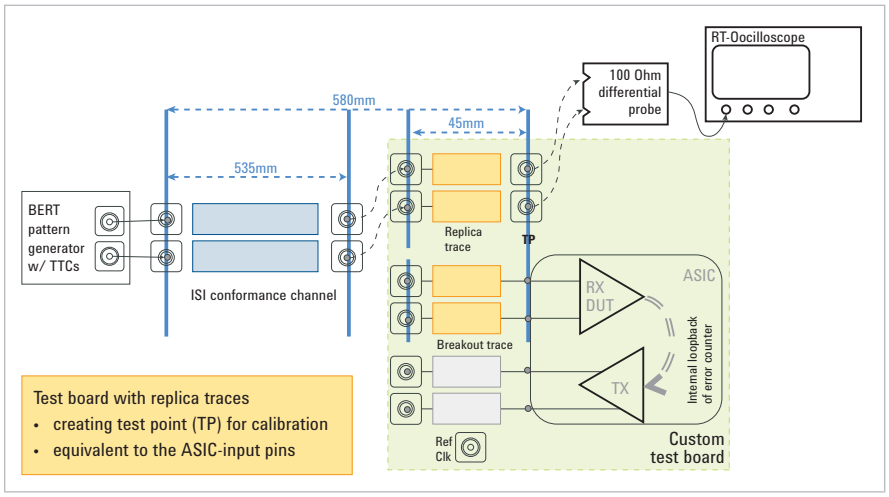


Figure 10. Set up used for RX test and calibration of the stress signal.

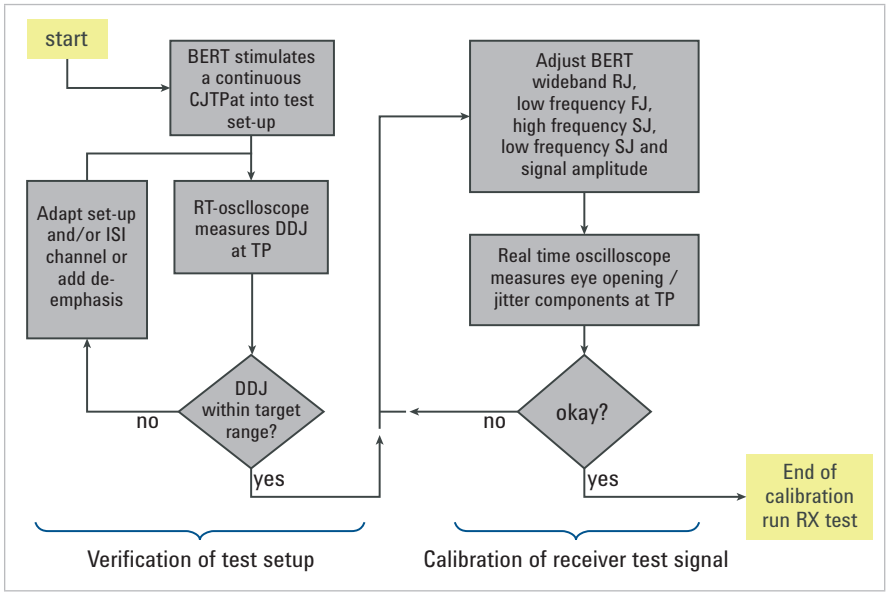


Figure 11. Flow chart for calibration of RX stress signal according to CTS rev. 1.0.

3.3. Verifying the test setup

The calibration procedure is illustrated in the flow chart depicted in Figure 11. It shows that at first the parametric conformance of the test setup has to be verified by measuring the resulting DDJ (the CTS additionally lists loss values as an alternative figure of merit). In case of significant deviation, the overall loss of the setup has to be corrected (either longer, more lossy channel or compensate excessive channel loss introducing de-emphasis through the BERT PG).

Only when the setup is correct (in terms of loss or DDJ it generates), calibration of all other signal parameters can be performed.

3.4. The jitter cocktail for HS_RX tolerance characterization

With the jitter specification as visualized in Figure 7, there are indefinite possible combinations of several jitter types to fill the jitter budget during RX test.

However, it is neither possible nor necessary to test with every combination of jitter frequencies in every jitter band or to completely fill every specified band exactly (with discrete SJ frequencies or RJ).

The M-PHY specification already lists the important jitter frequencies (see Table 5) as a first guidance. Furthermore, the CTS group came up with a suggestion of how to check the conformance of HS_RXs respectively, with a well redefined jitter cocktail.

However, it is up to the designer's diligence to sufficiently characterize an ASIC or implementation and to decide what to follow and where to deviate from these suggestions.

The CTS's suggestion is depicted in Figure 12 and the steps for calibration are listed in Table 2.

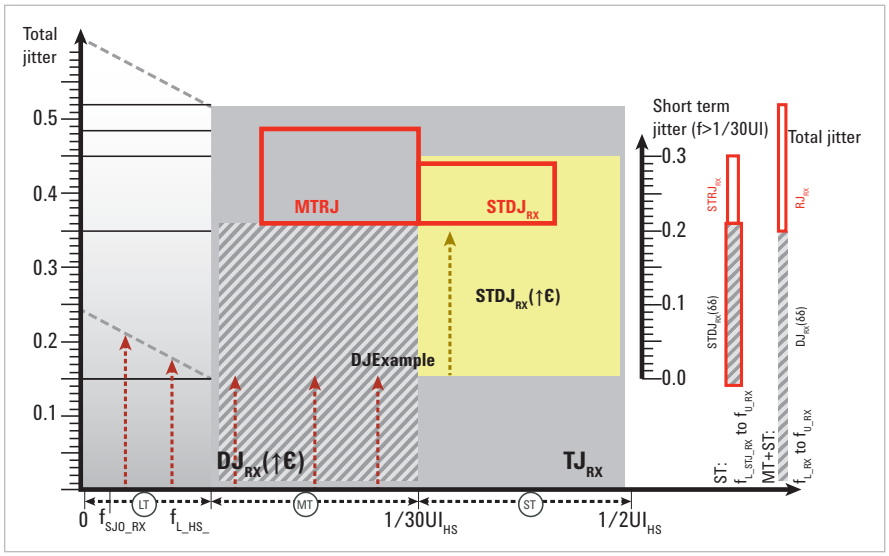


Figure 12. Jitter "cocktail" for HS_RX test.

Step	Action	J-BERT parameter	Target Value	Pattern	TIE-HP-filter
1	Adjust wideband RJ (>fL_RX) to achieve STRJ=STTJ-STDJ	RJ	0.10 UI_{pp} 7.9 UI_{rms}	clk/2 (1010)	1/30 UI
2	Add low frequency RJ (<1/30UI) to achieve RJ=TJ-DJ	BUJ	0.17 UI_{pp} 13.5 mUI_{rms}	clk/2 (1010)	fL_RX
3	Turn all RJ off; calibrate SJ (f_SJ1, f_SJ2, f_SJ3, f_SJ4)	PJ1	0.15 UI_{pp}	CJPat	off
4	Turn all SJ off; calibrate STSJ (300 MHz) to achieve STDJ (STSJ=STDJ-DDJ)	PJ2	0.2 UI_{pp}	CJPat	off
5	Turn on all Jitter types calibrated above and perform measurement				

Table 2: Steps to achieve proper calibration of jitter for RX testing (numbers refer to M-PHY CTS rev. 1.0).

Step 1 and 2 of table 2

The two RJ components are shown (only as an example) a little less wide than the specified bands (compare to Figure 7).

For the calibration of the jitter components jitter frequency filtering is required. For practical reasons calibration is performed with a clock/2 pattern (see below).

Step 3 of table 2

The M-PHY specification defines STDJ (the dashed arrow on the right side in Figure 12) as the sum of the total (not band-limited) DDJ and a short term sinusoidal jitter STSJ with f(SJ)> f_{SJ4_RX} = 1/30UI and $STSJ_{RX} = STDJ_{RX} - DDJ$.

At first glance this definition seems obvious, because commonly DDJ is assumed to consist of high frequency contributories only. However, there are more reasons for this definition:

Depending on the test pattern and the repetition of sub-patterns with specific edge displacements, the DDJ jitter spectrum can extend to fairly low frequencies particularly below f_{SJ4_RX} = 1/30 UI. Furthermore some of these specific edge displacements may be early and some others maybe late, partially cancelling each other out, hence reducing the total amount of DDJ.

Thus jitter filtering should be avoided when DDJ is present or vice versa when jitter filtering is required, as during the calibration of (ST)RJ, concurrent presence of DDJ should be avoided. Otherwise some portions of the DDJ will be filtered out and thus cancellation would be inhibited, resulting in an increased DDJ (and TJ) vs. an unfiltered measurement.

Specification rev. 3 and CTS were developed concurrently in an attempt to avoid this irritating effect.

The CTS suggests using a clock-type pattern, which doesn't show any DDJ when jitter filtering has to be used for the calibration of (ST)RJ, and using no jitter filtering when DDJ is present during calibration of SJs and TJs. As a prerequisite for this calibration method, the specification has to be a bit inconsistent and define STDJ including the whole unfiltered DDJ.

Step 4 of table 2

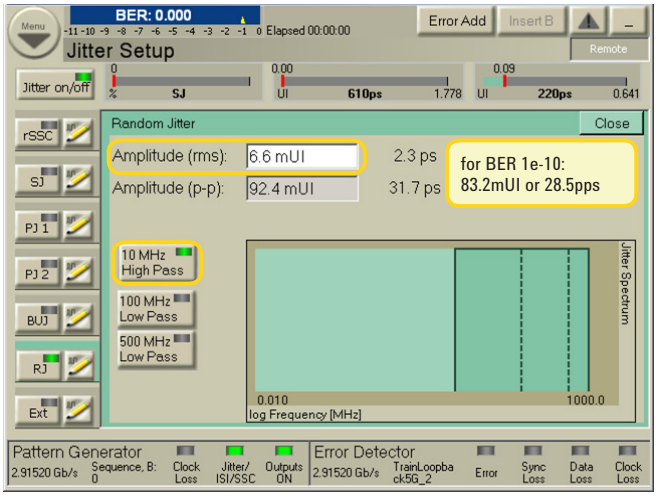
The last ingredient to complete the jitter cocktail is a second SJ tone in the frequency range between f_{SJ4_RX} and $f_{C\_HS\_RX}$ for M-PHY rev. 1 and 2 or between f_{SJ4_RX} and $f_{SJ0\_RX} = f_{C\_HS\_RX}/10$ for M-PHY rev. 3 (one of the dotted arrows in the lower left of Figure 12).

The CTS-suggested jitter frequencies are identical to those of the M-PHY specification.

3.5. Realization of the RX-test stress signal with Agilent J-BERT N4903B

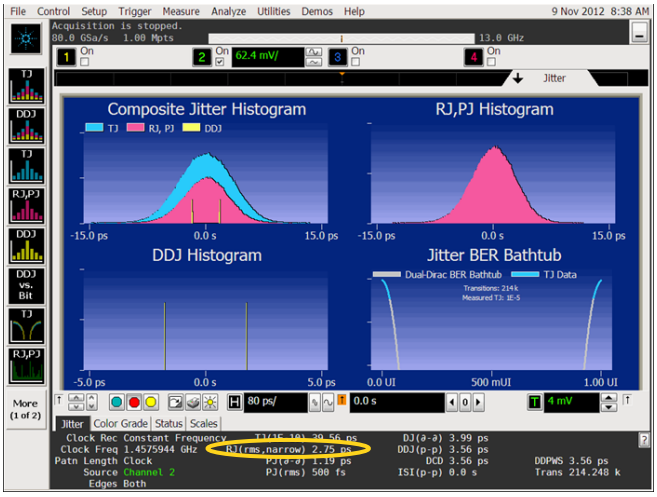
The following screenshots (combined in Figure 13) show how relatively simply and unambiguously the M-PHY jitter cocktail can be generated and calibrated. According to Figure 10, this can be achieved by substituting BERT Pattern Generator, ISI Conformance Channel and RT Oscilloscope with the Agilent N4903B J-BERT, Agilent N4915-60001 (see Figure 18) S-ATA ISI trace and the Infiniium DSA 91304A. Details about the J-BERT N4903B and its jitter generation capabilities can be found in the appropriate data sheet [3].

1.



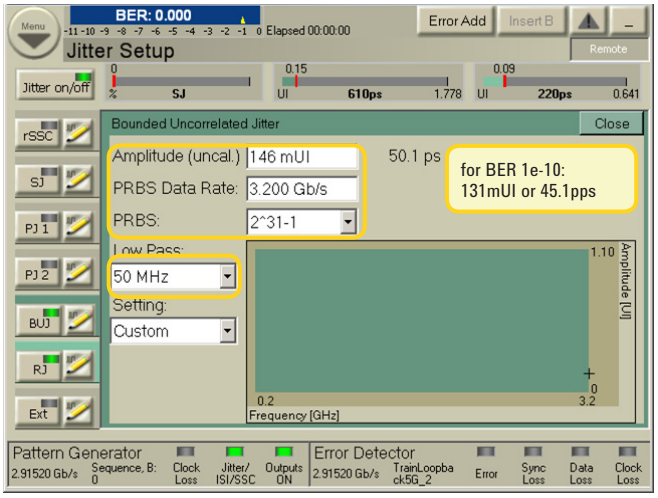
- Activate RJ (and 10MHz high pass filter)
- Note: J-BERT N4903B assumes BER 10-12 (Crest factor =7) whiletarget BER for M-phy is 10-10 (Crest factor =6.3) => 90%

2.



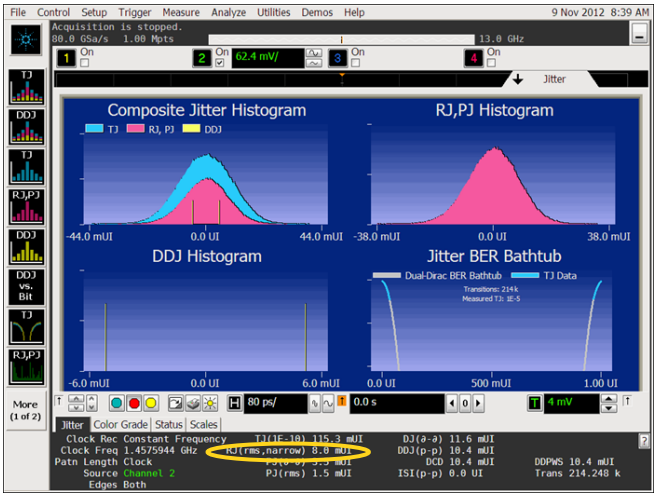
- Measure STRJ with TIE set to"Highpass" Filter with "Start Frequency" at 1/30UI = 97MHz for G2b
- Target rms-values: 2.72ps, 7.9mUI

3.



- Activate BUJ with longest PRBS at highest data rate filtered at 50MHz
- Note: J-BERT N4903B assumes BER 10-12 (Crest factor =7) whiletarget BER for M-phy is 10-10 (Crest factor = 6.3) => 90%

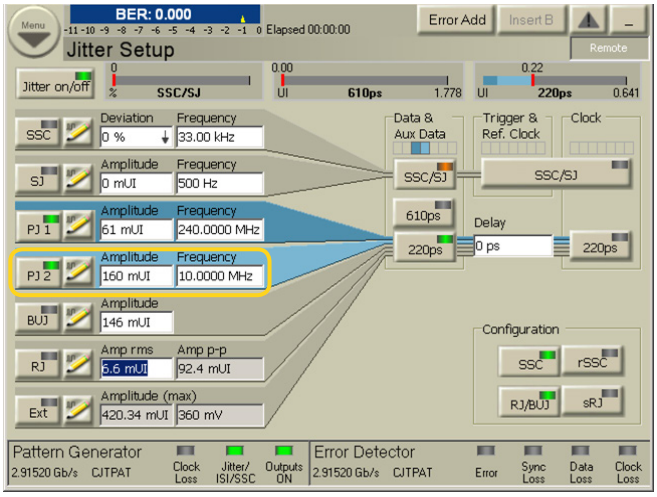
4.



- Measure MTRJ with TIE set to"Highpass" Filter with "Start Frequency" at f_SJ1 = fC_HS_RX = 4.0 MHz for G2b
- Target rms-values: 4.63 ps, 13.5 mUI

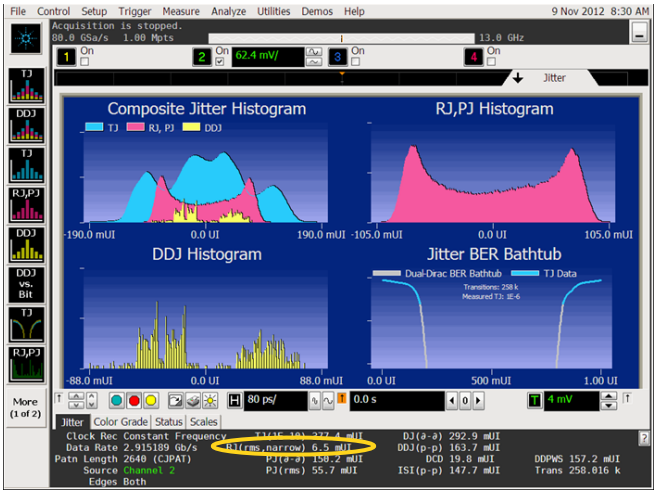
Figure 13a: Screenshots from N4903B J-BERT GUI (left) showing set up of dual-band RJ and from DSA 91304A oscilloscope showing measurement (right) of the individual RJ components.

5.



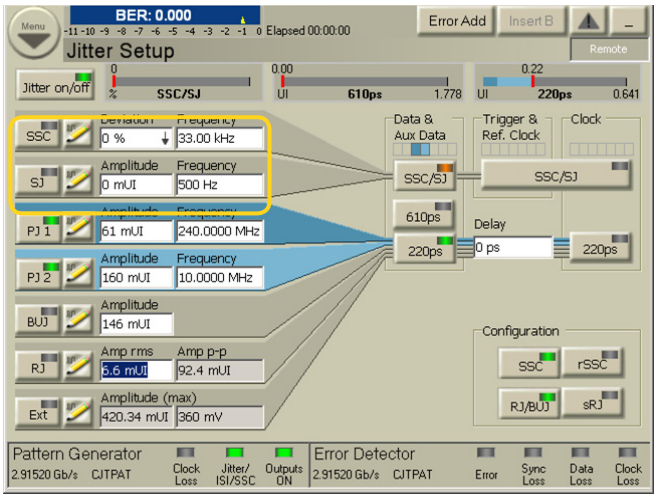
- Deactivate RJ/BUJ
- Turn on PJ2 with frequency set to f_SJ1, f_SJ2, f_SJ3, f_SJ4

6.



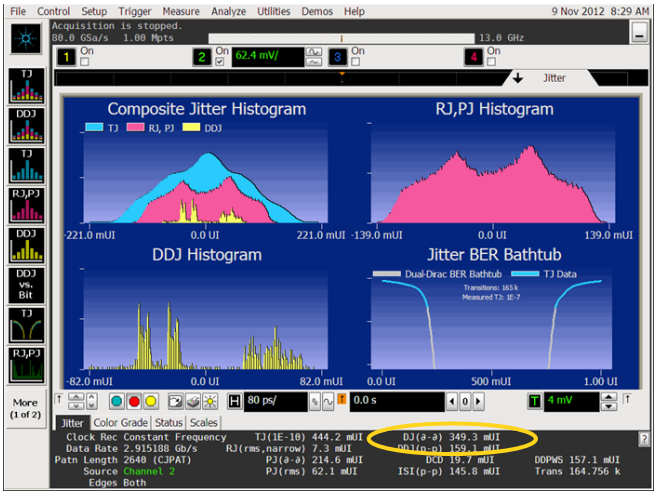
- Measure PJ with TIE turned off
- Calibrate PJ to target value of MTSJ = 150 mUI

7.



- Deactivate RJ/BUJ
- Turn on PJ2 and
- Turn on PJ1 with frequency set to >1/30UI e.g. 240 MHz

8.



- Measure PJ with TIE turned off
- Calibrate DJ to target value of MTSJ = 350 mUI

Figure 13.b: Screenshots from N4903B J-BERT GUI (left) showing set up of dual-tone SJ and from DSA 91304A oscilloscope showing measurement (right) of the individual Jitter components

After the jitter calibration is done, eye height adjustment is performed. As mentioned earlier (paragraph 2.4), the only adjustment that is necessary / the only degree of freedom that is left, is the adjustment of the differential receiver input voltage ($V_{DIF\_HS\_RX}$) / the BERT PG's output voltage, which allows to scale the waveform in a vertical direction in order to meet the inner eye height or accumulated differential receiver input voltage ($V_{DIF\_ACC\_HS\_RX}$).

The description given above applies to Gears 1 and 2. How the test has to be performed for Gear 3 has not yet been defined by the CTS group. However, combining the J-BERT N4903B with the Agilent N4916B De-emphasis Signal Converter and setting the post cursor to -6 dB[4] to compensate for the DDJ resulting from the (Gear 1 and 2) ISI conformance channel, results in the accumulated eye diagram as shown in Figure 14.

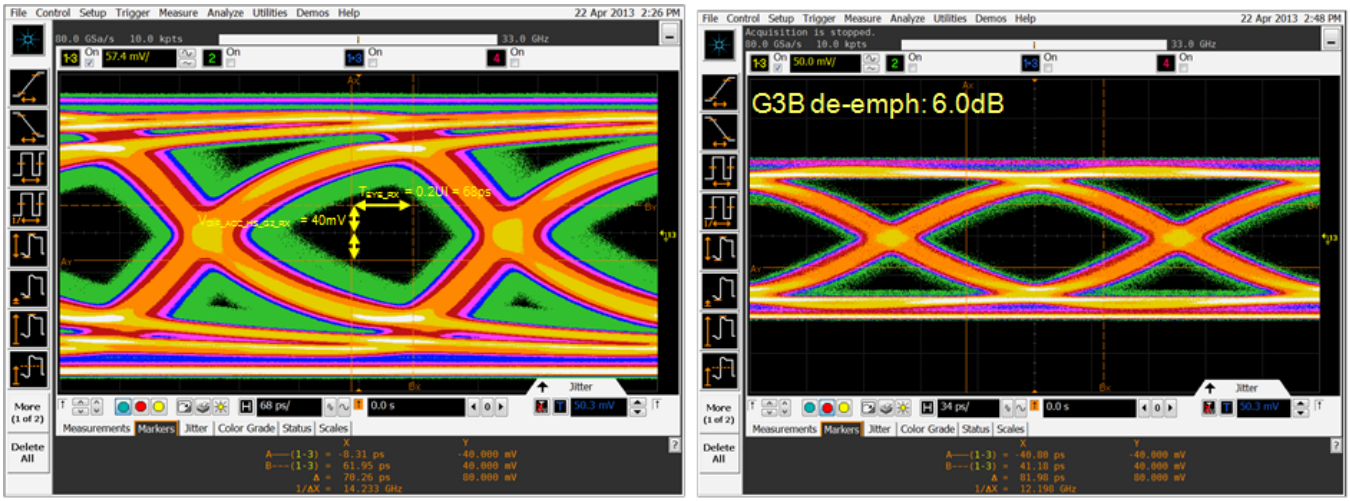


Figure 14. Accumulated eye diagrams for a CJTPat for Gear 2B (left) and Gear 3B (right) with 6 dB de-emphasis.

Summary: CTS conformant test setup, calibration and test signal generation using Agilent J-BERT N4903B

- CTS proposed test setup introduced.
- Purpose such as generation of test points usable for calibration and emulation of potentially long channel between application processor and display in a tablet PC plus method of verification explained.
- CTS's definition of jitter cocktail and method of calibration discussed.
- Realization of jitter cocktail and accumulated eye with Agilent J-BERT N4903B and 1:1 match of its capabilities and the spec. requirements shown.
- Excursion to PWM mode showed usage of BitifEye's frame generator SW for creation of PWM patterns and sequences in user terms and generation using Agilent J-BERT N4903B.

4. *The M-PHY definition of de-emphasis is different (negative sign) from other standards such as PCIe or USB. Agilent J-BERT uses those as they were released years earlier. Therefore to achieve the M-PHY specified value of 6dB -6dB must be set on J-BERT.*

3.6. Excursion: PWM mode

Although an in-depth description of any PWM related test is not within the scope of this document, some hints about how to generate these signals shall be given, because generation of commands in low power mode is necessary to set the DUT-RX to an appropriate test mode and/or to get the results of the respective (error) counters.

A high speed BERT generally works with NRZ data format. PWM is not usually supported. Furthermore, as very often a sequence of a (low speed) PWM followed by a high speed NRZ burst is required, and as a BERT cannot change its data rate on the fly, PWM data is generated using bit-multiplication of (NRZ-formatted) data. As the PWM data rate is usually some orders of magnitude lower than the NRZ-data rate, it is possible to set/vary PWM parameters such as the PWM-data rate or the ratio of $T_{PWM\_MAJOR\_TX}$ to $T_{PWM\_MINOR\_TX}$ with sufficient resolution.

In order to unburden the user from the task of translating the PWM parameters into NRZ bit sequences, Agilent's Solution Partner, BitifEye, provides the M-Phy Frame Generator SW (see paragraph 6.1)

Its graphical user interface (GUI) is depicted in Figure 15. It shows that the frame generator SW enables setting up - in user terms - the PWM parameters (3) such as gear and frequency (variation) plus the test patterns (1) in 8b or 10b domain (in most cases this is a CJpat) plus burst headers and footers such as synch sequences, markers, and cyclic redundancy check (CRC), plus burst properties (2) such as customer selectable lengths of DIF-N and DIF-P. Furthermore, it allows direct control of frequently used parameters of the connected Agilent ParBERT 81250 or J-BERT N4903B.

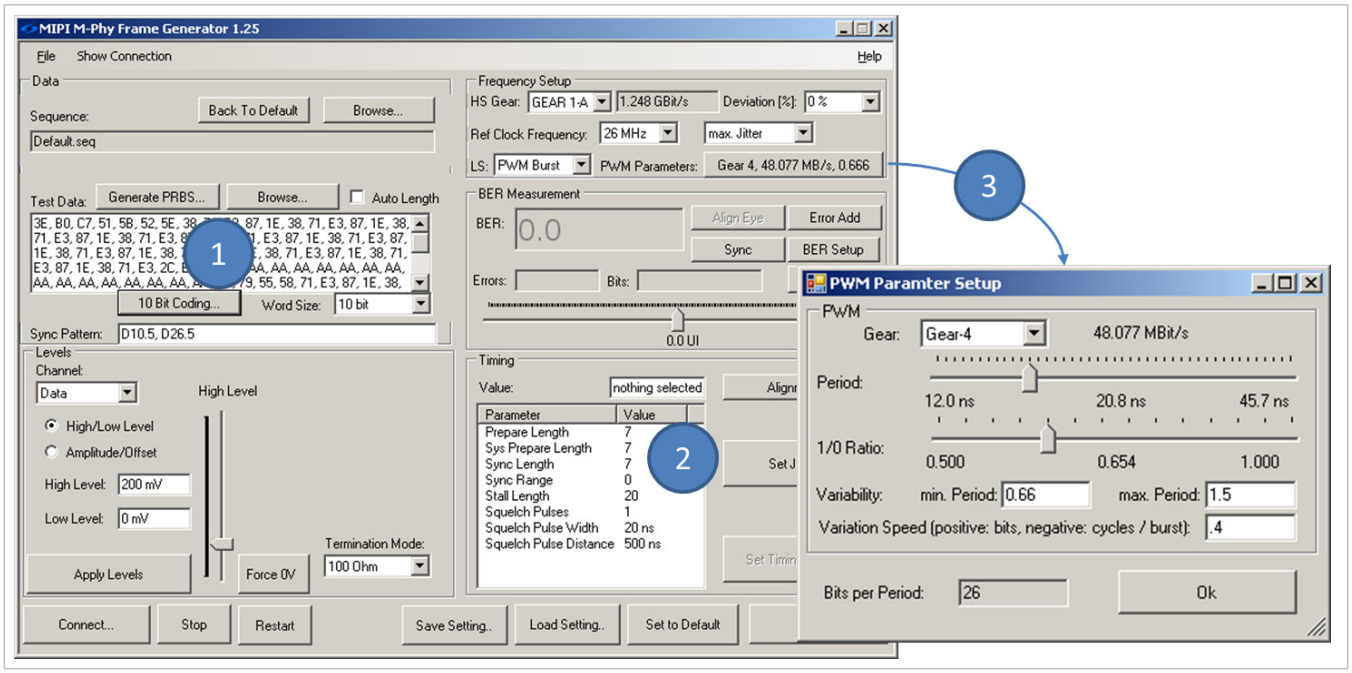


Figure 15. User Interface of the BitifEye M-PHY Frame Generator.

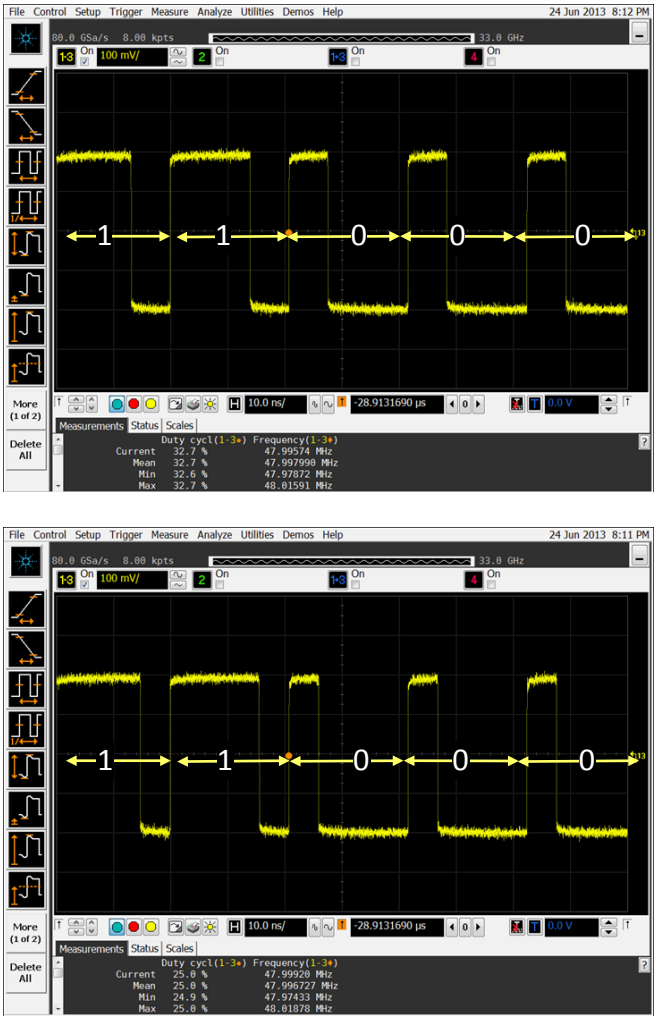


Figure 16. Section of a PWM burst showing ideal (2:1, left) and non-ideal (3:1, right) ratio of $T_{PWM\_MAJOR\_TX}$ to $T_{PWM\_MINOR\_TX}$.

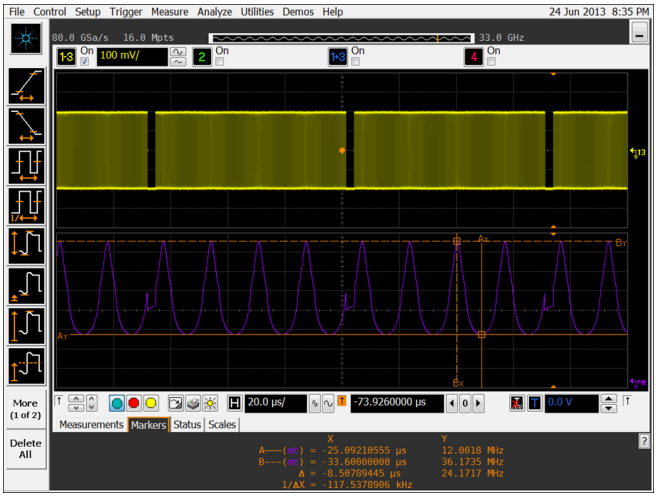


Figure 17. PWM burst signal of PWM Gear 4 for which the frequency is swept 4x per burst over the entire range, i.e. from 24 to 72 MHz. It is generated with an Agilent J-BERT N4903B and set up easily using the MIPI M-PHY frame generator SW.

Two example waveforms are presented in Figure 16 and Figure 17, which were created using an Agilent J-BERT and the BitifEye Frame generator SW. They show a small portion of a PWM gear 4 burst with ideal (2:1) and non-ideal (3:1) ratio of $TP_{WM\_MAJOR\_TX}$ to $T_{PWM\_MINOR\_TX}$ and several PWM gear 4 burst packages for which the frequency is swept 4x per burst over the entire range, i.e. from 24 to 72MHz.

4. The RX test

In order to actually perform the RX test, three steps have to be followed:

1. Connect the DUT-RX with the BERT, including all auxiliary signals
2. Set the DUT into an appropriate / well-suited / provided test mode
3. Count bit errors or check for error free performance

These steps will be described in the subsequent chapters.

4.1. DUT-RX clocking

In order to actually perform the RX test, the BERT PG has to be connected to the DUT according to Figure 18. Some DUTs may require that a reference- or system-clock is provided. Which exact frequency is required depends on the clocking architecture (of the DUT-RX).

If a forwarded (reference) clock is required, then the actual data rate and the reference clock provided by the BERT PG shall be synchronous emulating a system TX, which would have used its integer multiplying PLL to generate the actual output data rate. This would mean that when for test purposes extreme (± 2000 ppm, min or max) values of the data rate shall be generated, then the clock would be off from its nominal value too. This test case can be exactly emulated by the Agilent J-BERT N4903B, as it can supply a clock signal which is an integer divider of its main data output. Furthermore, the reference clock (of a TX in such a system or the BERT PG in a test environment) would also be off from its nominal value (about 1100 ppm), even when a nominal B-rate of any gear is generated (see Table 1).

If, however, an asynchronous architecture (e.g. a DUT RX with clock data recovery (CDR) was to be tested, then it could be desirable that a reference clock with nominal frequency be provided. In order to address this test case properly, an additional clock source (such as an Agilent 81150A or 33250A) should be used for generation of the reference clock.

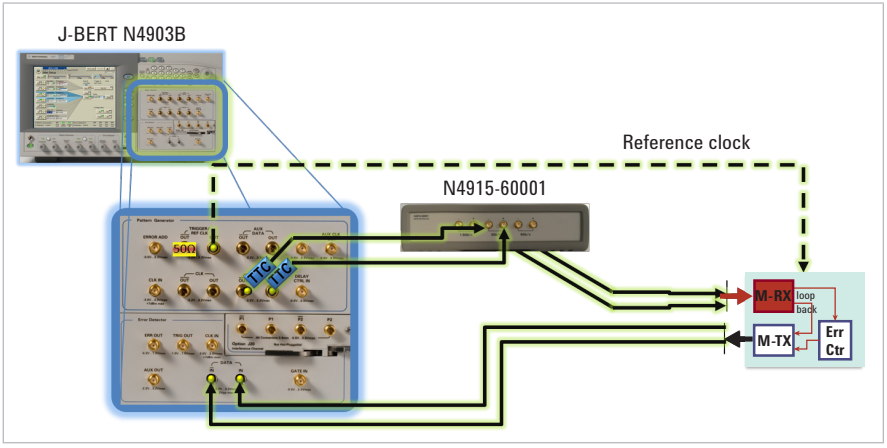


Figure 18. Actual test setup realized with Agilent J-BERT N4903B and N4915-60001 ISI Trace as conformance channel.

4.2. RX Test modes

In order to perform an RX test the RX has to be set to a suitable test mode, during which bit errors can be counted or at least correct detection can be monitored.

Loopback mode is one of the most common mechanisms used for this purpose. Its implementation, however, is not mandated by the M-PHY standard as already explained in paragraph 3.1 . However, if it is implemented, then it shall be a “near-end” or “synchronous” loopback where the recovered clock from the RX is used to retransmit the signal on the TX achieving a bit-by-bit relationship between RX and TX and where the exact bit sequence that was sent into the RX will appear at the TX (of course except for erroneously detected bits).

Dig_RF_v4, SSIC and M-PCIe specify this type of loopback for RX testing (limitations apply, see below)

Our experience with semiconductor vendors shows that it is obviously best practice to implement a (proprietary) means of enabling loopback as the test method of choice, even when the protocol standard doesn’t mandate it or when at first glance it seems impossible according to the descriptions above. For example, for testing the RX port of an application processor’s camera interface (which has high-speed RX’s but maybe no high-speed TX) the received data is routed through the TX of another port (e.g. for display); enabling this mode requires in-depth and DUT-specific knowledge and control capabilities over the ASIC, which is of course outside the scope of the M-PHY specification and this application note.

The LLI standard defines a test mode for a single lane utilizing a built-in TPV for an LLI-type CJpat. Once the device has entered this test mode, the results of the TPV are continuously transmitted via an associated TX and can then be decoded with suitable test equipment.

UniPro (and subsequently UFS, DSI-2 and CSI3) specifies to use a real frame (single or multi-lane) encapsulating a CJPat as a test pattern and read the protocol's Frame- and Frame Error Counter (PA_PACPFrameCount and PA_PACPErrorCount) to verify an RX's Phy-layer. The transmission of the counter results does not occur automatically (as for LLI) but has to be explicitly requested by sending appropriate commands to the RX. Decoding can be done in a similar way as for the LLI-case.

The different test methods are summarized in Table 3. Refer to the text box aside if none of these methods are implemented.

The IBerReader interface

Description of IBER reader interface as it is used by the N5990A measurement automation SW, which is defined in the Appendix of the current CTS [2]. It requires a custom implementation of the following functions:

- Connect (the string connection used by the N5990A measurement automation): will be called once at the beginning of the test run. The connection string can contain a customized address (like a COM port) to access to the tool, which is able to read out the internal counters of the DUT
- Init (string mode): will be called once at the beginning of each test. This allows you to configure the DUT into the test mode of a particular test (HS or PWM, Gear, Functional Test)
- ResetDUT (): will be called once at each test point. This allows you to reset error counters, or set the DUT in a defined mode to be ready for the next test point
- GetCounter (out double errorCounter, out double bitCounter) will be called after or during a test point execution. The errorCounter value can contain a CRC- or symbol-error, and the bitCounter can contain a bit or burst counter. The counters can only provide simple indicators; if errors happened and if the DUT was able to receive data, or, in case of both error- and bit- counters being implemented, to calculate BER

In any case, the test automation should make sure that the number of sent bits is sufficient to reach the confidence level for the target bit error rate, even if no error has occurred (see paragraph 4.3)

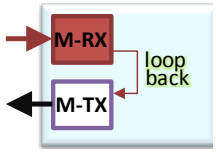
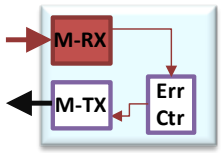
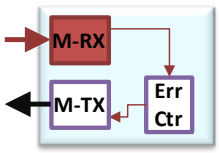
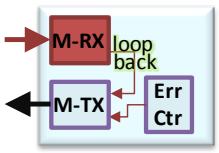
	DigRF 4	UniPro	LLI	SSIC, MEX
	Single and multi-lane test possible	Single and multi-lane test possible	Test one lane at a time; initiate test always on lane 0	Test on lane at a time
DUT block diagram				
Error detection method	Loopback using BERT ED for error counting: Challange: Bit shift due to resynch alternatives: • Dig_RF_v4 exerciser • Custom method, e.g. based on internal error counter (jBER)	Frame-counter and frame-error counter: Use either BERT error detector or oscilloscope to capture and decode counter readings	Internal error counter (T PV): Use either BERT error detector or oscilloscope to capture and decode counter readings	Loopback or optional internal error counter (IBER): • Loopback requires J-BERT B SER mode • The internal error counter can be read either with BERT error detector or with oscilloscope
Recommended instrument	J-BERT N4903B B (1 or 2 lanes), ParBERT (if >2 lanes)		J-BERT N4903B	

Table 3. Commonly used methods for error detection for M-PHY working under different protocols.

There are, however, a few conditions under which error checking as described above may not work.

1. Loopback, high speed burst mode

- BERT ED's may have to be clocked with BERT PG's clock, as ED's clock recovery (CR) may not be usable. It depends on the quality of the DUT's CR if the signal looped back is stable enough with respect to the PG's clock, as otherwise the BERT ED cannot sample the returned signal error-free.

- Due to burst mode signals being mandatory for DigRFv4, the BERT ED will expect the same exact bit sequence as it has sent out including the length of the DIF-N. However, due to resynchronization of the DUT RX at the beginning of every burst, the length of the pause between the bursts when looped back may vary by ± one bit. Consequently, the BERT ED will lose synch itself and needs to resynchronize, which may take longer than a burst. If the bit shifts by the DUT happen too frequently, the BERT ED might not be in synch long enough to measure a sufficient number of bits.

2. Loopback in low power mode: BERTs used for high speed applications can usually neither work in the low MHz data rate range nor do they feature PWM-mode, which means loopback cannot be used for error detection with the BERT's ED for any low power mode.

3. Method specified by protocol is not implemented: In these cases reading error counters or checksums through DUT specific SW interfaces is required. The CTS defines the so-called IBerReader interface, enabling linkage to suitable SW (such as the Agilent N5990A Measurement Automation SW, see paragraph 4.4) utilizing a customer provided DLL.

4.3. Verifying BER <10^{-10}

A question that arises is how long we have to measure for how many bits have to be observed and how many errors may occur along the way in order to verify the DUT's target BER of better than 10^{-10}.

Due to the statistical nature (binomial function), the actual BER cannot be determined exactly. What, however, can be determined with a certain confidence level (CL) depending on the parameters mentioned, is if the BER is above or below a certain threshold [3]; this relation is visualized in Figure 19, which shows that at least $3*10^{10}$ bits have to be tested without a single error occurring.

Note: the statistical methods mentioned above have been developed for real systems with impairments such as Gaussian distributed unbounded Random jitter. It is therefore important that test equipment emulates these conditions sufficiently. Agilent J-BERT N4903B fulfills this requirement, as its RJ is based on a diode generating a Gaussian distributed noise voltage with a CF>12 and is then converted linearly into "timing noise" or random jitter. Synthetically generated noise or RJ usually does not fulfill this requirement.

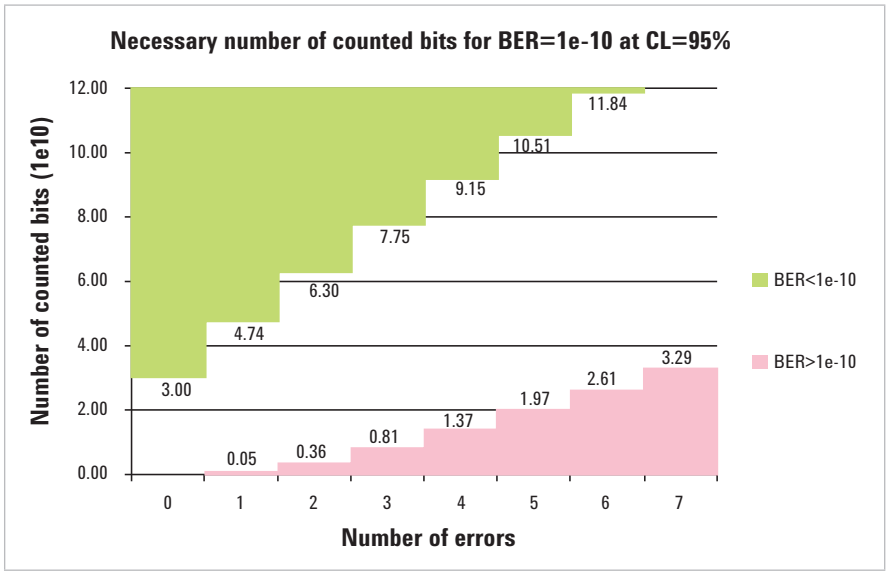


Figure 19. BER versus the number of errors and number of measured bits.

4.4. The Agilent N5990A-165 automation software for calibration and test

The complete calibration procedure (going further than the calibration of the jitter cocktail as discussed above in paragraph 3.5) can be performed automatically using the Agilent Automation SW N5990A opt 165. It not only automates calibration but also performs all tests according to the CTS 1.0, not only the high speed tests but also those for low power modes.

It works with the J-BERT N4903B as mentioned above plus Agilent's ParBERT 81250 (which is sometimes used, when MIPI- D-Phy test has to be performed on the same test station).

Furthermore, the BERT ED's can be used for error counting in HS_Loopback mode or to capture the results of the DUT's internal counters or it can connect to the DUT via a customer provided DLL using the iBER reader, so that fully automated for RX characterization can be achieved.

Summary of RX test

- Options for RX test modes such as loopback and internal error counting (TPV) have been described and the necessity of custom specific interaction has been explained
- Necessary measurement time to verify target BER of 10-10 has been explained
- Test automation SW N5990A opt 165 has been introduced

5. Summary: Testing MIPI M-PHY RXs with Agilent test solution

An introduction to the M-PHY specification has been given and the most important high speed RX test parameters have been explained. A practical and complete test setup using Agilent equipment adhering to the CTS has been shown. The calibration procedure for the M-RX jitter stress signal has been discussed. Using the Agilent J-BERT N4903B revealed this to be a very straight-forward task. The various possibilities and challenges of checking proper signal detection by the RX under test have been discussed.

The most important advantages of the Agilent offering for testing MIPI M-PHY RXs have been demonstrated:

- CTS-conformant test setup.
- Direct match between J-BERT N4903B capabilities and M-PHY jitter cocktail.
- Flexible Jitter generation to characterize part beyond specifications to determine margins.
- True RJ maintaining required frequency distribution and the QBER requirement supporting the minimum BER and beyond unambiguously.
- Simple calibration using automation SW N5990A opt 165.
- The calibration is independent from the test pattern: i.e. you can load a new pattern without impacting the calibration respectively keeping the same signal impairments.
- Ability to place custom data hassle-free into compliant M-PHY bursts using the BitifEye Frame Generator SW.
- Testing of PWM characteristics and transitions between low power and high speed mode.
- Choose and mix PWM and HS traffic in accordance to the M-PHY state machine.
- Change of signal parameters/impairments while the M-PHY link is active.
- CTS conformant characterization and test.
- Variety of error counting methods from BERT ED to IBER reader interface supported by N5990A test automation SW.
- Automated/unattended setup calibration and RX test execution.

6. Appendix

6.1. Test equipment

The required instruments and accessories for building the test setups are listed in Table 4.

Part number	Option	Source if not Agilent	Description	Qty	Comments
N4903B	C07 / C13 J10 002 J20		7G/13G J-BERT pattern generator and error detector	1	Option C13 for HS-gear 4, otherwise C07 Option 002 needed for 2 lane configuration (otherwise ParBERT required) J20 for common mode interference test
N4911A	002		Adapter 3.5mm(f) to 2.4mm(m)	10	Note: You may have to order less: Qty. 10 are supplied with J-BERT N4903B
1250-2206			50 ohm termination resistors	4	Note: May not be needed: 5 are supplied with J-BERT N4903B
15442A			Set of 4 SMA cables	3	Suited for HS-gears 1 and 2
N4915-60001			ISI channel (SATA ISI trace)	1	Use SATA-II channel of lower gears
DSA or DSO91204A			Digital signal analyzer or digital signal oscilloscope with 12GHz or higher bandwidth	1	
N5380B			13-GHz high-bandwitd differential SMA probe head	1	Substitutes 100 ohm differential termination
1134/68/69 A			InifiniiMax II probe amplifier	1	Selection depending on tested gear
N5990A	010 165 265 001 500		Core product MIPI M-Phy receiver compliance tests Interface to U7249A scope Tx compliance tests SQL database interface User programming	1	Test automation software Options 001, 265, and 500 optimal
BIT-1001-0002-0		BitifEye	120ps transition time conver	2 (4)	One lane configuration: 2, two lane configuration: 4
BIT-1006-0000-0		BitifEye	LAN hub (includes 5 LAN cables)	1	Optional
BIT-2060-0001-0		BitifEye	MIPI M-PHY frame generator S/W	1	Not required; necessary to generate custom pattern
BIT-2001-0000-0		BitifEye	1 yr S/W support extension	1	1st year included in N5990A-010

Table 4. Test equipment for M-PHY RX test according to set-up of Figure 10

6.2. Specifications for RX-stress signal

Symbol	Values		Unit	Description
	Min.	Max.		
HS-RX electrical				
$V_{DIF\_ACC\_RX}$	40		mV	Accumulated differential receiver input voltage for HS-G1. Defined for CJTPAT.
$V_{DIF\_ACC\_HS\_G2\_RX}$	40		mV	Accumulated differential receiver input voltage for HS-G2. Defined for CJTPAT.
$V_{DIF\_ACC\_G3\_RX}$	40		mV	Accumulated differential receiver input voltage for HS-G3. Defined for CJTPAT.
HS-RX timing				
T_{EYE_RX}	0.20		UI_{HS}	Receiver eye opening. Defined for CJTPAT over a statistical confident record set.
$T_{EYE\_HS\_G3\_RX}$	0.48		UI_{HS}	Receiver eye opening in HS_G3. Defined for CJTPAT[2] over statistical confident record set.
T_{PULSE_RX}	0.80		UI_{HS}	Receiver pulse width. Defined for CJTPAT.
HS-RX jitter				
DJ_{RX}		0.35	UI_{HS}	Receiver deterministic jitter over the frequency range from $f_{C\_HS\_RX}$ to f_{U_RX} which includes $STDJ_{RX}$. Defined for CJTPAT for a statistical confident record set.
$SJ_{RX(f)}$		0.15	UI_{HS}	Receiver sinusoidal jitter tolerance. Defined for CJTPAT and frequency range from $f_{C\_HS\_RX}$ to f_{SJ4_RX}.
		$\frac{0.15 \times f_{C\_HS\_RX}}{f}$	UI_{HS}	Receiver sinusoidal jitter tolerance. Defined for CJTPAT and frequency range from f_{SJ0_RX} to $f_{C\_HS\_RX}$.
$STDJ_{RX}$		0.20	UI_{HS}	Receiver deterministic jitter over the frequency range from f_{SJ4_RX} to f_{U_RX}. Defined for CJTPAT for a statistical confident record set.
TJ_{RX}		0.52	UI_{HS}	Receiver total jitter tolerance for galvanic interconnect without OMC. Defined for CJTPAT and a statistical confident record set.
$STTJ_{RX}$		0.60	UI_{HS}	Receiver total jitter tolerance for interconnect with OMC. Defined for CJTPAT and a statistical confident record set.
		0.30	UI_{HS}	Receiver total jitter over the frequency range from f_{SJ4_RX} to f_{U_RX}. Defined for CJTPAT and a statistical confident record set.

Symbol	Values		Unit	Description
	Min.	Max.		
Frequency				
$f_{C\_HS\_G1\_TX}$		2.0	MHz	Corner frequency of jitter transfer function in HS-G1.
$f_{C\_HS\_G2\_TX}$		4.0	MHz	Corner frequency of jitter transfer function in HS-G2.
$f_{C\_HS\_G3\_TX}$		8.0	MHz	Corner frequency of jitter transfer function in HS-G3.
f_{U_TX}		$\frac{1}{2UI_{HS}}$	Hz	Upper frequency of jitter transfer function.
f_{STJ_TX}		$\frac{1}{30UI_{HS}}$	Hz	Lower bound of short term jitter.
ζ		*0.707*	N.A.	Damping ratio of jitter transfer function.
Limit for BER				
Q_{BER}		6.36		Q-factor for a BER of 10^{-10}
BER			10^{-10}	Target BER

Table 5. PHY test specification for M-RX test

6.3. References

[1] MIPI M-PHY standard rev. 3.0 at http://mipi.org

[2] MIPI M-PHY CTS rev. 1.0 at http://mipi.org

[3] Agilent J-BERT N4903B High-Performance Serial BERT data sheet: 5990-3217EN

[4] Agilent N5990A Test automation software: 5989-5483EN

[5] Digital Communications Test and Measurement; Dennis Derickson-Marcus Mueller; Prentice Hall

Glossary

ASIC	Application-specific integrated circuit
BER	Bit error ratio
BERT	Bit error ratio tester
BERT PG	Bit error ratio tester pattern generator
BUJ	Bounded uncorrelated jitter
BW	Bandwidth
CDR	Clock data recovery
CF	Crest factor
CL	Confidence level
CR	Clock recovery
CTS	Conformance test suite
DDJ	Data dependent jitter
DJ	Deterministic jitter
DUT	Device under test
ED	Error detector
EH	Eye height
EQ	Equalizer
EW	Eye width
ESG	Electrical sub group
GUI	Graphical user interface
HF	High frequency
HS_RX	High speed receiver
HS_TX	High speed transmitter
ISI	Inter-symbol interference
LF	Low frequency

MIPI	Mobile Industry Processor Interface
M-PCIe	Mobile PCIe
M-PHY	MIPI physical layer interface (specification) with a base rate (Gear1) of approximately 1000MHz (1000=M)
MOI	Method of implementation
M_RX	M-PHY receiver
M_TX	M-PHY transmitter
NRZ	Non return to zero
OMC	Optical media converter
PG	Pattern generator
PHY	Physical layer or physical layer device
PLL	Phased-locked loop
PJ	Periodic jitter
PWM	Pulse width modulation
RJ	Random jitter
RX	Receiver
SJ	Sinusoidal jitter
STDJ	Short term deterministic jitter
STRJ	Short term random jitter
STSJ	Short term sinusoidal jitter
TJ	Total jitter
TPV	Test pattern verifier
TX	Transmitter
UI	Unit interval

PCI-SIG, PCI EXPRESS, and PCIe are US registered trademarks and/or service marks of PCI-SIG.

Figure 2, Figure 4, Figure 6, Figure 8, Figure 10, and Figure 11 are courtesy of MIPI alliance (from website, M-PHY standard or CTS).

More information:

http://mipi.org/
www.agilent.com/find/mipi
www.agilent.com/find/jbert
www.agilent.com/find/automation

myAgilent

www.agilent.com/find/myagilent
A personalized view into the information most relevant to you.

Agilent Channel Partners

www.agilent.com/find/channelpartners
Get the best of both worlds: Agilent's measurement expertise and product breadth, combined with channel partner convenience.

Agilent Advantage Services

www.agilent.com/find/AdvantageServices
Accurate measurements throughout the life of your instruments.

www.agilent.com
www.agilent.com/find/mipi-mphy
www.agilent.com/find/J-BERT

For more information on Agilent Technologies' products, applications or services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Americas

Canada	(877) 894 4414
Brazil	(11) 4197 3600
Mexico	01800 5064 800
United States	(800) 829 4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 112 929
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Other AP Countries	(65) 375 8100

Europe & Middle East

Belgium	32 (0) 2 404 93 40
Denmark	45 45 80 12 15
Finland	358 (0) 10 855 2100
France	0825 010 700* *0.125 €/minute
Germany	49 (0) 7031 464 6333
Ireland	1890 924 204
Israel	972-3-9288-504/544
Italy	39 02 92 60 8484
Netherlands	31 (0) 20 547 2111
Spain	34 (91) 631 3300
Sweden	0200-88 22 55
United Kingdom	44 (0) 118 927 6201

For other unlisted countries:
www.agilent.com/find/contactus
(BP2-19-13)

Product specifications and descriptions in this document subject to change without notice.

Published in USA, August 6, 2013
5991-2848EN

Agilent Technologies