HEWLETT PACKARD

Application Bulletin 56

INTERFACE TIMING AND DISPLAY LENGTH EXPANSION INFORMATION FOR THE HDSP-2000 CODED DATA CONTROLLER

The HDSP-2000 CODED DATA CONTROLLER shown in Application Note 1001 is a versatile circuit and is easily modified to multiplex any display length. This Application Bulletin contains the key timing information and a detailed explanation of how the circuit operates. With this information, it should be a straightforward exercise to expand the display to any desired length. Included in this Application Bulletin are designs for 32, 64, and 128 character displays. The ASCII to 5x7 decoder table within the Motorola MCM6674 ROM has also been shown. This decoder table can be stored within a Bipolar PROM if faster speeds are required.

The circuit shown in Figure 2 shows a CODED DATA CONTROLLER designed for a 32 character HDSP-2000 alphanumeric display. The key waveforms shown in Figure 1, labeled ① ② , and ③ , are shown to simplify the analysis of this circuit. Label ① is the 1 MHz clock. Label ② is the output of 7404 pin 2 which is the inverted Q_D output of the 74197. Label ③ is the output of the 7404 pin 6 which is the ANDed output of $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393. The Motorola 6810 RAM stores 32 bytes of ASCII data which is continuously read, decoded, and displayed. The ASCII data from the RAM is decoded by the Motorola 6674 128 character ASCII decoder. The 6674 decoder has five column outputs which are gated to the Data Input of the display via a 74151 multiplexer. Strobing of the display is accomplished via the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 6674. As shown by waveform ② , the 74197 also enables seven clock cycles to be gated to the clock input of the display. The 74393 is a divide by 256 counter connected so that the five lowest order outputs select each of the 32 ASCII characters within the RAM. The three highest order outputs determine the relationship between load time and column on time. When $2Q_B = 2Q_C = 2Q_D = 1$ of the 74393, waveform ③ goes to a logical 1. The circuit then scans 32 characters from the RAM and serializes the column data by counting through each of the seven rows of the 6674 and gating the appropriate column of the display. During the seven counts when $2Q_B$, $2Q_C$, and $2Q_D$ of the 74393 are not equal to a logical 1, the column data is displayed, as shown in waveform ④ . Since only one column can be on at a single moment, the highest possible column on time is 1/5 or 20%. Thus, the column on time of the display in Figure 2 is (20%) (7/8) or 17.5%.

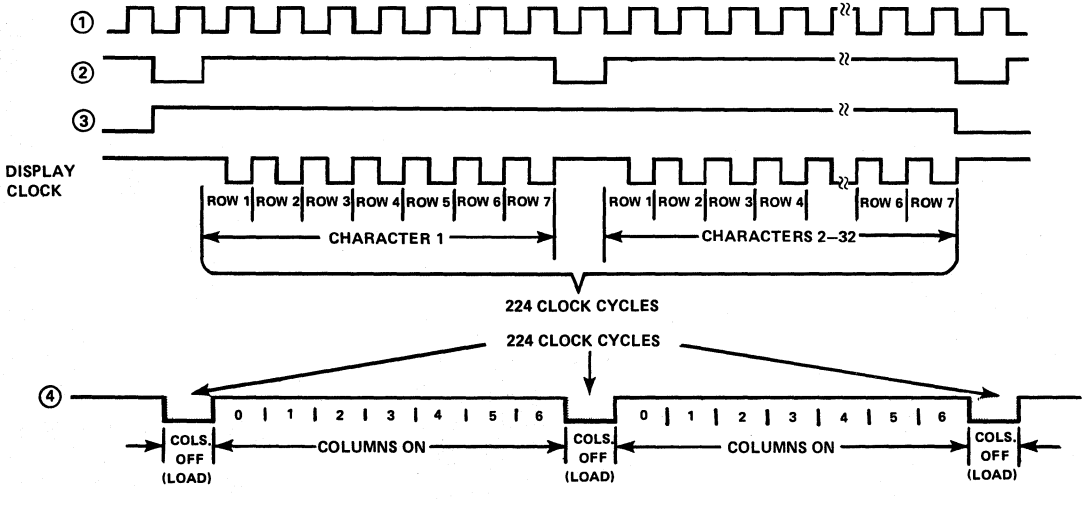

Figure 1. Timing Information for the 32 Character HDSP-2000 CODED DATA CONTROLLER

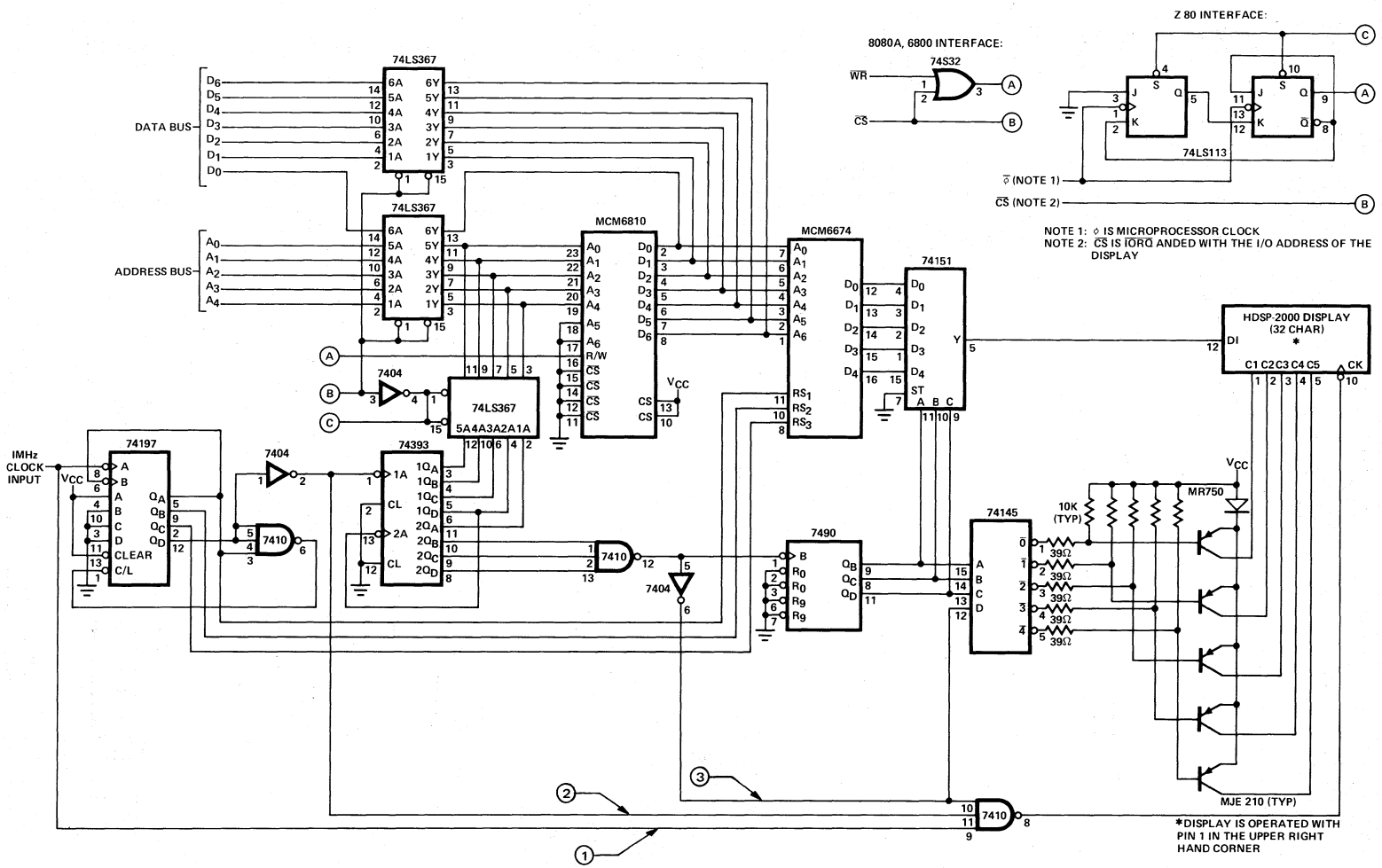

Figure 2. 6800, 8080A, and Z-80 Interface to the 32Character HDSP-2000 CODED DATA CONTROLLER

Changing the display length to 64 characters is a simple modification. This configuration can be easily realized by disconnecting $2Q_B$ of the 74393 from the 7410 and connecting it through the remaining tri-state buffer on the 74LS367 and using the 6810 RAM to store 64 ASCII characters. By leaving only $2Q_C$ and $2Q_D$ attached to the 7410, the column on time of the display is reduced from 17.5% to 15%. This reduction is caused because the relationship between actual column on time and theoretical column on time is 3/4 as opposed to 7/8 for the 32 characters. Since the display length has been doubled, the drive transistors must be upgraded to handle the higher column currents.

To implement a 128 character display, several modifications are needed. These changes are incorporated into the circuit in Figure 5. First, the input clock frequency has been increased to 2 MHz. This has been done to maintain a refresh rate of approximately 100 Hz for each digit, thus providing a flicker-free display. This higher speed of operation causes propagation delay problems within the MCM6674 (NMOS) whose maximum access time is 350ns. For this reason, the MCM6674 must be replaced by a faster Bipolar PROM. Refer to Figure 3 for a list of 1Kx8 PROMs that will function correctly in the circuit. From this list, the 82S2708 (maximum access time of 70ns) has been implemented. If this PROM is programmed with the code listed in Figure 4, it will decode a character font identical to the MCM6674. This same propagation delay problem is present with the MCM6810 RAM. Following worst case design procedures, the MCM68A10 1.5 MHz RAM should be used. To accommodate the additional address line made necessary by the display length expansion, the two 74LS367 tri-state buffers have been replaced with the 74LS244 octal version. Strobing of the display is accomplished using the 74197, 74393, and 7490 counter string. The 74197 is connected as a divide by 8 counter that sequentially selects the seven rows within the 82S2708. The 74393 is a divide by 256 counter connected so that the seven lowest outputs select each of the 128 ASCII characters within the RAM. The previously unused input A/output Q_A of the 7490 has been used as an additional divide by 2 counter. Thus, when the highest output of the 74393, $2Q_D$, and the Q_A output of the 7490 are NANDed through 7437, the basic relationship between load time and column on time is established. However, the external gating that has been added does affect the column on time slightly. Although these additional gates increase the total package count by one, they perform the necessary function of ensuring that the column drivers are turned off before the clock is gated to the display. This prevents noise from being generated on the clock of the display and eliminates erroneous display data. The resultant column on time is (23/32) (1/5) or 14.4%. The final modification made concerns the necessary column current needed to drive the display. Since the HDSP-2000 is rated at $I_{col(max)} = 410$ mA and there are 32 modules of four digits each, the transistors must source up to (32) (410 mA) or approximately 13A. Darlington PNP power transistors (2N6285) with the proper resistors have been used to accomplish this task.

Part Number	Manufacturer	Construction
7608	Harris	Bipolar — NiCr
3628-4	Intel	Bipolar — Si
82S2708	Signetics	Bipolar — NiCr
6381	Monolithic Memory	Bipolar — NiCr
6385	Monolithic Memory	Bipolar — NiCr
825228	National	Bipolar — TiW
93451	Fairchild	Bipolar — NiCr

Figure 3. 1Kx8 PROMs for Use in the HDSP-2000 CODED DATA CONTROLLER

PROM ADDRESS	HEXIDECIMAL DATA																
080	FF	FF	E4	E1	E8	FF	E0	EE	E4	E0	FF	E0	E4	E0	EE	EE	ROW 1
090	FF	EE	EE	EE	EE	E0	EE	E1	FF	E4	EE	EE	FF	FF	FF	FF	
0A0	E0	E4	EA	EA	E4	F8	E8	EC	E2	E8	E4	E0	E0	E0	E0	E0	
0B0	EE	E4	EE	EE	E2	FF	E6	FF	EE	EE	E0	EC	E2	E0	E8	EE	
0C0	EE	E4	FE	EE	FE	FF	FF	EF	F1	EE	E1	F1	F0	F1	F1	EE	
0D0	FE	EE	FE	EE	FF	F1	F1	F1	F1	FF	EE	E0	EE	E4	E0		
0E0	E6	E0	F0	E0	E1	E0	E2	ED	F0	E4	E1	F0	EC	E0	E0	E0	
0F0	F6	ED	E0	E0	E4	E0	E0	E0	E0	F1	E0	E2	E4	E8	E8	EA	
100	F1	F0	E4	E1	E4	F1	E1	F1	E8	E4	E0	E4	F5	E4	F1	F1	ROW 2
110	F1	F5	F1	F1	F5	E5	EA	E1	F1	E4	F1	F1	F5	F1	F1	F5	
120	E0	E4	EA	EA	EF	F9	F4	EC	E4	E4	F5	E4	E0	E0	E0	E1	
130	F1	EC	F1	F1	E6	F0	E8	E1	F1	F1	EC	EC	E4	E0	E4	F1	
140	F1	EA	E9	F1	E9	F0	F0	F0	F1	E4	E1	F2	F0	FB	F9	F1	
150	F1	F1	F1	F1	E4	F1	F1	F1	F1	F1	E1	E8	F0	E2	EA	E0	
160	E6	E0	F0	E0	E1	E0	E5	F3	F0	E0	E0	F0	E4	E0	E0	E0	
170	F9	F3	E0	E0	E4	E0	E0	E0	E0	F1	E0	E4	E4	E4	F5	F5	
180	F1	F0	E4	E1	E2	FB	E2	F1	FE	E2	E0	E4	EE	E8	FB	F1	ROW 3
190	F1	F5	F1	F1	F5	E2	EA	E1	EA	EE	F0	F1	F5	F1	F1	F5	
1A0	E0	E4	EA	FF	F4	E2	F4	E8	E8	E2	EE	E4	E0	E0	E0	E2	
1B0	F3	E4	E1	E1	EA	FE	F0	E2	F1	F1	EC	E0	E8	FF	E2	E1	
1C0	E1	F1	E9	F0	E9	F0	F0	F0	F1	E4	E1	F4	F0	F5	F5	F1	
1D0	F1	F1	F1	F0	E4	F1	F1	F1	EA	EA	E2	E8	E8	E2	F1	E0	
1E0	E4	EE	F6	EE	ED	EE	E4	F3	F6	EC	E1	F2	E4	FA	F6	EE	
1F0	F1	F1	F6	EF	FF	F1	F1	F1	F1	F1	FF	E4	E4	E4	E2	EA	
200	F1	F0	E4	E1	EF	F5	F4	FF	E9	FF	FF	F5	E4	FF	F5	F5	ROW 4
210	FF	F7	F7	FD	FD	F5	EA	FF	E4	EE	E8	FF	FD	FD	F7	F7	
220	E0	E4	E0	EA	EE	E4	E8	F0	E8	E2	FF	FF	EC	FF	E0	E4	
230	F5	E4	EE	E6	F2	E1	FE	E4	EE	EF	E0	EC	F0	E0	E1	E2	
240	ED	F1	EE	F0	E9	FC	FC	F3	FF	E4	E1	F8	F0	F5	F3	F1	
250	FE	F1	FE	EE	E4	F1	EA	F1	E4	E4	E4	E8	E4	E2	E0	E0	
260	E2	E1	F9	F1	F3	F1	EE	ED	F9	E4	E1	F4	E4	F5	F9	F1	
270	F9	F3	F9	F0	E4	F1	F1	F1	EA	EF	E2	E8	E0	E2	E0	F5	
280	F1	F0	E4	E1	E4	FB	F8	EA	E5	E2	E0	EE	F5	E8	FB	F1	ROW 5
290	F1	F1	F5	F5	F1	F8	EA	E1	EA	E4	E4	F1	F1	F5	F5	F1	
2A0	E0	E4	E0	FF	E5	E8	F5	E0	E8	E2	EE	E4	EC	E0	E0	E8	
2B0	F9	E4	F0	E1	FF	E1	F1	E8	F1	E1	EC	EC	E8	FF	E2	E4	
2C0	F5	FF	E9	F0	E9	F0	F0	F1	F1	E4	E1	F4	F0	F1	F1	F1	
2D0	F0	F5	F4	E1	E4	F1	EA	F5	EA	E4	E8	E8	E2	E2	E0	E0	
2E0	E0	EF	F1	F0	F1	FF	E4	E1	F1	E4	E1	F8	E4	F5	F1	F1	
2F0	F6	ED	F0	EE	E4	F1	F1	F5	E4	E1	E4	E4	E4	E4	E0	EA	
300	F1	F0	E4	E1	E2	F1	F0	EA	E1	E4	E0	E4	EE	E4	F1	F1	ROW 6
310	F1	F1	F5	F5	F1	F0	EA	E1	F1	E4	E0	F1	F1	F5	F5	F1	
320	E0	E0	E0	EA	FE	F3	F2	E0	E4	E4	F5	E4	E8	E0	EC	F0	
330	F1	E4	F0	F1	E2	F1	F1	F0	F1	E2	EC	E8	E4	E0	E4	E0	
340	F5	F1	E9	F1	E9	F0	F0	F1	F1	E4	F1	F2	F0	F1	F1	F1	
350	F0	F2	F2	F1	E4	F1	E4	FB	F1	E4	F0	E8	E1	E2	E0	E0	
360	E0	F1	F9	F1	F3	F0	E4	F1	F1	E4	F1	F4	E4	F5	F1	F1	
370	F0	E1	F0	E1	E5	F3	EA	F5	EA	F1	E8	E4	E4	E4	E0	F5	
380	FF	F0	FF	FF	E1	FF	E0	FB	E1	E0	FF	E0	E4	E0	EE	EE	ROW 7
390	FF	EE	EE	EE	EE	E0	FB	E1	FF	E4	E4	EE	FF	FF	FF	FF	
3A0	E0	E4	E0	EA	E4	E3	ED	E0	E2	E8	E4	E0	F0	E0	EC	E0	
3B0	EE	EE	FF	EE	E2	EE	EE	F0	EE	EC	E0	F0	E2	E0	E8	E4	
3C0	EE	F1	FE	EE	FE	FF	F0	EF	F1	EE	EE	F1	FF	F1	F1	EE	
3D0	F0	ED	F1	EE	E4	EE	E4	F1	F1	E4	FF	EE	E0	EE	E0	FF	
3E0	E0	EF	F6	EE	ED	EE	E4	EE	F1	EE	EE	F2	EE	F5	F1	EE	
3F0	F0	E1	F0	FE	E2	ED	E4	EA	F1	EE	FF	E2	E4	E8	E0	EA	

Figure 4. 82S2708 PROM Listing

APPLICATION NOTES

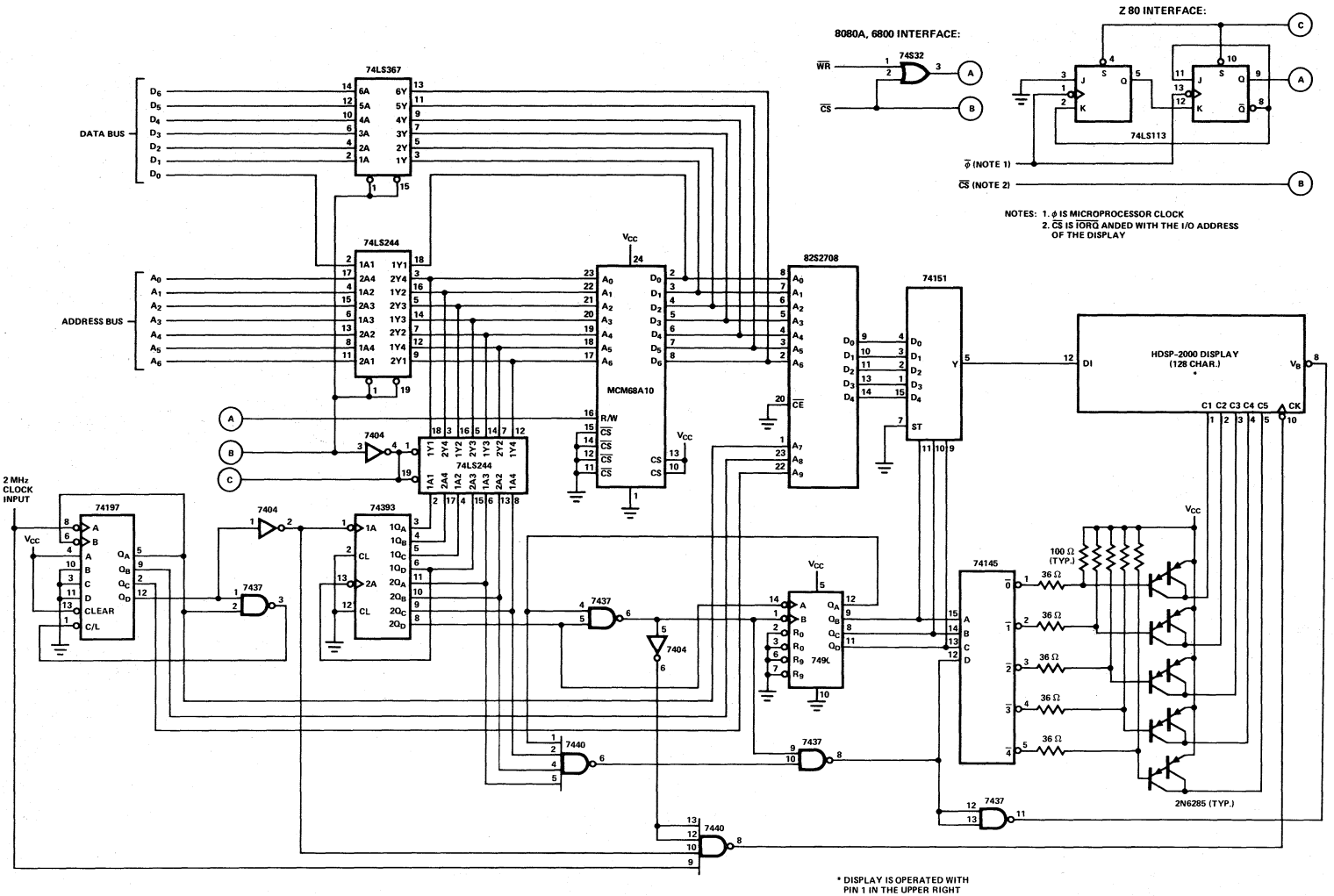

Figure 5. 6800, 8080A, and Z-80 Interface to the 128 Character HDSP-2000 CODED DATA CONTROLLER