Agilent Technologies
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Interfacing to PECL Optical Transceivers

Application Note 1173

Introduction

The original PECL is implemented by just taking the standard ECL components and applying +5 V and Ground instead of Ground and -5.2 V. Some of the practices used in ECL are carried over to the PECL. An example of this is in the PECL logic high and low specifications. Logic 1 is nominally -0.9 V and logic 0 is -1.7 V. Logic levels are specified as values "below V_{CC}" (0 V in ECL and + 5 V in PECL). When measuring these voltages with respect to the PECL Ground potential, the numbers translate to 4.1 V (V_{OH}) and 3.3 V (V_{OL}). Similarly, the PECL input requirement is often specified as values below +5 V as illustrated in Figure 1. Note that in this example the PECL input sensitivity is about 300 mV and that the average voltage developed as the result of such a repetitive waveform is about 3.7 V. The traditional ECL technology uses the upper supply rail as the reference for the I/O and internal switching bias levels. Any noise on this rail will couple directly onto these parameters. In the case of the ECL, the upper supply rail is Ground and it is relatively simple to keep it noise free. However, the upper supply rail for PECL logic voltages is V_{CC}, in other words, they change as V_{CC} changes. This is particularly important to note as often equipment is tested with low supply voltage during design verification. Designers must pay special attention to ensure that the PECL devices have clean power supply voltages that meet their minimum operating voltage requirements.

PECL optical transceivers have gained tremendous popularity. Circuit designers are faced with interfacing these PECL optical transceivers to various flavors of physical layer ICs (PHY). This application note will present the basic techniques used to interface

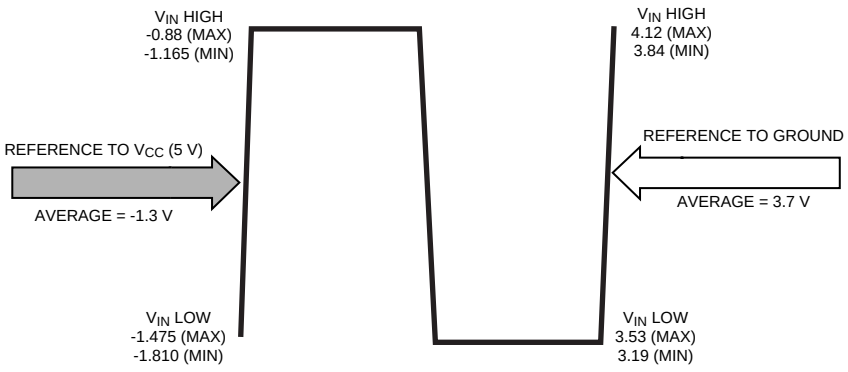

Figure 1. Example of PECL Input Voltage Specifications

to PECL and uses some of the PHY IC/optical transceiver interfaces to illustrate these techniques.

It may be easier and more intuitive for most of the logic designers to associate the PECL parameters with respect to Ground. This application note will explain the "below V_{CC}" value whenever necessary but will focus upon voltages referenced to Ground.

The Basics

Unlike most of the digital gates where each functional block can function independently without any external components, the PECL functional blocks are often not independent. For the inputs to work, the base of the input transistor needs to be biased.

Similarly, to complete the output circuit, it is necessary to provide a path for the emitter current. Figures 2a and 2b show the typical PECL Input and Output circuitry.

PECL and ECL are intended for high-speed (>50 MHz) applications typically with 50 Ohm input/output impedance. Transmission line with 50 Ohm characteristic impedance with proper termination is required. The termination should be matched to the 50 Ohm transmission line. However, 50 Ohms to Ground demands too much current from the output stage (V_O+ and V_O- in Figure 2b). So instead of terminating the 50 Ω load to Ground it is terminated to a voltage above Ground but low enough so that the output emitter follower would not be in cut off at V_{OL} (3.3 V in a 5 V system). This voltage, V_{TT}, is 3 V (2 V below V_{CC} of 5 V). See Figure 3a.

At V_{OL}, the load current:

$$I_O = \frac{3.3\ V - 3.0\ V}{50\ \Omega} = 6\ mA$$

To demand an extra 3 V supply in the modern digital system is not very practical. Instead, a two-resistor divider is used to generate the 3 V and the Thévenin-equivalent resistance of 50 Ω is matched to the transmission line. This resistance also provides the open-emitter output a current path as shown in Figure 3b.

Typical value for:
R1 = 82 Ω
R2 = 130 Ω

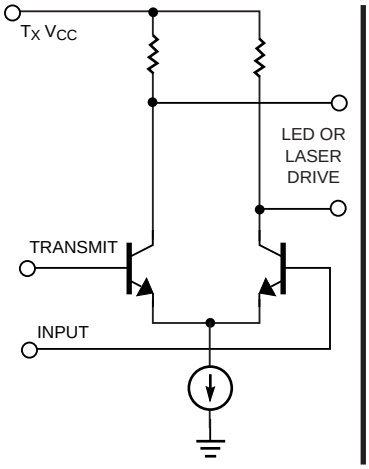

Figure 2a. Typical PECL Inputs

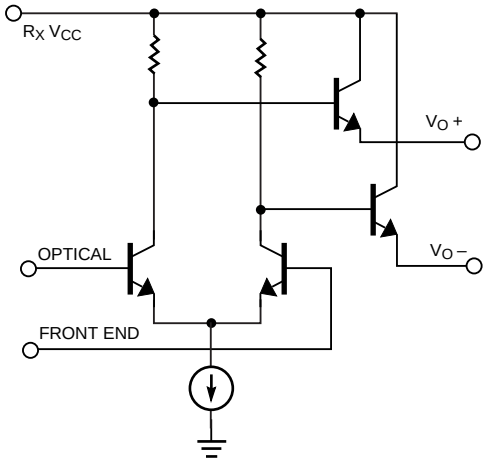

Figure 2b. Typical PECL Outputs

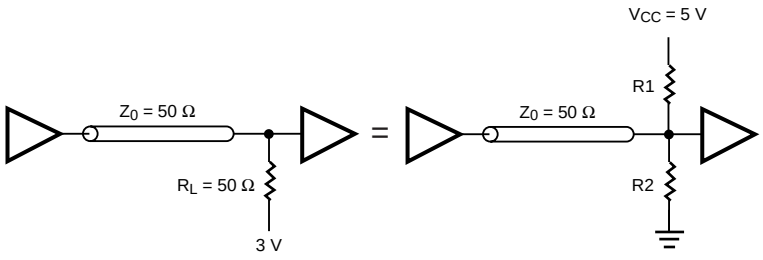

Figure 3a.

Figure 3b.

The transmission lines in this application note are all assumed to be with 50 Ω characteristic impedance (Z_0). The termination is best placed at the receiving end of the transmission line.

As seen in Figure 2a, standard PECL input needs biasing due to the open base circuitry. When you direct-couple the PECL output to the PECL input, the PECL output is supplying the bias. Most high-speed PECL signals are differential. You can treat both outputs as illustrated in Figure 4a. Here the 330 Ohm resistors provide the current paths to the outputs. For 50 Ohm differential transmission lines, $2Z_0$, the line-to-line termination equals 100 Ohms. The electrical length of the transmission lines should be kept matched. Mismatch will cause reflections. This termination technique is simple and works well if there are only differential signals. However, if there is common-mode signal, such as

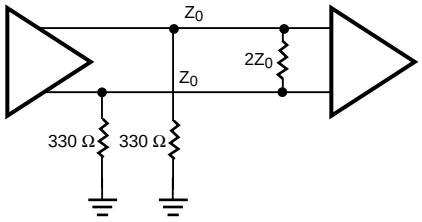

Figure 4a.

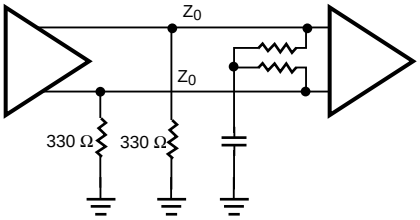

Figure 4b.

coupling from nearby circuits, Figure 4b rejects the common-mode interference by providing an ac Ground for the common-mode signal current. The 100 Ohm resistor is split into two 50 Ohm resistors and a bypass capacitor provides the ac ground.

Beyond the Basics

Optical links are most suited for high-speed serial data transmission. The optical transceiver usually connects to the Physical Layer (PHY) or serializer/deserializer (SerDes) IC. SerDes is also referred to as multiplexer/demultiplexer (Mux/Demux). Figure 5 shows the typical interface. Thanks to industry standards such as Fiber Channel, FDDI, ATM, Fast Ethernet and Gigabit Ethernet, this interface is universally PECL. However, there are different implementations and subtle variations. In general this interface can be in one of two forms: dc coupled or ac coupled.

a) DC Coupled.

This interface is straightforward. The concept in Figure 4 applies. A good example of this configuration is the interconnections

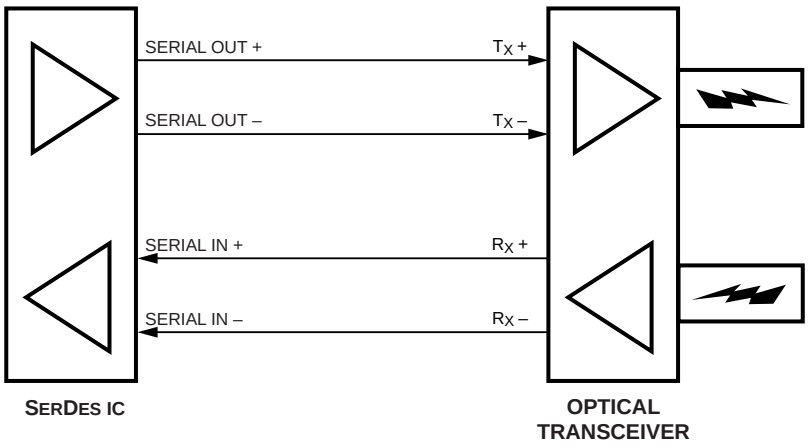

Figure 5. Typical SerDes to Transceiver Interface

between the HFBR/HFCT-5208 and the AMCC's S3028B as shown in Figure 6. The S3028B is a SONET OC-12 Mux/Demux. This diagram only shows the differential transmit and receive signals. For all other signal connections, refer to the HFBR/HFCT-5208 and S3028B data sheets and application note.

b) AC Coupled.
The inputs or outputs for the PHY or the SerDes are not always standard PECL although they may retain the PECL signal amplitude specification (p-p signal level). These inputs/outputs deviate from the standard PECL structure, i.e., the inputs can be internally biased or terminated; or the outputs are not open emitter but rather open Drain as in CMOS.

A good example is Agilent Technologies' Gigabit Ethernet SerDes HDMP-1646A. The high speed Serial In ± are internally biased. When interfacing to these SerDes inputs from the optical transceiver high-speed serial outputs (RX ±), in order to preserve the internal bias on the HDMP-1646A you must ac-couple the optical transceiver RX ± and the SerDes Serial In ±. A different approach is needed to complete the circuit for the RX ±. A simple pull down resistor is all that is needed to provide a path for the output emitter current. Instead of a 50 Ohms to 3 V, you can use a 270-510 Ohms to Ground. You can properly terminate the transmission lines carrying the high-speed differential output signals from the optical transceiver to the SerDes by placing the impedance matching resistor at the Serial In ± terminals. See Figure 7.

The Serial Out ± of the HDMP-1646A SerDes are also not standard PECL. They are not open emitters and these outputs require ac coupling to the following stage. The HDMP-1646A data sheet recommends a 150 Ohms pulldown resistor at each of the outputs.

The Tx ± common mode is centered around 3.7 V and therefore the 68/191 Ohms combination is chosen to bias the Tx ± inputs to be at the middle of the common mode range. This will give the Tx input the maximum sensitivity (equal swing above and below 3.7 V).

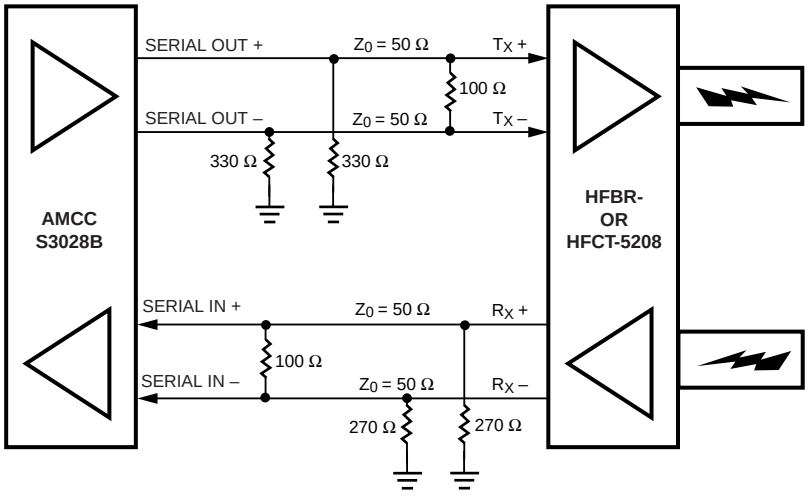

Figure 6. AMCC S3028B SerDes to HFBR/HFCT-5208 OC-12 Optical Transceiver

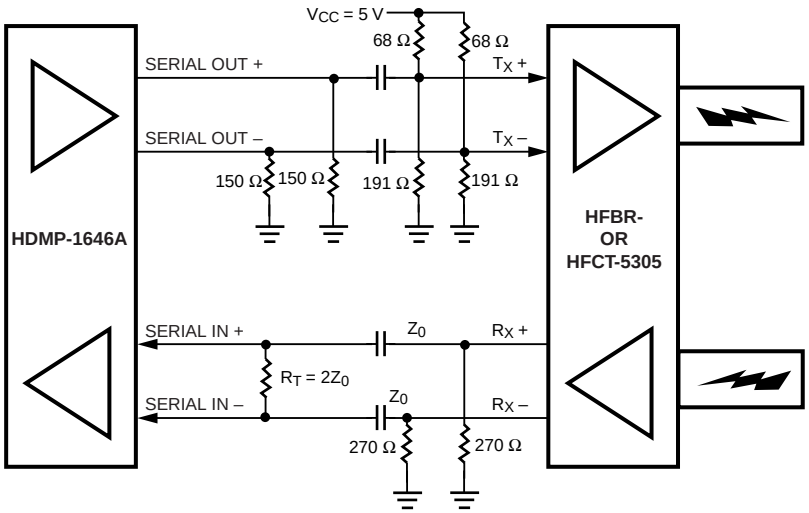

Figure 7. Typical HDMP-1646A to HFBR/HFCT-5305 Interface

3.3 V PECL Transceivers

The HFBR/HFCT-59XX series of Small Form Factor optical transceivers with the MT-RJ optical connector are specified to operate with 3.3 V supply voltage. These are basically PECL devices that operate at 3.3 V supply voltage. The differential input voltage requirement (minimum p-p level) and the output p-p voltage swing continue to be the same as the 5 V counterpart. The HFBR-59XX series enables 2x the port density when compared to the duplex SC transceiver. Thanks to their reduced width and power consumption, a single-board, 24-port configuration can be achieved.

The dc- and ac-coupling topology is exactly the same as previously discussed. However, with supply voltage reduced to 3.3 V, V_{TT}, which in the 5 V case equals to 3 V (2 V below V_{CC}, 5 V - 2 V = 3 V) is now 1.3 V (3.3 V - 2 V = 1. 3 V). Similarly, the ac-signal swing used to center around 3.7 V (1.3 V below V_{CC}) is now centered around 2 V (3.3 V - 1.3 V = 2 V). Leveraging from the smaller footprint of these new transceivers, they are typically used with dual or quad PHY ICs.

AC coupling the HFBR/HFCT-59XX

To implement an ATM User-Network Interface (UNI), the connections between the PMC-Sierra's PM5348 and the HFBR/HFCT-5905 require special considerations. See Figure 8. The PM5348 (S/UNI Dual) is a 5 V CMOS part with TTL TXD ±. This interface not only requires ac-coupling but the TTL TXD ± (output) signals also need conversion to the PECL input level for the HFBR/HFCT-5905. The TXD ± output impedance, the 237 Ω resistor and the termination form a network for the proper attenuation. For detailed operation and specifications for the PM5348 please refer to its data sheet and application note.

The RXD ± inputs on the PM5348 are internally self-biased and therefore require ac-coupling. Note that the 100 Ohms line-to-line termination should be placed close to PM5348's RXD ± inputs.

Interfacing the HFBR/HFCT-59XX to PHY ICs with +5 V supply typically requires ac-coupling. As long as the input/output signal levels are compatible, ac-coupling will take care of any dc conflicts.

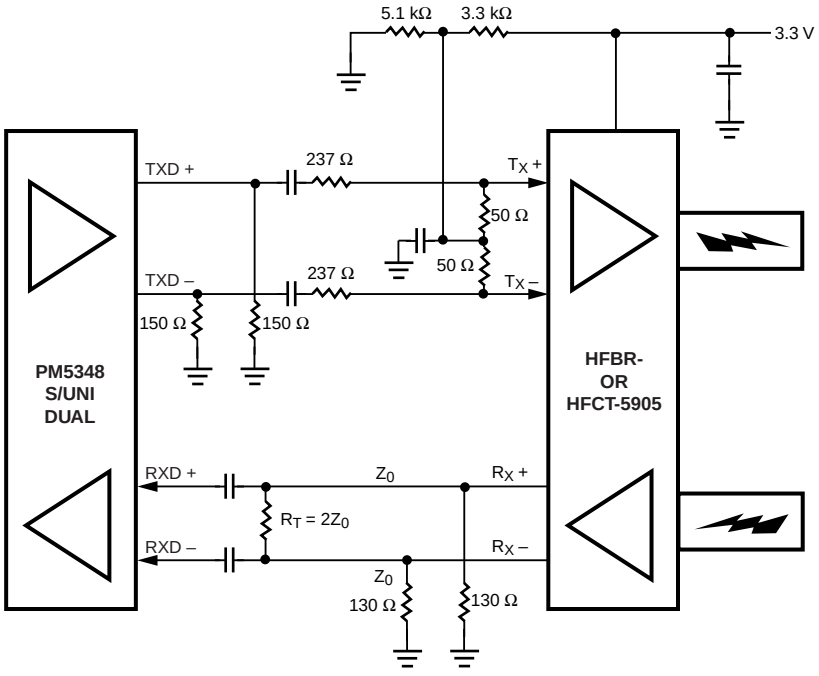

Figure 8. Interface Between the PM5348 and the HFBR/HFCT-5905

Figure 9 illustrates yet another subtle variation. Here the HFBR/HFCT-5903 is interfaced to the Level One LXT 974, a 5 V Quad PHY. AC-couplings are used for both the transmit- and the receive-paths. For a typical 24-port implementation, you can further reduce your system's power consumption by separating the transmission line termination and the input bias network. In Figure 9, the TX ± inputs are terminated with two 50 Ω resistors. The 2 V dc bias is developed via the 3.3 kΩ / 5.1 kΩ network, which can be used to bias multiple ports (i.e., multiple of four). The TXD ± outputs of the LXT 974 require no external pulldown resistors.

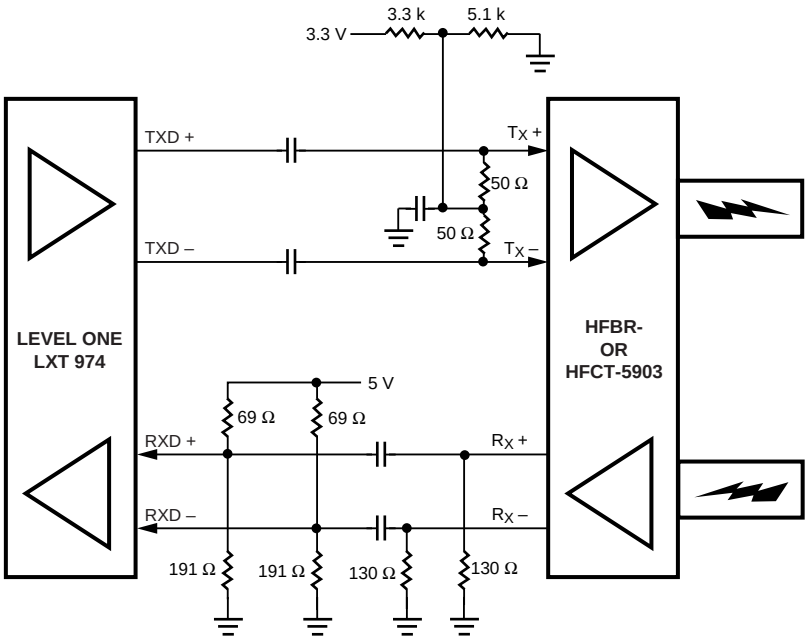

Figure 9. Interface Between the LXT 974 and the HFBR/HFCT-5903

Figure 10 illustrates how to interface the HFBR/HFCT-5903's input/output to SEEQ's 84220 10/100BASE PHY. 84220's FXOP/N differential outputs alternately sink 15 mA as FX data. The external resistors (69 Ohms) provide the current paths to these nodes. In addition, as 15 mA is alternately drawn through these resistors, the voltage drops developed across them translate this current to the PECL levels recognized by the HFBR/HFCT-5903. Lastly, 69/174 Ohm networks form the 50 Ohm terminations for the transmission lines.

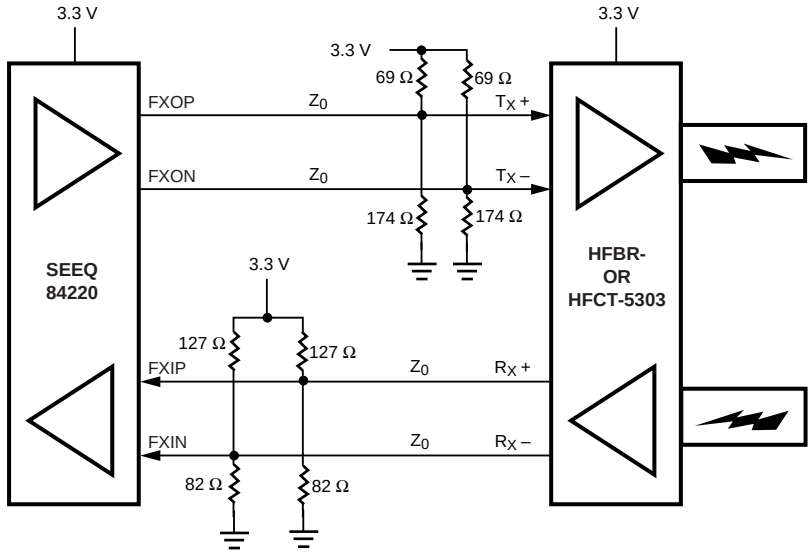

Figure 10. Typical SEEQ 84220 to HFBR/HFCT-5303 Interface

Note that the FXOP/FXON outputs are not the standard PECL structure (not open emitters) although through external circuits they are capable of supplying the PECL signal level (± 800 mV) needed to drive standard PECL inputs.

Assume FXOP is on (sinking 15 mA) and FXON is off,

The voltage at the Tx - terminal of the 5903 :

$$3.3\ \text{V}\ \frac{174\ \Omega}{69\ \Omega + 174\ \Omega} = 2.4\ \text{V}\ \ \text{(PECL logic high)}$$

The current through the 69 Ω resistor is:

$$\frac{3.3\ \text{V} - 2.4\ \text{V}}{69\ \Omega} = 14\ \text{mA}$$

When FXON turns on, an additional 15 mA will be drawn through the 69 Ω. The voltage at the Tx– terminal of the 5903 becomes:

$$3.3\ V - (14\ mA + 15\ mA) \bullet 69\ \Omega = 1.3\ V \quad \text{(PECL logic Low)}$$

Interfacing to 84220's FXIP/N inputs is straightforward. The HFBR/HFCT-5903's RXD ± outputs are dc coupled to 84220's FXIP/N inputs. The 127/82 Ohm resistor-networks bias the inputs and terminate the transmission lines.

Interfacing Signal Detect

Signal Detect is a single-ended output commonly available with optical transceivers. It gives an indication if there is light received at the optical receiver. Typically Signal Detect is a light/no light indicator (with Logic 1 or 0). It is not an optical power meter. The Signal Detect output is at a fixed logic state during normal receiver operation. It toggles to the opposite state when the receiver detects light below a specified level. The Signal Detect output is not repetitive and therefore you cannot ac couple this signal. You also do not need to use 50 Ohm transmission line for Signal Detect. DC coupling the PECL Signal Detect signal between a 5 V (or 3.3 V) optical transceiver and a 5 V (or 3.3 V) PHY is straightforward. However, when feeding the 3.3 V PECL Signal Detect to a 5 V PHY, you may need to level shift the 3.3 V PECL Signal Detect (Typical Logic 1 ≅ 2.4 V, Logic 0 ≅ 1.6 V). Figure 11 illustrates a level-shifting circuit.

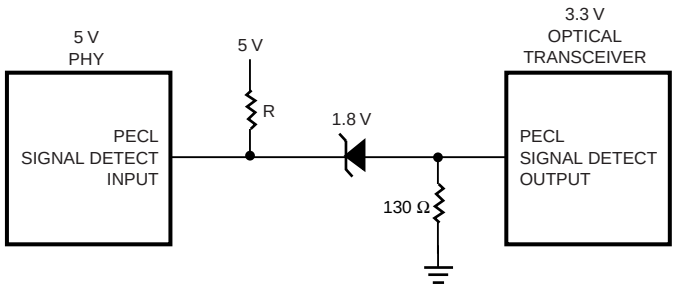

Figure 11.

The Zener diode should be biased with about 10 mA of current. To calculate for the value of R:

$$R = \frac{5\ V - 1.8\ V - 2.4\ V\ (\text{signal detect high})}{10\ mA} = 80\ \Omega$$

This level shifting circuit is simple but not without tradeoffs. PECL devices, as stated earlier, are very often ECL devices (upper rail is ground, V_{EE} is -5.2 V) operating with positive supply voltages (upper rail V_{CC} is positive supply and lower rail is ground). The internal circuit of these devices is designed to reference to the upper rail (ground in ECL). Supply voltage variations will affect dc levels of these devices. In order to accommodate V_{CC}, output and input ranges, a more robust Signal Detect interface circuit may be required. Figure 12 illustrates this idea.

Some of the PHY ICs provide differential inputs for the Signal Detect. As the Signal Detect output from the transceiver is fed to one of the inputs, a reference voltage should be supplied to the complementary input. The reference voltage is compared against the Signal Detect logic level so the PHY can determine its logic state. The reference voltage, therefore, should be set to:

Vref = 1/2 (Signal Detect Input High + Signal Detect Input Low)

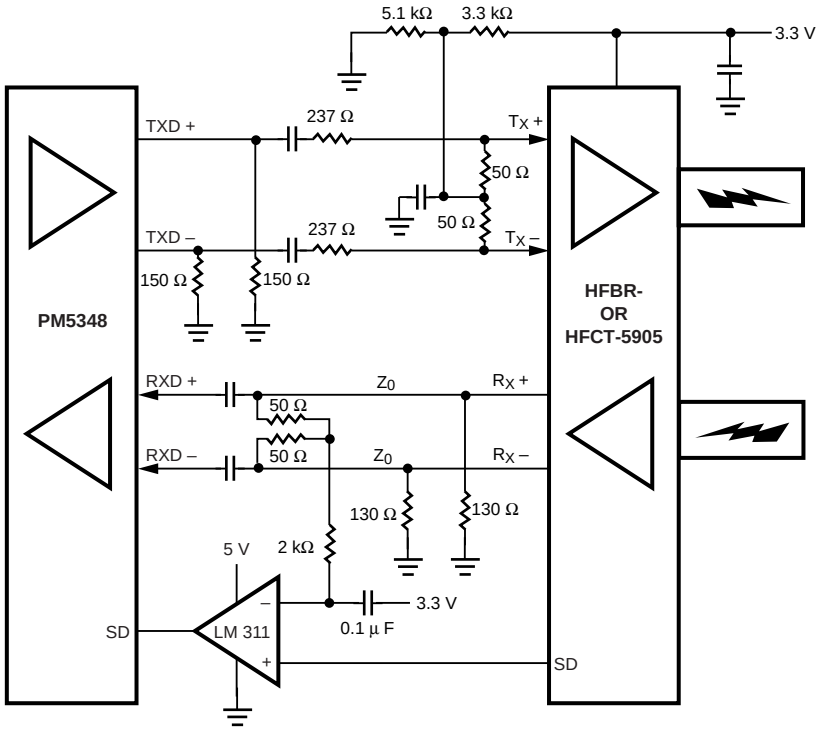

Figure 12. Interface between the PM5348 and the HFBR/HFCT-5905

For 5 V PECL optical transceiver, the Signal Detect output typically is from 3.3 V (PECL logic Low) to 4.1 V (PECL logic High),

Vref = 3.7 V

For 3.3 V PECL optical transceiver, the Signal Detect output typically is from 1.6 V (PECL logic Low) to 2.4 V (PECL logic High),

Vref = 2.0 V

Summary

There are many variations to the input/output structures of physical layer ICs. When interfacing a specific IC to either the 5 V or the 3.3 V PECL optical transceivers, observe the supply voltage differences and the input/output topologies used for the IC.

Consider the following when interfacing to PECL optical transceivers:

- DC-couple "standard" PECL output to "standard" PECL input with equal V_{CC}.
- Consider using ac coupling if the interfaced output and input belong to devices using different supply voltages.
- When ac coupling standard PECL output to standard PECL input:
  – Provide proper bias to the standard PECL input unless it is self-biased
    - The switching threshold for standard 5 V PECL is 3.7 V (1.3 V below V_{CC})
    - The switching threshold for standard 3.3 V PECL is 2 V (1.3 V below V_{CC})

  – Complete the current path for the standard PECL output
- If either the output or the input is not standard PECL, use ac coupling unless the ac coupling is built-in, typically at the input
- Provide proper transmission line termination

Data subject to change.
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