Agilent Technologies
Innovating the HP Way

High Intercept Low Noise Amplifiers for 1500 MHz through 2500 MHz using the ATF-34143 Low Noise PHEMT

Application Note 1175

Introduction

Agilent Technologies' ATF-34143 is a low noise PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. The ATF-34143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The 800 micron gate width of the ATF-34143 makes it ideal for applications in the VHF and lower GHz frequency range by providing low noise figure coincident with high intercept point. The wide gate width also provides lower impedances that are easy to match.

The ATF-34143 is described in two low noise amplifiers for use in PCS applications. With minor component changes, the same amplifier design can be optimized for GPS and ISM applications. The circuits are designed for use with 0.032 inch thickness FR-4 printed circuit board material. The amplifiers make use of low cost miniature wirewound and multilayer chip inductors for small size. When biased at a V_{ds} of 2 volts and an I_{ds} of 20 mA, the ATF-34143 amplifier will provide 15 to 16 dB gain, 0.6 dB noise figure and an output intercept point (IP3) of +25 dBm. At an elevated bias of V_{ds} = 4 V and I_{ds} = 60 mA, the LNA will achieve an OIP3 of +31 dBm with a corresponding IIP3 of +15 dBm. The IP3 performance coincident with low noise makes the ATF-34143 an ideal device for a high dynamic range low noise amplifier. Both self biased and dual power supply techniques are discussed.

Biasing Options and Source Grounding

Passive biasing schemes are generally preferred for their simplicity. One method of passive biasing requires the source leads be direct dc grounded. A negative voltage is applied to the gate through a bias de-coupling network. The gate voltage is then adjusted for the desired value of drain current. The gate voltage required to support a desired drain current, I_d, is dependent on the device's pinchoff voltage, V_p, and the saturated drain current, I_{dss}. I_d is calculated with the following equation.

$$V_{gs} = V_p \left(1 - \sqrt{I_d / I_{dss}} \right)$$

As an example, for the ATF-34143 for a I_d of 20 mA, I_{dss} of 118 mA and a V_p of -0.5 volts, the required V_{gs} is -0.294 volts.

Another option for passive biasing is to raise the source above ground with a resistor and dc ground the gate. This configuration forces the gate negative with respect to the source, thereby allowing the drain current to be set with the source resistor. The source resistor, R_s, is equal to $-V_{gs}/I_d$ = 14.7 Ω. The source resistor is then ac bypassed with a capacitor with a low impedance at the desired operating frequency. Both the dc grounded and bypassed source resistor technique of ac grounding the source have some inductance associated with the connection. Each bypass capacitor can have up to 0.7 to 1 nH of associated lead inductance which can be used to an advantage in the RF design. Even the dc grounded source leads have some finite length associated with the trace which correlates to some equivalent inductance.

The use of a controlled amount of source inductance can often be used to enhance LNA performance. Usually only a few tenths of a nanohenry or at most a few nanohenrys of inductance is required. This is effectively equivalent to increasing the source leads by only 0.050 inch or so. The effect can be easily mod-

eled using one of the Agilent/ EESOF microwave circuit simulators. The amount of source inductance that can be safely added depends on the device. Very short gate width devices such as the 200 micron gate width ATF-36163 can tolerate very little source inductance. Usually the inductance associated with just two plated through holes through 0.031 inch thickness printed circuit board is all that the device can tolerate. Hence the smaller gate width devices such as the ATF-36163 are typically used as low noise amplifiers for C and Ku Band applications such as TVRO and DBS.

The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate width devices have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be. The ability of the 800 micron gate width ATF-34143 to tolerate greater source inductance allows the designer to take advantage of self biasing thereby only necessitating a single positive power supply.

LNA Design

The amplifiers were designed for optimum performance in the 1.9 to 2 GHz frequency range. The generic demo board shown in Figure 1 is used for both designs. The board gives the designer several design options for both the rf circuitry and biasing options.

The demo board was designed such that the input and output impedance matching networks can be either lumped element networks or etched microstrip networks for lower cost. Either low pass or high pass structures can be generated based on system requirements. The demo board also allows the FET to be either self biased or with grounded sources the FET can be biased with a negative voltage applied to the gate terminal. The demo board is etched on 0.031" thickness FR-4 material for cost considerations.

Design of ATF-34143 Amplifier # 1

The schematic diagram describing the dc grounded source amplifier is shown in Figure 2. The parts list for the first amplifier is shown in Table 1. The demo board as modified is shown in Figure 3. The modifications are discussed in the next section.

Table 1. Component Parts List for the ATF-34143 Amplifier #1.

Number	Description
C1	8.2 pF chip capacitor
C2,C5	8.2 pF chip capacitor
C3,C6	10000 pF chip capacitor
C4	6.8 pF chip capacitor
L1	2.7 nH inductor (Toko LL1608-F2N7S)
L2, L3	Strap each source pad to the ground pad with 0.040" wide etch. The jumpered etch is placed a distance of 0.070" away from the point where each source lead contacts the source pad. Cut off unused source pad. See text.
L4	3.3 nH inductor (Coilcraft 0805CS-030XMBC)
Q1	Agilent Technologies ATF-34143 PHEMT
R1	50 Ω chip resistor
R2	12 Ω chip resistor
Zo	50 Ω Microstripline

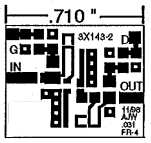

Figure 1. 1X Artwork for the ATF-34143 Low Noise Amplifier.

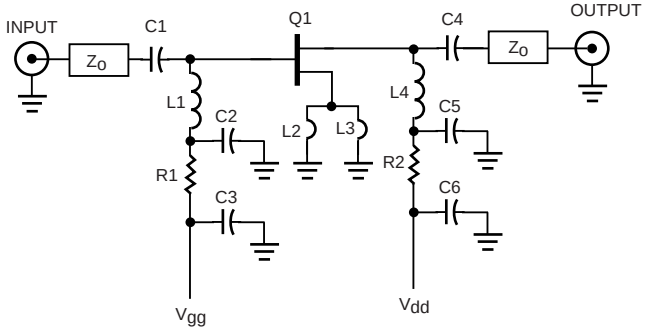

Figure 2. Schematic Diagram of the dc grounded source ATF-34143 Amplifier.

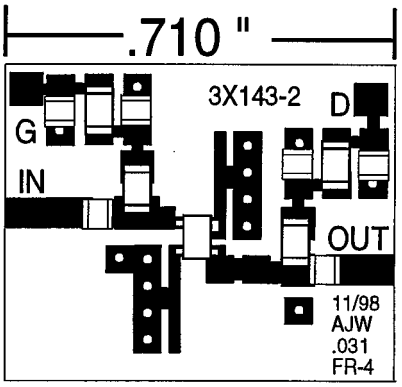

Figure 3. Component Placement Drawing for the ATF-34143 Low Noise Amplifier #1.

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor (C1) and a shunt inductor (L1). The high-pass topology is especially well suited for PCS and WLAN applications as it offers good low frequency gain reduction which can minimize the amplifier's susceptibility to cellular and pager transmitter overload. L1 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. C1 also doubles as a dc block. The Q of L1 is extremely important from the standpoint of circuit loss which will directly relate to noise figure. The Toko LL1608-F2N7S is a small multilayer chip inductor with a rated Q of 32 at 800 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. This network has been optimized primarily for noise figure with secondary emphasis on input return loss. Resistor R1 and capacitor C3 provide low frequency stability by providing a resistive termination.

The amplifier uses a similar high-pass structure for the output impedance matching network. L4 and C4 provide the proper match for best output return loss and maximum gain. L4 also doubles as a means of inserting voltage to the drain. Resistor R2 and capacitor C6 provide a low frequency resistive termination for the device which helps stability. C6 was chosen to be 10000 pF or 0.01 µF over a 1000 pF capacitor in order to improve output intercept point slightly by terminating the F2-F1 difference component of the two test signals used to measure IP3. This can be especially important for the typical 1.25 MHz spacing used in CDMA IP3 evaluation.

The original demo board incorporates additional series microstriplines in both the input and output impedance matching networks. They are not required for this amplifier design and can be removed from the demo board. They should be replaced with a small 0.040" wide piece of etch. There is also space allocated for a resistor in series with the drain of the device. This resistor is also not required for this amplifier design and the gap should be bridged with a small piece of etch. The lower gain of the wider gate width 800 micron ATF-34143 as compared to the 400 micron ATF-35143 minimizes the need for resistive loading in the drain circuit. The slightly lower gain of the 800 micron device is offset by a potential improvement in stability and output power.

Inductors L2 and L3 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstripline which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad is connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For amplifier #1, each source lead is connected to its corresponding ground pad at a distance of approximately 0.070" from the source lead. The 0.070" is measured from the edge of the source lead to the closest edge of the ground strap. The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. More on this subject next.

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far?

For an amplifier operating in the 2 GHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in

the 6 to 10 GHz frequency range. Normally the high frequency gain rolloff will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is OK as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device. A wide-band plot of S21 for an amplifier using the 400 micron ATF-35143 amplifier is shown in Figure 4. The ATF-35143 is used in this example because it is more sensitive to source inductance, i.e. high frequency gain is greater with smaller gate widths. Similar behavior is to be expected using the 800 micron ATF-34143 but to a lesser degree. The plot shown in Figure 4 represents an amplifier that uses minimal source inductance and has a relatively smooth gain roll-off at the higher frequencies.

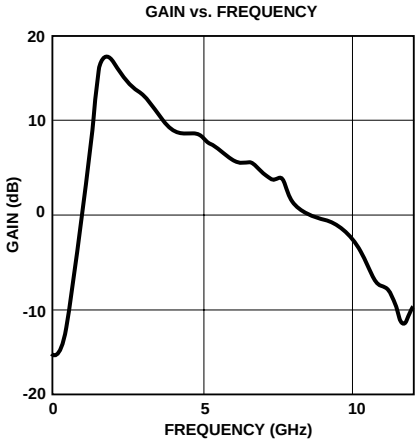

Figure 4. Wide-band gain plot of ATF-35143 amplifier using minimal source inductance.

The wideband gain plot shown in Figure 5 is for the same amplifier that uses additional source inductance to improve low frequency stability and input return loss. Its effect can be seen as some gain peaking in the 6 GHz frequency range. This level of gain peaking is not considered a problem because of its relatively low level compared to the in-band gain.

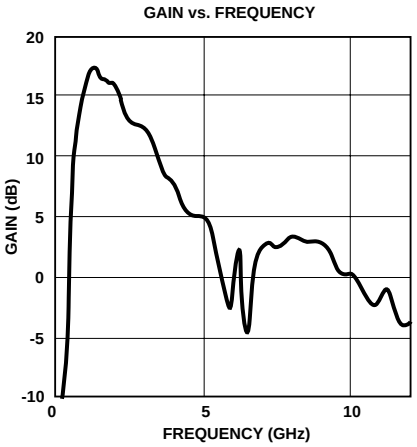

Figure 5. Wide-band gain plot of ATF-35143 Amplifier with an acceptable amount of source inductance.

Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak at about 6 GHz which could approach 20 to 30 dB. Its effect can be seen in Figure 6. The end result is poor amplifier stability especially when the amplifier is placed in a housing with walls and a cover. Larger gate width devices such as the 800 micron ATF-34143 will be less sensitive to source inductance than the smaller gate width devices. The wide-band gain plot does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance.

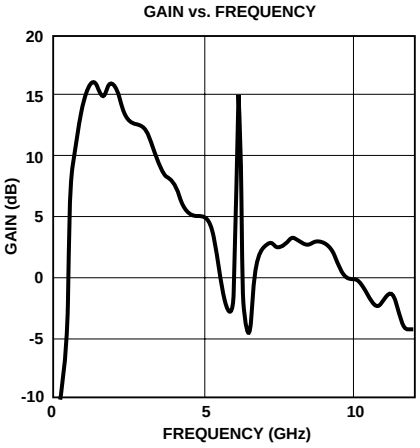

Figure 6. Wide-band gain plot of ATF-35143 amplifier with an unacceptable amount of source inductance producing undesirable gain peaking.

Performance of ATF-34143 Amplifier #1

The amplifier is tested at two bias points, V_{ds} = 2 V @ I_d = 20 mA and V_{ds} = 4 V @ I_d = 60 mA. The measured noise figure and gain of the completed amplifier is shown in Figures 7 and 8. Noise figure is a nominal 0.5 to 0.65 dB from 1850 through 2500 MHz at the lower bias point. One of the advantages of the ATF-34143 is its ability to deliver a very low noise figure at elevated bias points. At a V_{ds} = 4 V @ I_d = 60 mA, the noise figure is still only 0.7 dB at 2 GHz. Gain is a nominal 15 to 16 dB at 2 GHz at both bias points.

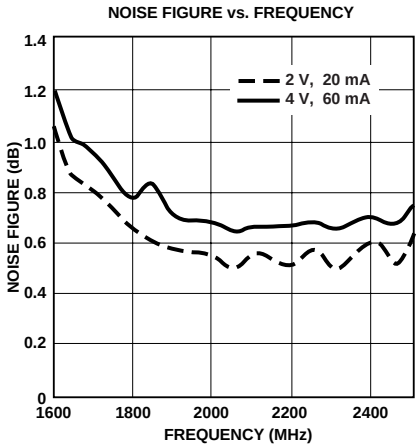

Figure 7. Amplifier #1 Noise Figure vs. Frequency.

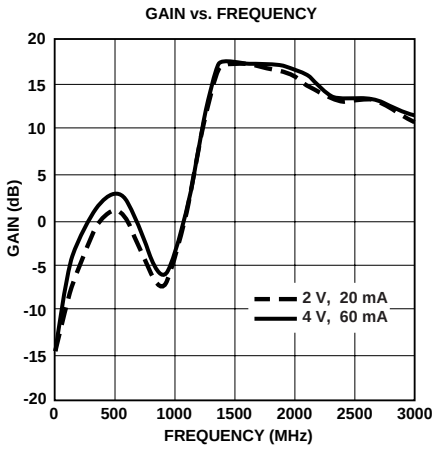

Figure 8. Amplifier #1 Gain vs. Frequency.

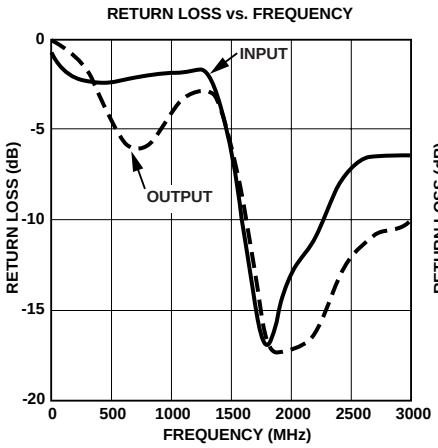

Figure 9. Amplifier #1 Input and Output Return Loss vs. Frequency at V_{ds} = 2 V and I_{ds} = 20 mA.

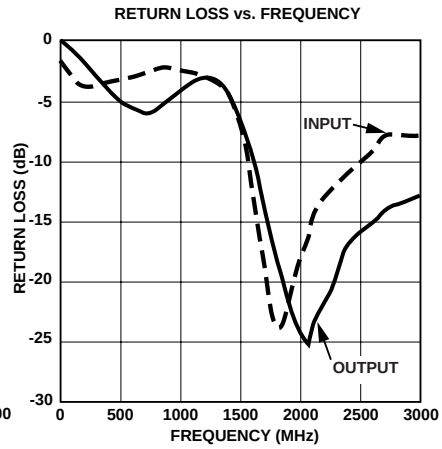

Figure 10. Amplifier #1 Input and Output Return Loss vs. Frequency at V_{ds} = 4 V and I_{ds} = 60 mA.

Measured input and output return loss is shown in Figures 9 and 10. The input return loss at 2 GHz at a bias point of V_{ds} = 2 V and I_{ds} = 20 mA is 14 dB with a corresponding output return loss of 19 dB. Note that best input return loss and minimum noise figure do not necessarily occur at the same frequency. This is due to Γ_o and S11* not occurring simultaneously at any one frequency.

When biased at a V_{ds} = 4 V and I_{ds} = 60 mA the input return loss improves to 18 dB and the output return loss improves to 24 dB.

The amplifier intercept point (IP3) was measured at several bias points, the results of which are shown in Table 2. The amplifier is capable of producing a very low noise figure coincident with good input and output return loss and a very good intercept point.

The amplifier was tested for P_{1dB} at two bias points. The first bias condition is at a V_{dsq} of 2 V and I_{dsq} of 20 mA which provides a P_{1dB} of +14 dBm for a power added efficiency of 58%. I_{ds} rises to about 21 mA at P_{1dB}. The second bias condition is at a V_{dsq} of 4 V and an I_{dsq} of 10 mA. A P_{1dB} of +18 dBm is achieved as I_{ds} increases to 30.2 mA. A power added efficiency of 52% is obtained. This data indicates the need for a power supply that allows the drain current to vary with RF drive level in order to achieve maximum power output. The use of active biasing (where the drain current, I_d, is held constant under varying RF drive level) will tend to limit the device's RF output power capability.

Table 2. Amplifier IP3 vs. Bias Point.

Bias Point	OIP3	IIP3
2 V 20 mA	+25 dBm	+9.5 dBm
3 V 20 mA	+28 dBm	+12.5 dBm
4 V 40 mA	+30.5 dBm	+14.5 dBm
4 V 60 mA	+31 dBm	+15 dBm

Design of ATF-34143 Amplifier # 2

The second amplifier is a self biased version of the first amplifier. High pass matching networks are also used to provide input and output matching. The schematic of the self biased amplifier is shown in Figure 11. The parts list for the second amplifier is shown in Table 3.

The demo board as modified for self biasing is shown in Figure 12. A two element network consisting of L1 and C1 provide the noise match for the device and is identical to that used in the first amplifier. A sourced biased amplifier requires that a resistor be inserted between the source and ground and that the gate be DC grounded. Therefore, capacitor C3 in amplifier #1 is not used and resistor R1 is connected directly to ground. Gate voltage will be zero due to negligible gate current flowing through R1. R1 also provides an effective low frequency resistive termination for the device which is necessary for stable device operation. The output matching network consisting of L4 and C5 is identical to amplifier #1. L4 also doubles as a means of inserting voltage to the drain. Capacitor C6 provides a good quality bypass at 2 GHz for L4. Resistor R3 and capacitor C7 provide a low frequency resistive termination for the device to provide stability.

The original demo board incorporates additional series microstriplines in both the input and output impedance matching networks. They are not required for this amplifier design and can be removed from the demo board. They should be replaced with a small 0.040" wide piece of etch. There is also space allocated for a resistor in series with the drain of the device. This resistor is also not required for this amplifier design and the gap should be bridged with a small piece of etch. The lower gain of the wider gate width 800 micron ATF-34143 as compared to the 400 micron ATF-35143 minimizes the need for resistive loading in the drain circuit. The slightly lower gain of the 800 micron device is offset by a potential improvement in stability and output power.

The first amplifier used shorting straps to attach each source pad to its corresponding ground pad. The second amplifier uses capacitors C3 and C4 to accomplish the RF grounding of Q1. This allows the addition of R2 to set the drain

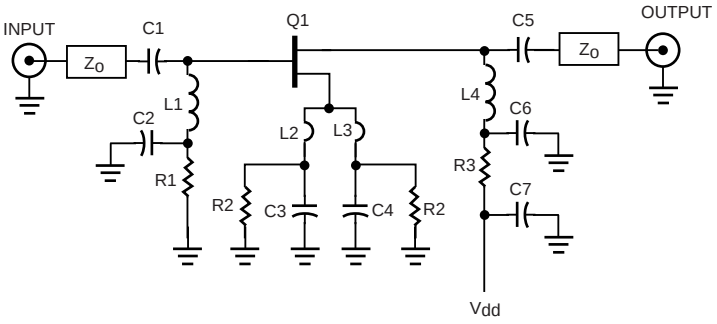

Figure 11. Schematic Diagram.

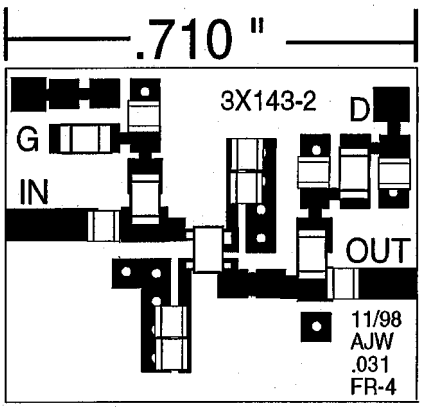

Figure 12. Component Placement Drawing for the ATF-34143 Low Noise Amplifier #2.

Table 3. Component Parts List for the ATF-34143 Amplifier #2.

Number	Description
C1	8.2 pF chip capacitor
C2, C6	8.2 pF chip capacitor
C3, C4	27 pF chip capacitor
C5	6.8 pF chip capacitor
C7	10000 pF chip capacitor
L1	2.7 nH inductor (Toko LL1608-F2N7S)
L2, L3	Place C3 and C4 a distance of 0.060" away from the source lead. See text.
L4	3.3 nH inductor (Coilcraft 0805CS-030XMBC) or (Toko LL1608-F3N3K)
Q1	Agilent Technologies ATF-34143 PHEMT
R1	50 Ω chip resistor
R2	Source resistor, suggest two 24 Ω resistors in parallel, one on each source lead, place resistors on source pad beyond point where C3 and C4 attach to source lead. Adjust R2 for desired I_d.
R3	12 Ω chip resistor
Zo	50 Ω Microstripline

current. C3 and C4 are placed approximately 0.060" away from the device source lead. This distance, called L2 and L3 in the schematic, can be used to optimize input return loss and gain. Be careful not to use excessive source inductance otherwise high frequency gain peaking will occur which will lead to instabilities and oscillations. See discussion in earlier section of this application note.

Performance of ATF-34143 Amplifier #2

The amplifier is biased at a V_{ds} of 2 volts with an I_d of 20.8 mA. Supply voltage, V_{dd}, is set at 2.5 volts. The measured noise figure and gain of the completed amplifier is shown in Figures 13 and 14. Noise figure is less than 0.67 dB from 1500 through 2500 MHz. Gain is nominally 16 dB at 1.9 GHz decreasing to 13.5 dB at 2500 MHz.

Measured input and output return loss is shown in Figure 15. The input return loss at 2 GHz is 18 dB while the output return loss measured 16.8 dB. Output IP3 was measured at a nominal +25 dBm.

Amplifier #2 can be rebiased at a V_{ds} of 4 V and I_d of 60 mA by readjustment of the source bias resistor R2. Performance similar to Amplifier #1 can be expected with the self-biased version.

LNA Optimization and Design for Other Frequencies

The basic designs presented in this application note can be scaled and/or optimized for use at other frequencies in the 1.5 to 2.5 GHz frequency range. C1 and L1 can be altered to optimize noise figure and input return loss for a particular application.

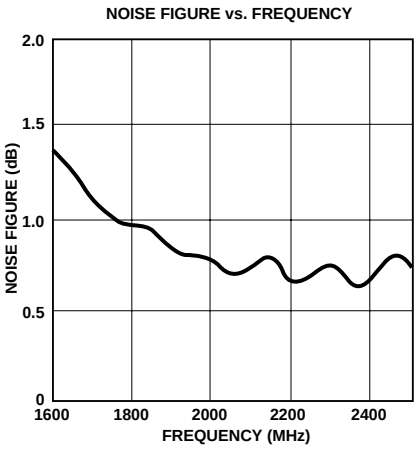

Figure 13. Amplifier #2 Noise Figure vs. Frequency.

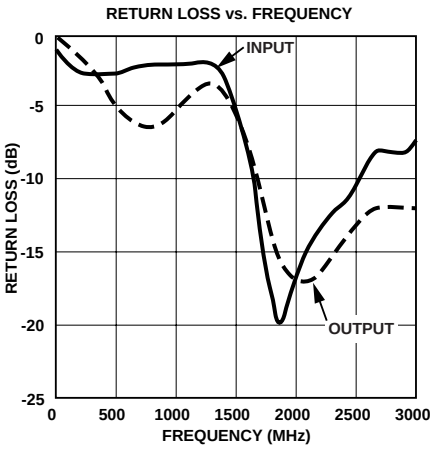

Figure 15. Amplifier #2 Input and Output Return Loss vs. Frequency.

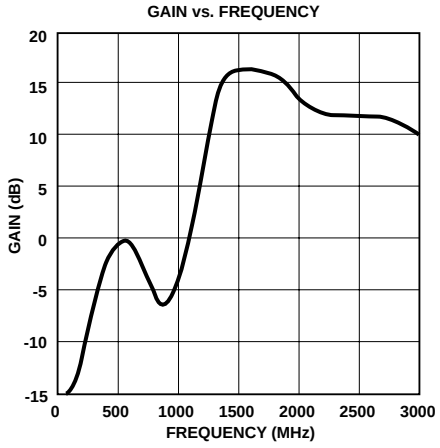

Figure 14. Amplifier #2 Gain vs. Frequency.

L4 and C5 will be the major factors effecting OIP3 and output return loss. As with any discrete transistor there will be interaction between input and output tuning because device S12 is not zero.

Conclusion

Two amplifier designs have been presented using the Agilent Technologies ATF-34143 low noise PHEMT. The ATF-34143 provides a very low noise figure along with high intercept point making it ideal for applications where high dynamic range is required. In addition to providing low noise figure, the ATF-34143 can be simultaneously matched for very good input and output return loss, making it easily cascadable with other amplifiers and filters with minimal effect on system passband gain ripple. The wide gate width of the ATF-34143 provides the added benefit of self-biasing requiring only a single power supply voltage.

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