Low Noise Amplifiers for 900 MHz using the Agilent ATF-34143 Low Noise PHEMT

Application Note 1190

Introduction

Agilent Technologies' ATF-34143 is a low noise PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. The ATF-34143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The 800 micron gate width of the ATF-34143 makes it ideal for applications in the VHF and lower GHz frequency range by providing low noise figure coincident with high intercept point. The wide gate width also provides lower impedances that are easy to match.

The ATF-34143 is described in low noise amplifiers for use in the cellular markets. The circuits are designed for use with 0.032 inch thickness FR-4 printed circuit board material. The amplifiers make use of low cost miniature wirewound and multilayer chip inductors for small size. When biased at a V_{ds} of 4 volts and an I_{ds} of 40 mA, the ATF-34143 amplifier will provide 18 to 20 dB gain, 0.4 dB noise figure and an output intercept point (IP3) of +29 to +30 dBm. An active bias solution using dual power supply techniques is discussed.

Biasing Options and Source Grounding

Passive biasing schemes are generally preferred for their simplicity. One method of passive biasing requires the source leads be direct dc grounded. A negative voltage is applied to the gate through a bias de-coupling network. The gate voltage is then adjusted for the desired value of drain current. The gate voltage required to support a desired drain current, I_d, is dependent on the device's pinchoff voltage, V_p, and the saturated drain current, I_{dss}. I_d is calculated with the following equation.

$$V_{gs} = V_p \left(1 - \sqrt{\frac{I_d}{I_{dss}}}\right)$$

Values for V_{gs} may be calculated from the typical I-V curves found in the data sheet.

The use of a controlled amount of source inductance can often be used to enhance LNA performance. Usually only a few tenths of a nanohenry or at most a few nanohenrys of inductance is required. This is effectively equivalent to increasing the source leads by only 0.050 inch or so. The effect can be easily modeled using one of the Agilent/ EEsof microwave circuit simulators. The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate width devices have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be. The ability of the 800 micron gate width ATF-34143 to tolerate greater source inductance allows the designer to take advantage of self-biasing, thereby only necessitating a single positive power supply.

LNA Design

The amplifier was designed for a V_{ds} of 4 volts and an I_{ds} of 40mA. Typical power supply voltage, V_{dd}, would be in the 5 volt range. The generic demo board shown in Figure 2 is used. The board gives the designer several design options for both the rf circuitry and biasing options. The demo board was designed such that the input and output impedance matching networks can be either lumped element networks or etched microstrip networks for lower cost. Either low pass or high pass structures can be generated based on system requirements. The demo board also allows the FET to be either self-biased or with grounded sources the FET can be biased with a negative voltage applied to the gate terminal.

The demo board is etched on 0.031" thickness FR-4 material for cost considerations.

Design of ATF-34143 Amplifier

The schematic diagram describing the dc grounded source amplifier is shown in Figure 1. The parts list for the first amplifier is shown in Table 1. The demo board as modified is shown in Figure 3. The modifications are discussed in the next section.

The amplifier uses a low-pass impedance matching network for the noise match. The low-pass network consists of a series inductor (L4) and a shunt inductor (L1). The demo board incorporates series microstripline on the input. It is not required for this amplifier design and can be removed from the demo board. It should be replaced with a series inductor, L4. The circuit loss will directly relate to noise figure, thus Q of L4 is extremely important. The Coilcraft 0603HS-12NTJBC or similar device is suitable for this purpose. Series capacitor (C1) provides low frequency gain reduction, which can minimize the amplifier's susceptibility to low frequency transmitter overload. C1 also doubles as a dc block. L1 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. The Q of L1 is also extremely important from the standpoint of circuit loss which will directly relate to noise figure. The Toko LL1608-FH56N is a small multilayer chip inductor with a rated Q of 32 at 500 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. This network has been optimized primarily for noise figure with secondary emphasis on input return loss. Resistor R1 and capacitor C3 provide low frequency stability by providing a resistive termination.

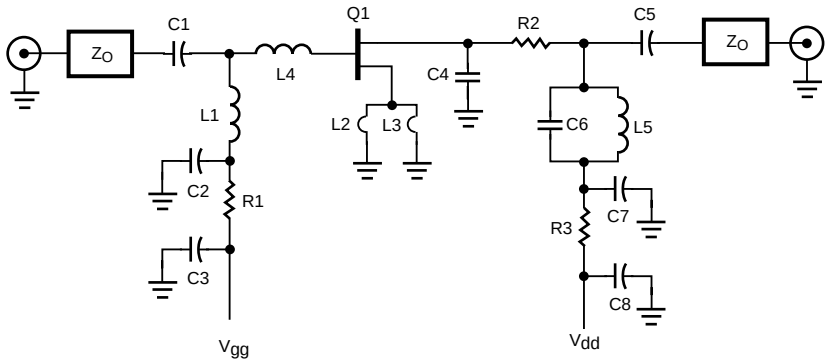

Figure 1. Schematic Diagram of the dc grounded source ATF-34143 Amplifier.

Table 1. Component Parts List for the ATF-34143 Amplifier.

C1	47 pF chip capacitor
C2	10 pF chip capacitor
C3, C8	1000 pF chip capacitor
C4	1.0 pF chip capacitor
C5	47 pF chip capacitor
C6	1.8 pF chip capacitor
C7	5.6 pF chip capacitor
L1	56 nH inductor (Toko LL1608-FH56N)
L2, L3	Strap each source pad to the ground pad with 0.040" wide etch. The jumpered etch is placed a distance of 0.070" away from the point where each source lead contacts the source pad.
L4	12 nH inductor (Coilcraft 0603HS-12NTJBC)
L5	8.2 nH inductor (Toko LL1608-F8N2)
Q1	Agilent Technologies ATF-34143 PHEMT
R1	47 Ω chip resistor
R2	12 Ω chip resistor
R3	15 Ω chip resistor
Zo	50 Ω Microstripline

The amplifier uses a tuned LC network to replace the normal high pass structure for the output impedance matching network. Due to the opposite behaviors of inductors and capacitors, the impedance of the parallel LC goes to infinity at the resonant frequency.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Some adjustments were made to the simulated component values to accommodate the use of preferred component values and small amounts of capacitance and inductance of the board. L5 also doubles as a means of inserting voltage to the drain. C4 provides the proper match for best output return loss and along with R2 and C7 provide amplifier stability out to 12 GHz. C4 also improves the input return loss by 1.5 dB and the

output IP3 performance by 3 dBm. Resistor R3 and capacitor C8 provide a low frequency termination for the device. There is also space allocated for a resistor in series with the drain of the device. R2 is placed here. C5 provides a dc block as well as important matching element for improved output return loss and rolls off low frequency gain.

Inductors L2 and L3 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstrip line, which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad is connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the amplifier, each source lead is connected to its corresponding ground pad at a distance of approximately 0.070" from the source lead. The 0.070" is measured from the edge of the source lead to the closest edge of the ground strap. The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. More on this subject next.

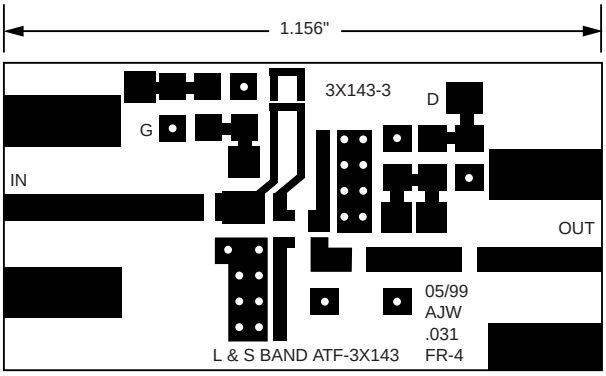

Figure 2. Artwork for the ATF-34143 Low Noise Amplifier.

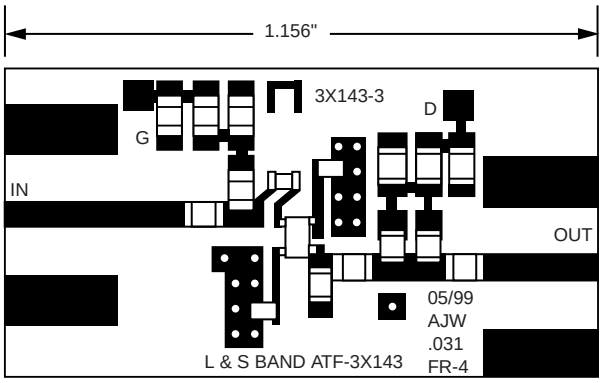

Figure 3. Component Placement Drawing for the ATF-34143 Low Noise Amplifier #1.

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far? For an amplifier operating in the 900 MHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in the 6 to 10 GHz frequency range. Normally the high frequency gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is OK as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device.

Performance of ATF-34143 Amplifier

The amplifier is biased at a V_{ds} of 4 volts and I_d of 40 mA. Typical V_{gs} is -0.41 volts. The measured noise figure and gain of the completed amplifier is shown in Figures 4 and 5. Noise figure is a nominal 0.4 to 0.45 dB from 700 through 1200 MHz. Gain is a minimum of 15 dB from 700 MHz through 1200 MHz with a peak of 20.3 dB at 700 MHz.

Measured input and output return loss is shown in Figure 6. The input return loss at 900 MHz is 10.8 dB with a corresponding output return loss of 13.3 dB. Note that best input return loss and minimum noise figure do not necessarily occur at the same frequency. This is due to G_o and S11* not occurring simultaneously at any one frequency.

The amplifier output intercept point OIP3 was measured at a nominal +29 dBm at a dc bias point of 4 volts V_{ds} and an I_d of 40 mA. P-1dB measured +17.5 dBm.

Conclusion

The amplifier designs have been presented using the Agilent Technologies ATF-34143 low noise PHEMT. The ATF-34143 provides a very low noise figure along with high intercept point making it ideal for applications where high dynamic range is required. In addition to providing low noise figure, the ATF-34143 can be simultaneously matched for very good input and output return loss, making it easily cascadable with other amplifiers and filters with minimal effect on system passband gain ripple.

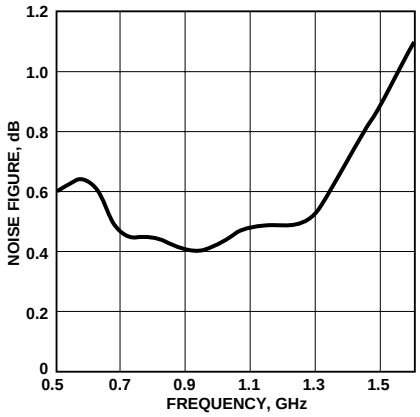

Figure 4. Amplifier Noise Figure vs. Frequency.

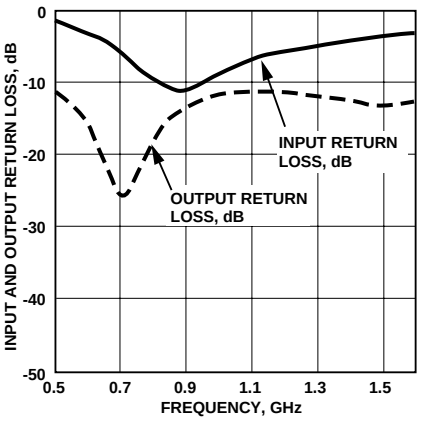

Figure 6. Amplifier Input and Output Return Loss vs. Frequency.

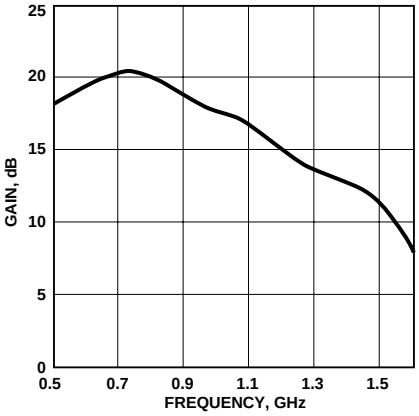

Figure 5. Amplifier Gain vs. Frequency.

References

Performance data for ATF-34143 PHEMT may be found on www.semiconductor.agilent.com

Application Notes

Applications Bulletin: Low Noise Amplifiers for 1500 MHz through 2500 MHz using the ATF-34143 Low Noise PHEMT - A.J. Ward

5968-9128E (2/00)

Agilent Technologies
Innovating the HP Way