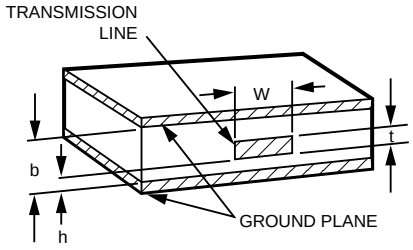
Agilent HDMP-1636A and HDMP-1646A Gigabit Ethernet Transceiver Design Considerations

Application Note 1205

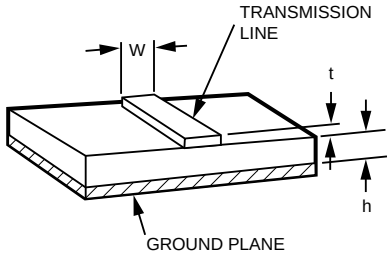
Introduction

The HDMP-1636A/1646A[1] ICs are complete 1.25 GBd Gigabit Ethernet transceivers in a single IC and compatible with the IEEE 802.3z Gigabit Ethernet standard [2]. The HDMP-1636A and HDMP-1646A are +3.3 V parts available in a 10x10 mm and 14x14 mm QFP plastic package respectively. Both parts use the same silicon bipolar die. The transmitter is designed to serialize a 8b/10b encoded 10 bit wide word and transmit it across either cable or to an external fiber optical transceiver. At the other end of the link, the receiver of another HDMP-1636A/46A takes the serialized data and reconstructs the 10 bit parallel word. The transceiver contains all the necessary high-frequency circuitry, PLL, mux, demux, clock, data recovery circuitry, cable driver and cable equalizer.

The purpose of this application note is to show how to get the best possible performance from the IC and take advantage of its capabilities. Information on how to test the HDMP-1636A/46A and the equipment required is discussed. Guidelines for PC board layout are also discussed in detail. The HDMP-1636A/46A incorporates the latest in PLL and high frequency design techniques. It removes the difficult job of dealing with such circuitry, but does require that the designer use and understand proper layout techniques in order to get the best performance from the IC. The next section briefly covers some of these important topics.



(a) STRIPLINE TRANSMISSION LINE



(b) MICROSTRIP TRANSMISSION LINE

Figure 1. Stripline and Microstrip Dimensions Defined

Signal Interconnections

The parallel data outputs of the HDMP-1636A/46A are TTL compatible and are TTL +5 V tolerant. The high-speed serial lines from the TX to the RX are Positive ECL (PECL) connections. The TTL lines have rise/fall times that are typically 1.1 to 1.5 ns and the high-speed lines have rise/ fall times that are in the range of 200 ps. Because of these fast rise/fall times, interconnects should be treated as transmission lines rather than simple wire connections. Using transmission lines with a basic understanding of line matching will reduce signal reflection which degrades overall performance of the part. Before discussing the various methods of connecting the I/Os it is useful to briefly cover the topics of microstrip and stripline transmission lines since their characteristics determine layout practice.

Figure 1a defines the dimensions of stripline. In this case the signal transmission line is sandwiched between the dielectric material of the PC board and two conducting ground planes. Impedance of the transmission line is determined by the relative dielectric constant (ε_r) of the PC board material, thickness of the dielectric (h), and the width of the copper transmission line strip (w). The impedance is also affected when the thickness of the copper strip (t) becomes significant compared to the value h.

Figure 1b defines the dimensions of microstrip. In this case the signal transmission line is open to air on the topside and has PC board material and a conducting ground plane underneath it. Impedance of the transmission line is determined by the relative dielectric

constant (ε_r) of the PC board material, its thickness (h), and the microstrip trace width (w). Thickness of the copper strip can also be significant in the impedance calculation. Calculation of the microstrip impedance is more difficult than stripline, because the electric fields from the transmission line propagate through two different dielectric materials; air and the PC board.

The following equations for calculating microstrip and stripline impedance are often referenced in the literature [3,4,5]. These equations are useful as a first order approximation. More accurate equations exist, but the approximation equations are adequate for most digital design work. More accurate equations are available in the literature [6].

The characteristic impedance Zo of the microstrip is calculated using the approximation:

$$Zo = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right]$$

The propagation delay for microstrip is:

$$t_{pd} = 1.017\sqrt{0.475\varepsilon_r + 0.67}$$

$$Co = \frac{t_{pd}}{Zo} \quad \text{(pF/ft)}$$

where:
ε_r = relative dielectric constant of the PCB board
Zo = characteristic impedance of the transmission line
Co = capacitance of the transmission line

The characteristic impedance for stripline is calculated using the equation:

$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4b}{0.67\pi(0.8w + t)}\right]$$

and propagation delay is:

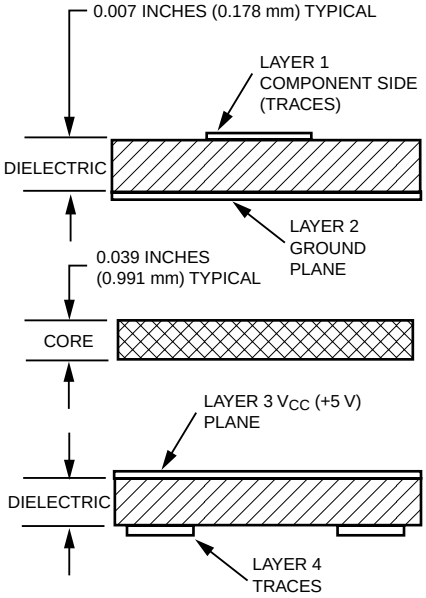
$$t_{pd} = 1.017\sqrt{\varepsilon_r} \quad \text{(ns/ft)}$$

Dielectric constant (ε_r) of glass-epoxy board (FR4) varies from about 4.4 to 5.0. As an example, calculating the transmission line impedance and propagation delay for microstrip using the variables ε_r = 4.4, h = 7 mils, w = 12 mils and t = 0.7 mils results in Zo = 50.6 Ω, tpd = 140.8 ps/in. and Co = 2.78 pF/in. Reflections can be minimized by keeping the total round trip delay of the transmission line shorter than the rise or fall time of the driving signal. This number is an approximation only, since it depends on the dielectric constant which can vary over a wide range, the impedance of the transmission line used and the load at the end of the line.

PC Board Layout

Proper PC Board layout is important in order to minimize parasitic capacitance and inductance which can cause ringing and poor VSWR match on the high-speed serial lines. It is also important to use transmission lines with controlled impedance on all frame rate and serial rate lines. Figure 2 shows a 4 layer PC board structure used to build the HDMP-163K evaluation board [7]. Standard FR4 material was used with a typical relative dielectric constant (ε_r) of 4.4.

Input and output lines that require controlled impedance are placed on layers 1 and 4. The microstrip



LAYERS 1 AND 4: 1/2 OZ. COPPER FOIL = 0.0007 INCHES (0.0178 mm) THICK.

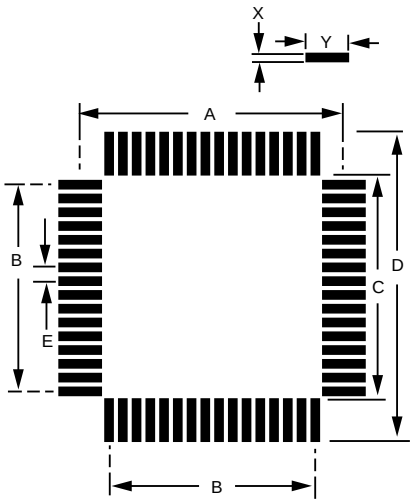
LAYERS 2 AND 3: 1 OZ. COPPER FOIL = 0.0014 INCHES (0.0356 mm) THICK.

ε_r = 4.4

Figure 2. Multilayer PC Board Structure.

media is formed from the combination of layer 1, the dielectric material, and the solid copper plane of layer 2. The same scheme is used for layers 3 and 4. Transmission line widths are 0.012 inches (0.3048 mm) for 50 Ω using the thickness and dielectric constant of Figure 2. Data lines should be of equal length in order to minimize skew between lines. The high-speed serial differential lines should also be routed together for the same reason.

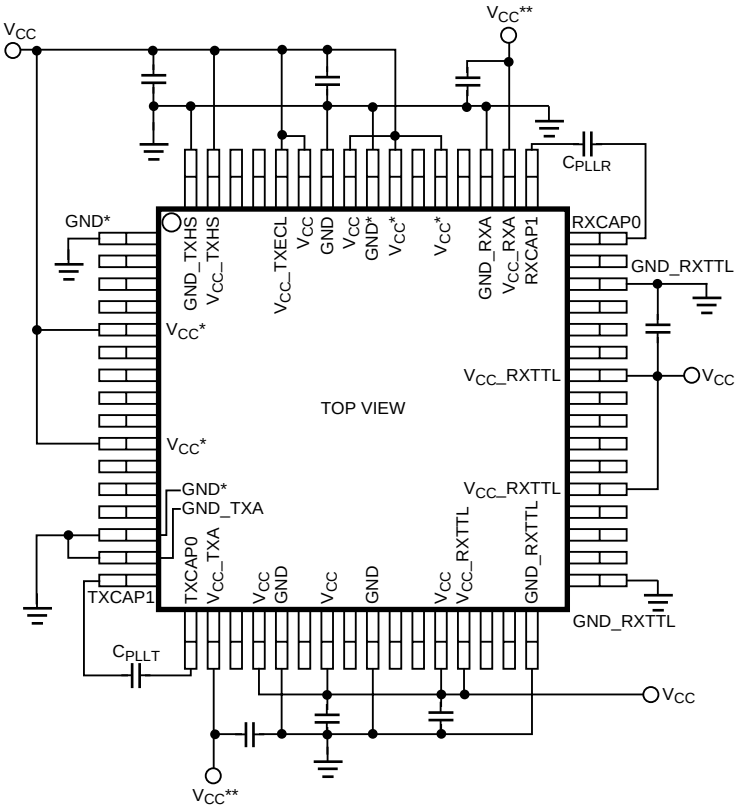
The HDMP-1636A conforms to the QFP 10x10 -64 package outline and the HDMP-1646A conforms to the QFP 14x14 -64 package outline. Figure 3 shows the recommended PC board land pattern recommended to conform to the package leads [8].



	HDMP-1646A	HDMP-1636A
A	16.00	12.00
B	12.00	7.5
C	14.2	10.2
D	17.8	13.8
E	0.80	0.50
X	0.5	0.30
Y	1.80	1.80

All dimensions are in mm.

Figure 3. HDMP-1636A/46A PC board Land Pattern.



** SUPPLY VOLTAGE INTO V_{CC}_RXA AND V_{CC}_TXA SHOULD BE FROM A LOW NOISE SOURCE. ALL BYPASS CAPACITORS = 0.1 µF.

Figure 4. Power Supply Bypass.

Power Supply Decoupling

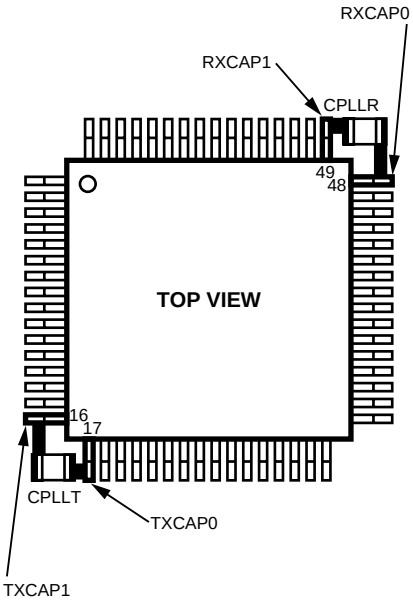
The HDMP-1636A/46A removes much of the burden of high-frequency design from the designer, but it does require that good layout and bypass techniques are used to get the best performance from the IC. Bypass capacitors should be used and placed as close as possible to the appropriate power supply pins of the HDMP-1636A/46A as shown on the schematic of Figure 4. The voltage into these pins should be clean with minimum noise.

PLL Loop Filter Capacitors

The PLL loop filter capacitors and pin locations on the transceiver IC are shown in Figure 5. Notice that only two capacitors are required; CPLLT for the transmitter and CPLLR for the receiver. Nominal capacitance is 0.1 µF. The maximum voltage across the capacitors is on the order of 1 volt, so the capacitor can be a low voltage type and physically small. The PLL capacitors are placed physically close to the appropriate pins on the transceivers as shown in Figure 5. Keeping the lines short will prevent the PLL loop capacitors from picking up stray noise from surrounding lines or components.

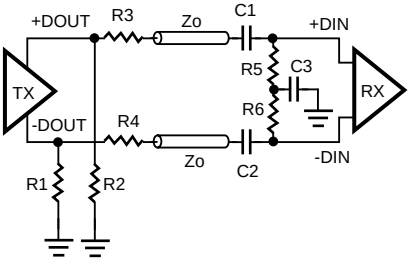
I/O Interfacing

The HDMP-1636A/46A has four different I/O types as summarized in Table 1. The I-TTL and O-TTL are compatible to standard TTL. The high-speed serial lines are Positive ECL (PECL) output voltage swings, but are designed to be AC coupled. All I/O connections have ESD protection diodes. Figure 6 shows the high-speed serial connections. Resistors R1 and R2 (150 Ω) sets the DC bias current through Dout+ / Dout- . The value of R5 and R6 depends on the impedance of the transmission line that the transmitter drives. Their values are simply equal to the transmission line impedance. For Z0 = 75 Ω; R5 and R6 = 75 Ω, and for Z0 = 50 Ω ; R5 and R6 = 50 Ω. The optional series padding resistors (R3 and R4) help dampen load reflections. Typical



CPLLR, CPLLT = 0.1 µF PLL LOOP FILTER CAPACITORS.

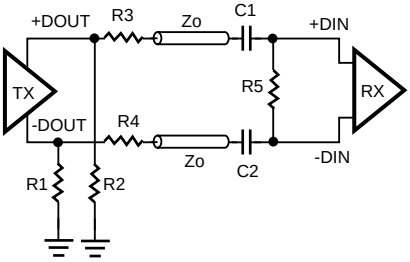
Figure 5. Placement of the PLL Loop Filter Capacitors.



R1 = R2 = 150 OHMS, R3 = R4 = OPTIONAL (SEE TEXT)

R5 = R6 = Zo C1 = C2 = C3 = 0.01 µF

(a) HIGH SPEED Tx TO Rx CONNECTION.



R1 = R2 = 150 OHMS, R3 = R4 = OPTIONAL (SEE TEXT)

R3 = R4 = Zo C1 = C2 = 0.01 µF

R5 = 2Zo

(b) HIGH SPEED Tx TO Rx CONNECTION WITH SINGLE TERMINATION RESISTOR.

Figure 6. High-Speed Serial Line Connection.

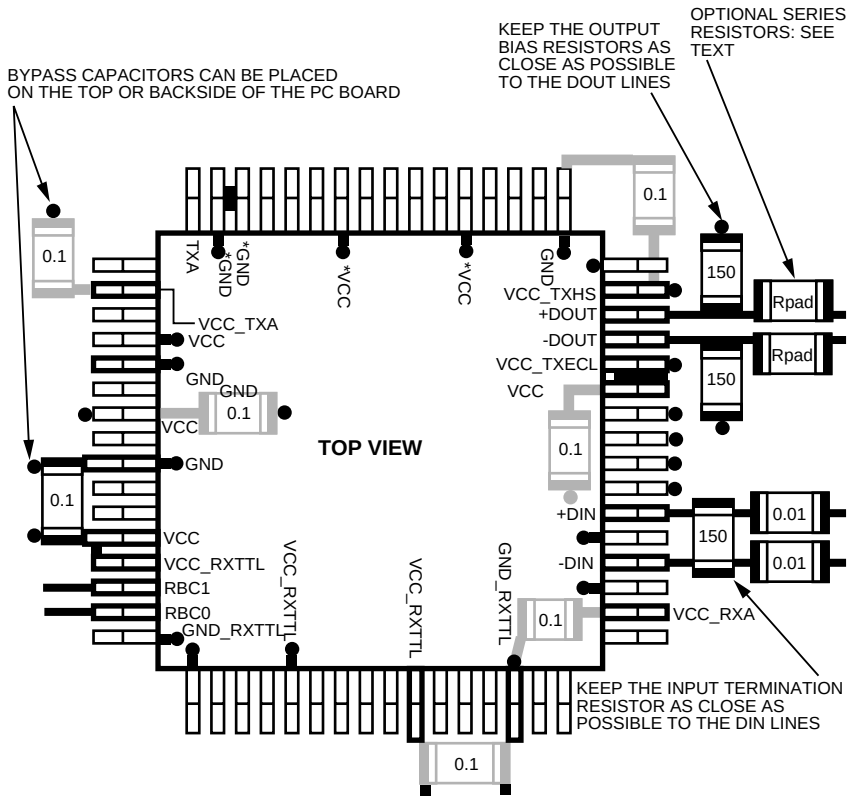


Figure 7. Layout Example

Table 1. I/O Type Definitions and PIN Usage.

I/O Type	Definition	Used on Pins:
I-TTL	Input TTL. Floats high when left open	TX[0...9], LOOPEN, REFCLK, ENBYTSYNC
O-TTL	Output TTL	RX[0...9], RBC0, RBC1, BYTSYNC,
HS_OUT	High-Speed Output. PECL Compatible.	+DOUT, -DOUT
HS_IN	High-Speed Input. PECL Compatible.	+DIN, -DIN

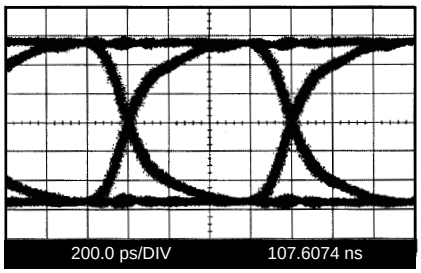
padding resistor values for mismatched loads range from 25 Ω to 75 Ω. A single differential termination resistor can also be used as shown in Figure 6b. Its value is simply 2Zo or 100 Ω for 50 Ω transmission lines and 150 Ω for 75 Ω transmission lines. Notice that the +DIN / -DIN input pins do not require any external bias resistor. Bias is applied internally on the chip. Figure 7 shows an example of the PC board layout highlighting the placement of the high-speed terminations.

Thermal Considerations- HDMP-1636A/46A

The body of the package is composed of a high temperature plastic. Because of the very low power dissipation of the +3.3 V parts (630 mW typical), no internal heat spreader is used in these plastic package parts. The HDMP-1636A has a typical junction to thermal resistance number of 11 C/W and the HDMP-1646A is typically 8 C/W per the data sheet.

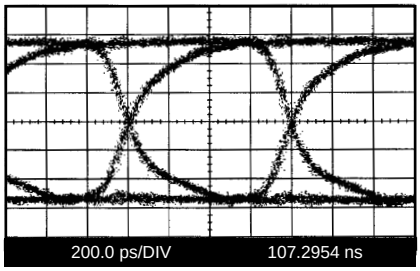
Applications Support

System designers can quickly evaluate the HDMP-1636A or the HDMP-1646A by ordering the HDMP-163K evaluation board. This is a completely assembled board for the HDMP-1636A transceiver (electrical performance is the same as the HDMP-1646A). The evaluation board is designed to make it quick and easy to evaluate the transceiver chip. The board brings out all pins from the chip to various connectors and jumper options. It can be used in a stand-alone configuration, or connected to an external host. The parallel interface to the host is through a 2x10 ribbon header on the input and a 2x14 ribbon header on the output. SMA connectors are provided on all the high-speed serial coax lines, and on the reference clock input (REFCLK). A socket for an onboard reference clock at 125 MHz is also provided. A BER much better than 1 x 10^{-14} can be routinely measured using the HDMP-163K evaluation board. This is over 24 hours of error free operation at 1.25 GB. Figure 8 shows the eye diagram at 1.25 GB when measured using an Agilent 83480A Communications Analyzer connected to the Dout- coax port of the HDMP-1636A.



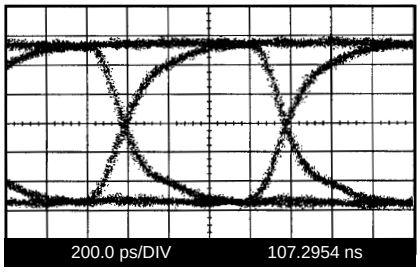
f1 300 mV/DIV

(a) DIFFERENTIAL OUTPUT (DOUT±DOUT-).



f1 150 mV/DIV

(b) DOUT+



f1 150 mV/DIV

(c) DOUT-

Figure 8. Eye Diagrams of the high-speed serial outputs from the HDMP-1636A as captured on the Agilent 83480A Digital Communications Analyzer. The equipment setup of Figure 8 was used with a PRBS = 2^{7}-1.

Fiber-Optic Interface

Figure 9 shows how the HDMP-1636A/46A can be connected to the HFBR-53D5 multimode, 1-row-of-9-pins (1x9) VCSEL fiber-optic transceiver. The following are some suggested layout guidelines when using the HDMP-1636A/46A and HFBR-53D5.

• Use controlled impedance transmission lines on the parallel and high-speed serial lines.

• Route the high-speed differential lines together and keep them of equal length to minimize pulse-width distortion.

• Use differential signals to interconnect components. Avoid unbalanced, single-ended use of the high-speed data lines which can cause pulse-width distortion.

• Place power supply filter circuits as close as possible to the V_{CC} pins of the fiber-optic transceiver and SERDES for best noise filtering.

• The SERDES can have a V_{CC} “island” of metal cut out from the common digital +3.3 volt V_{CC} plane. This island can be located under the SERDES. The digital V_{CC} can be bridged over to the SERDES V_{CC} “island” via the ferrite bead as shown in Figure 9.

• The HFBR-53D5 can have an “island” of metal cut out of the common +5 volt V_{CC} plane and located under the receiver section of the HFBR-53D5. The +5 volt digital V_{CC} can then be bridged over to the receiver V_{CC} “island” via the 1 µh inductor as shown in Figure 9. The power suppy bypass capacitors must be as close as possible to the transmitter V_{CC} pin.

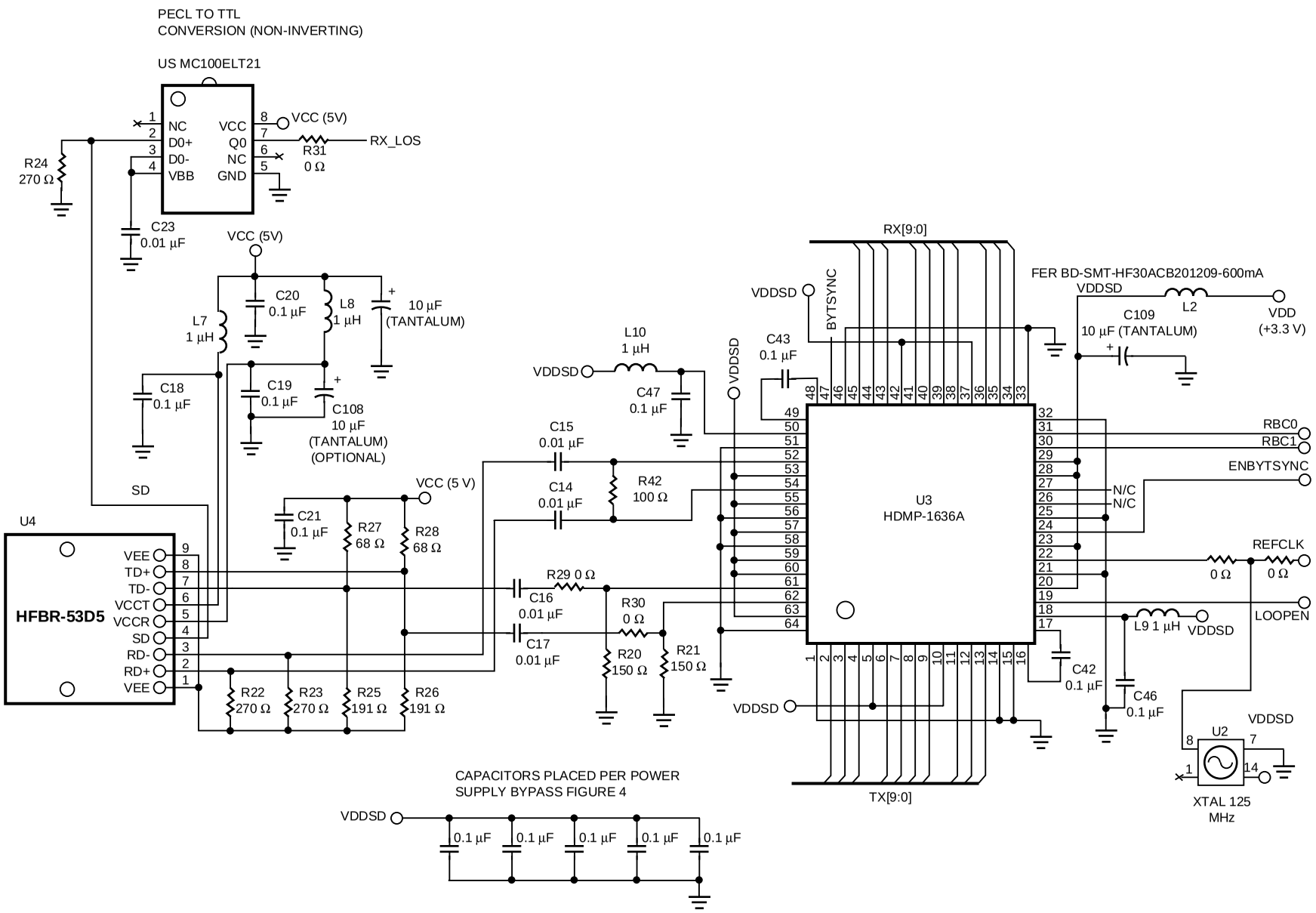


Figure 9. HDMP-1636A/46A and HFBR-53D5 reference schematic.

• Keep high-speed load and source resistors close to their respective pins. A source or load resistor will not be as effective when positioned physically far from its respective pin. Using 0603 size components on the high-speed terminations and series capacitors makes layout easier. The 0603 size compared to 0805 is smaller, which reduces unwanted parasitics (less inductance) and since they are physically small, they are easier to position close to the required pins.

• Use short transmission lines between the SERDES parallel I/Os and a MAC or protocol IC. Choose shorter parallel lines at the expense of longer high-speed differential lines between the SERDES and the fiber-optic module. The Tx high-speed outputs can drive longer lengths of microstrip transmission lines than the Rx TTL outputs.

• Mount the Tx and Rx PLL charge pump capacitors close to their respective pins and keep the connections to these capacitors short.

Jitter Performance

The HDMP-1636A/46A meets the jitter budget in Table 38-10 of the IEEE 802.3z Gigabit Ethernet specification [9]. Transmitter jitter transfer, jitter tolerance and V_{CC} jitter transfer curves for the SERDES are provided in the next sections. Although not required by the Gigabit Ethernet standard, the graphs are useful information in understanding the performance of the SERDES.

Jitter Transfer

Jitter transfer for the transmitter PLL is shown in Figure 10. The curves are generated by modulating REFCLK (125 MHz) with a sinusoidal waveform and measuring the resulting jitter transferred or imposed on the high-speed 1.25 Gb/s transmitter output lines. In this case the sinusoidal waveform is swept from 10 KHz to about 7 MHz. The PLL behaves like a low-pass filter to any noise present on REFCLK. Below the corner frequency (f - 3 dB) of about 1 to 2 MHz, frequencies are passed with no attenuation. Only a slight 0.6 dB amplification of the modulating signal occurs at the corner frequency. The REFCLK modulation signal is attenuated when it exceeds the corner frequency of the PLL's low pass filter response. The vertical axis is expressed in jitter gain (dB). Because of the non-linear nature of the PLL, the corner frequency is also a function of the jitter amplitude. The jitter amplitude is varied from 0.05 UI to 1 UI resulting in the 4 different curves shown in Figure 10. UI stands for Unit Interval, and is a traditional unit of measurement for jitter amplitude. One UI is defined as the 800 ps time interval of one 1.25 GB symbol. When jitter is equal to 800 ps, the phase deviation of the clock is equal to 1 UI.

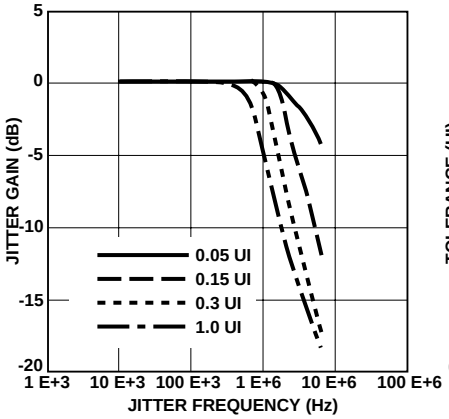


Figure 10. Tx Jitter Transfer for the HDMP-1636A/46A.

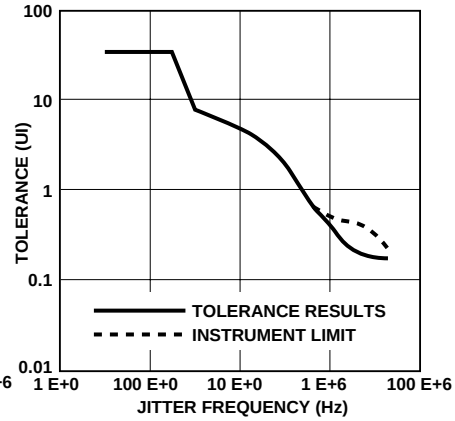


Figure 11. Jitter Tolerance for the HDMP-1636A/46A.

Jitter Tolerance

Jitter tolerance is a measure of design margin in a serial communications link. The purpose of the test is to measure the transceiver's error performance as a function of sinusoidal jitter at various frequencies and amplitude levels. There is no jitter tolerance mask in the Gigabit Ethernet standard. The following is provided as informative information only. Sinusoidal jitter is added to REFCLK. In this test, random and deterministic jitter are added in order to simulate a real system. Random jitter (0.287 UI) is added using a random noise generator (noise diode generator), and deterministic jitter (0.462 UI) is added using a fixed amount of coax cable. Detailed information on jitter tolerance measurement techniques is contained in the work done by the Fibre Channel Jitter Working Group and is a good reference [10]. Figure 11 shows the results of this test. The lower curve is the measured behavior of the HDMP-1636A/46A transceiver. Note that below about 300 KHz, the transceiver can tolerate jitter above 1 UI. If viewed on a digital oscilloscope, this corresponds to no eye opening. At these frequencies, the PLL

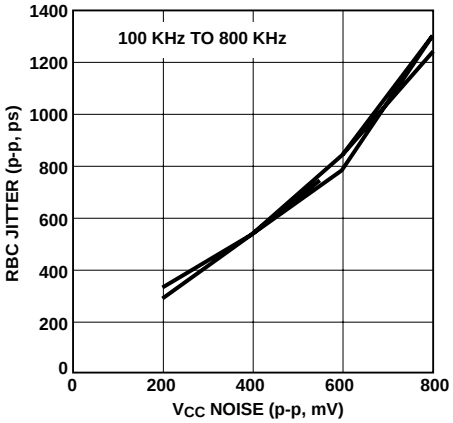


Figure 12. V_{CC} Noise Tolerance for the HDMP-1636A/46A.

is capable of tracking the input signal even when jitter causes the data to move more than 1 symbol time (800 ps). The transceiver's ability to track jitter decreases as frequency increases. A general discussion of measuring jitter transfer, jitter tolerance and the equipment used for such tests is available in the literature [11,12].

V_{CC} Jitter Transfer

Figure 12 shows the excellent noise immunity that the transceiver has against power supply noise. The graph shows the Rx recovered clock output (Rbc) jitter as the sinusoidal V_{CC} noise is increased in amplitude from 100 mV pk-pk to about 800 mV pk-pk. Curves are overlaid from 100 KHz to 800 KHz and show only 1.2 ns pk-pk jitter on Rbc with a V_{CC} noise level of 800 mV pk-pk! It would be difficult to create this much V_{CC} supply noise in an actual system when using the recommended bypass techniques. The data taken for this test used an evaluation board (HDMP-163K) with all bypass capacitors removed from the PC board, leaving only the intrinsic capacitance formed by the V_{CC} and ground plane layers.

Driving Copper Cable

The Gigabit Ethernet Standard [2] calls out two types of high-speed connectors; the 9 pin dB9 and the HSSDC. The HDMP-1636A/46A transceiver is fully capable of directly driving 25 meters of duplex Twinaxial copper cable. Twinaxial cable is a form of shielded twin-lead.

References

[1]. HDMP-T1636A/1636A/1646A Gigabit Ethernet Transceiver Chip Data Sheet, publication number 5968-3339E (5/99).

[2] IEEE 802.3z Gigabit Ethernet Interface Specification.

[3] Kaupp, H.R., "Characteristics of microstrip transmission lines," IEEE Trans. Electronic Computers, vol. EC-16, Apr. 1967.

[4] Springfield, W.K., "Multilayer printed circuitry in computer applications," presented at the Fall Meeting on Printed Circuits, Chicago, Ill., Oct. 1964.

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[8]. SQFP/QFP(Square) land pattern dimensions, "Surface Mount Design and Land Pattern Standard", Institute for Interconnecting and Packaging Electronic Circuits (IPC) IPC-SM-782 Rev A August 1993. 708-677-2850.

[9] IEEE Draft 802.3z Gigabit Ethernet Interface Specification, section 38.5 Table 38-10," 1000BASE-SX and 1000BASE-LX jitter budget".

[10] Fibre Channel Methodologies of Jitter Specification (MJS) - Jitter Working Group Technical Report, ANSI Rev 10.

[11] Agilent 71501C Jitter Analysis System Product Overview, publication number 5965-0801E

[12] Christopher Miller, David McQuate, "Jitter Analysis of High-Speed Digital Systems", HP Journal, Vol. 46A, no. 1, Feb 1995, pp 49-56.

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