Agilent SC Duplex +3.3 V Single Mode Transceivers

Application Note 1225

Introduction

This application note details the recommended circuit connections for Agilent's SC Duplex +3.3 V Single Mode Transceiver products shown in Table 1.

Agilent supplies an evaluation board HFCT-5800 to enable easy evaluation of the HFCT-5801 and HFCT-5805.

All products listed in Table 1 are 155 Mb/s SONET/SDH compliant SC receptacled transceivers.

Table 1 gives details of the options available for these products.

Functional Description

Transmitter Section Design

The transmitter section, shown in Figure 1, uses a laser as its optical source which has been designed to be compliant with IEC 825 eye safety requirements under fault conditions. The optical output is controlled by a custom IC which detects the laser output via the monitor photodiode. This IC provides both dc and ac current drive to the laser to ensure correct modulation, eye diagram and extinction ratio over temperature, supply voltage and end of life. Facilities are provided to monitor the laser bias and monitor diode status on the 2 x 9 products listed in Table 1.

Electrical Characteristics

Supply Voltage

The transceiver module operates with a positive supply voltage in the range +3.1 V to +3.6 V. Pins labeled N/C must not be connected.

Care should be taken to avoid power supply transients. These products are not recommended for 'hot plug' applications.

Table 1. Agilent's Single Mode SC Duplex +3.3 V Transceiver Products

Part Number	+3.3 V	Intermediate Reach	1 x 9 Pinout	2 x 9 Pinout	-40°C to +85°C	0°C to +70°C	Black Case	Blue Case
HFCT-5805A	✓	✓	✓		✓		✓	
HFCT-5805B	✓	✓	✓			✓	✓	
HFCT-5805C	✓	✓	✓		✓			✓
HFCT-5805D	✓	✓	✓			✓		✓
HFCT-5801A	✓	✓		✓	✓		✓	
HFCT-5801B	✓	✓		✓		✓	✓	
HFCT-5801C	✓	✓		✓	✓			✓
HFCT-5801D	✓	✓		✓		✓		✓

Agilent Technologies

Noise Immunity

It is recommended that the power supply filter network illustrated in Figure 2 is used to further improve device performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Power Supply Filtering

Good power supply filtering is required for optimum transmitter performance. When using the recommended filter arrangement, power supply noise >100 mV pk-pk, over a frequency range of 10 Hz to 1 MHz, can be tolerated before hits on a 10% eye mask margin occurs.

Data Inputs

The Data and $\overline{\text{Data}}$ inputs will accept standard LVPECL levels (10 KH). The use of standard logic levels is recommended although inputs will toggle with swings between 250 mV and 1 V peak to peak when driven differentially.

Both inputs are internally tied to V_{CC} -1.3 V.

Single-ended operation is not recommended as data sheet specifications can only be guaranteed when both differential inputs are used.

Transmitter Signal Input

The inputs to the transceiver module transmitter will require a 50% duty cycle or dc balanced signal for normal operation. Failure to provide this may cause the optical parameters to move out of specification. Extinction ratio and duty cycle distortion may be affected. The lower cutoff frequency of the transmitter mean power control loop is <20 KHz.

The module will function with up to 72 consecutive 1's or 0's within the PRBS pattern as specified by CCITT G.957 (ITU) for STM-1.

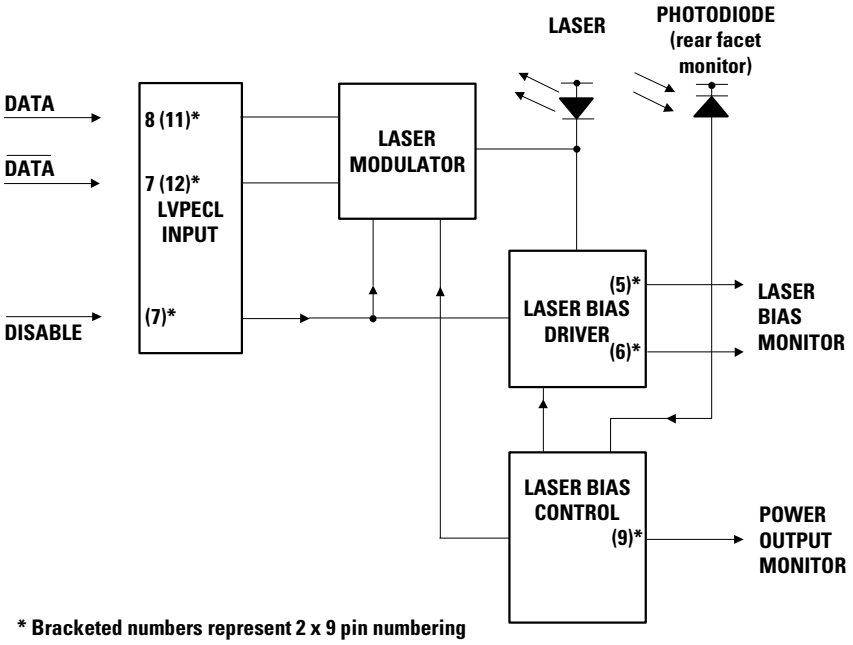


Figure 1. Simplified Transmitter Schematic

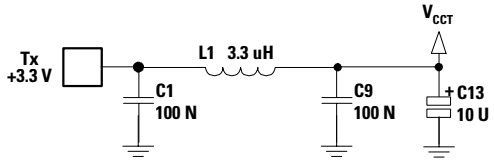


Figure 2. Recommended Transmitter Power Supply Filtering

In the absence of data the transmitter will emit a mean optical power within the specified limit.

Analog Monitor Points
Bias Monitor

The external connections to the laser bias monitor for the HFCT-5801 are implemented as in Figure 3.

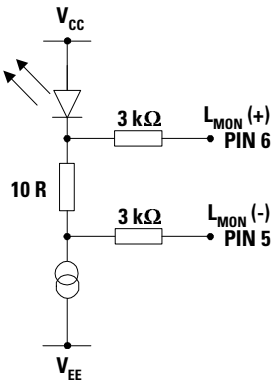


Figure 3. Bias Monitor External Connections for the HFCT-5801

During normal (modulated) operation the bias current will correspond approximately to laser threshold. In the absence of data the bias current will be equal to the laser forward current required to give the correct optical output power. This will equate to the laser bias current plus half of the current previously supplied by the data modulation current, Equation A.

$$\text{Equation A: } I_{bias} = I_{th} + \frac{I_{mod}}{2}$$

The differential voltage generated between pin 5 and pin 6 is 10 mV/mA with a common mode voltage of approximately V_{CC} -1.6 V (to Pin 6).

This monitor may be used to detect an end-of-life bias current. A typical example is to have an end-of-life current of 70 mA. This will give a differential voltage of 0.7 V at end-of-life and Tmax. It is important to note that if such an alarm is used - the absence of data will increase the bias current and may cause a false alarm. Users should note that bias current is temperature dependent. For more accurate alarms a temperature compensated operational alarm point will need to be provided by the user. For most applications a 70 mA end-of-life alarm will be sufficient.

Power Monitor

For the HFCT-5801, external connections are provided to the monitor photodiode that measures the rear facet power of the laser diode, as shown in Figure 4. This connection is part of the output power control loop.

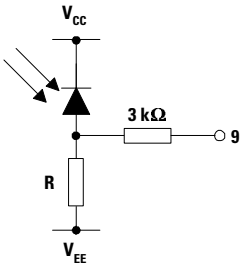


Figure 4. Laser Power Monitor External Connection for the HFCT-5801

Under normal operation, modulated or not, this voltage will remain constant ±10% (over life, over temperature). The dc voltage is measured at pin 9. The voltage on pin 9 is nominally 1.28 V with respect to V_{EE} (a bandgap voltage). Note this voltage should be measured into a high impedance.

This monitor may be used to detect a high or low optical power failure. Any such failure would be catastrophic and so the alarm should be set to ±50% of the initial value to detect gross movement.

It is recommended that an airflow of ≥ 2 m/s be provided to ensure that the case temperature does not exceed the specified maximum operating ambient temperature.

Functional Description

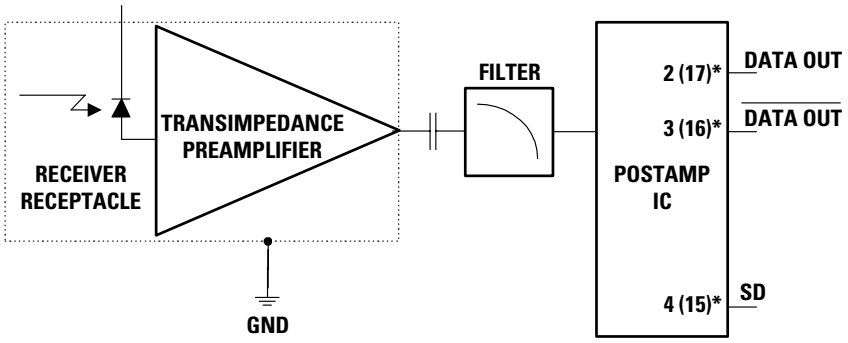
Receiver Section

Design

The receiver section contains an InGaAs/InP PIN diode and a preamplifier within the receptacle. This couples to a single postamp and Signal Detect circuit on a separate circuit board. The postamplifier is ac coupled to the preamplifier as illustrated in Figure 5. The coupling capacitor is large enough to pass the SONET/SDH test pattern at the rated speed without significant distortion or performance penalty. If a lower signal rate, or a code which has significantly more low frequency content is used, sensitivity, jitter and pulse distortion could be degraded.

Figure 5 schematically shows a filter network that limits the bandwidth of the preamp output signal. The filter is designed to bandlimit the preamp output noise and thus improve the receiver sensitivity.

These components will also reduce the sensitivity of the receiver as the signal bit rate is increased above the rated speed.



*** Bracketed numbers represent 2 x 9 pin numbering**

Figure 5. Simplified Receiver Schematic

Electrical Characteristics

Supply Voltage

The receiver module operates from a positive supply in the range +3.1 V to +3.6 V.

Noise Immunity

The receiver includes internal circuit components to filter power supply noise. The results are shown in Figure 6 for +3.3 V at +25°C without power supply filtering present. However, good power supply filtering is required for optimum receiver performance. It is recommended that the filter network illustrated in Figure 7 is used to further improve device performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Power Supply Filtering

The LC filtering technique illustrated in Figure 7 provides power supply noise immunity of >100 mV pk-pk, over a frequency range of 10 Hz to 1 MHz, before a receiver sensitivity penalty of 1.0 dB occurs.

Receiver Signal Input

The transceiver module receiver will function with up to 72 consecutive 1's or 0's within the PRBS pattern of the optical input signal as specified by CCITT G.957 (ITU) for STM-1.

Receiver Data Output

The Data and $\overline{\text{Data}}$ output voltage levels conform to LVPECL standard levels (10 kH). Single-ended operation is not recommended as data sheet specifications can only be guaranteed when both differential outputs are used.

The Signal Detect Circuit

The Signal Detect circuit works by sensing the peak level of the received signal and comparing this level to a reference. The

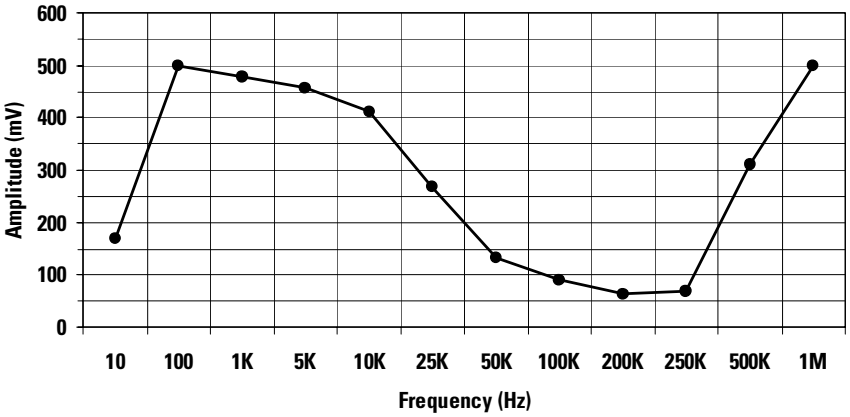


Figure 6. HFCT-5805/HFCT-5801 Receiver Injected Power Supply Noise Amplitude versus Frequency without Power Supply Filtering, for a 1 dB sensitivity penalty

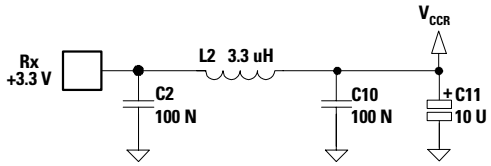


Figure 7. Recommended Receiver Power Supply Filtering

Signal Detect output of the receiver is LVPECL logic and must be terminated. The Signal Detect circuit is much slower than the data path, so the ac noise generated by an asymmetrical load is negligible. Power consumption may be reduced by using a higher than normal load impedance for the Signal Detect output as transmission line effects are not generally a problem with the switching rate being slow.

Termination Schemes for 155 Mb/s +3.3 V Transceivers

Standard PECL Voltage Levels

Agilent's serial data transceivers rely on Positive Emitter Coupled Logic for a high-speed interface. The PECL voltage levels shown in Figure 8 are measured with respect to the positive power supply. For measurement with respect to ground, these values would be subtracted from V_{CC}. For example, $V_{DC_{BIAS}}$ measured with respect to ground with a V_{CC} of +3.3 V would be 3.3 V – 1.3 V = 2 V. Figure 8 shows the minimum and maximum PECL levels for both input and output signals per the popular 100 K series of ECL logic. These voltage levels and the dc bias voltage will be referred to as Standard PECL. Note that Nonstandard PECL typically has a significantly different dc bias voltage but retains the standard peak-to-peak voltage swing of Standard PECL. The onset of +3.3 V products has resulted in the acronym of LVPECL meaning +3.3 V PECL.

There are several required design criteria that can be readily seen in the PECL levels of Figure 8. One requirement is that the dc voltage bias be V_{CC} -1.3 V at the input and output of Standard PECL. Another requirement is that the worst-case output voltage levels cannot allow the output transistor to enter cutoff mode. By definition, the output transistor of ECL gates must conduct current during the entire peak-to-peak voltage. It will be emphasized that the cutoff mode is possible with the cumulative effects of a lower than expected $V_{OL_{MIN}}$ and a marginal power supply.

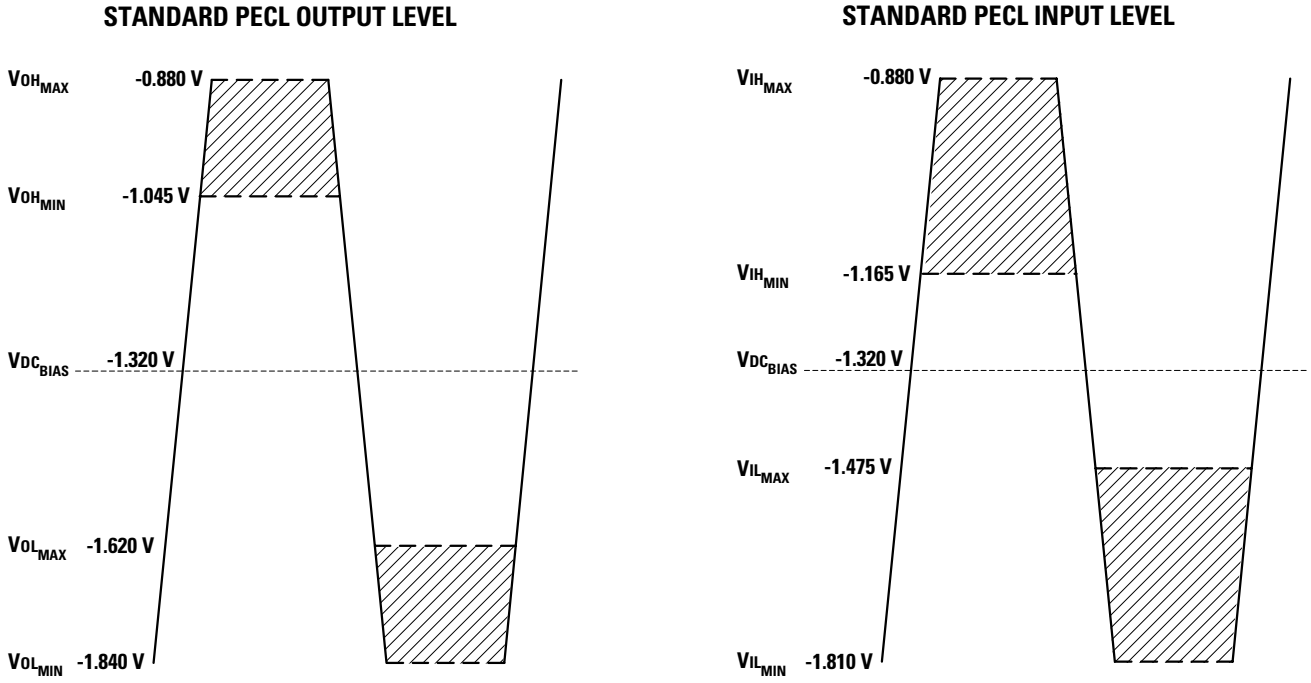


Figure 8. Standard PECL Input, Output Levels

Thevenin Equivalent of Standard PECL Terminations

The Thevenin equivalent for any Standard PECL termination scheme should match one of the two termination schemes shown in Figure 9. All PECL termination circuits strive to match an ideal 50 Ω termination with an ideal 50 Ω transmission line to prevent unwanted reflections. The 50 Ω termination resistor is mounted as close to the PECL input as possible. In addition, standard PECL terminations ensure the correct dc bias voltage of V_{CC} -1.3 V. In some cases, designers may prefer the dc isolation of the ac coupling capacitor shown in Figure 9 (b). In the case of mixing Standard with Nonstandard PECL, the ac coupling capacitor would be required. This is due to Nonstandard PECL having a dc bias voltage significantly different from V_{CC} -1.3 V. A potential pitfall when using ac coupling capacitors is that significant distortion could be introduced in a 125 Mb FDDI interface or any other interface that must meet the FDDI standard. This distortion is caused by the FDDI DDJ pattern and it's 50 KHz base- line wander effect described in the FDDI PMD standard, see Note 1 below.

In Figure 9 only partial internal schematics of a PECL gate are shown to emphasize a specific point. Also, only one side of the differential I/O pair is shown. There is an array of technical material readily available that exhaustively describes the remaining ECL/PECL circuit. The LVPECL Output Driver in Figure 9 (a) shows only the open-emitter output driver. This is to emphasize that all Standard PECL will set up a dc bias level of V_{CC} - 1.3 V at the output after termination. Also in Figure 9 (a), the LVPECL Input shows one transistor of the emitter-coupled pair. This is to emphasize that PECL has a high input impedance. The standard 50 Ω termination voltage of V_{CC} - 2 V is determined by two major requirements. The first is to reduce power consumption as much as possible by reducing the voltage drop across the 50 Ω termination resistor. The second requirement is to minimize any chance that the output driver would not enter a cutoff mode under worst case PECL levels. The culmination of all these requirements resulted in the Standard PECL termination, or Thevenin equivalent of 50 Ω into a termination voltage of V_{CC} - 2 V with a dc bias voltage of V_{CC} - 1.3 V. For dc coupled Standard PECL terminations, the Thevenin equivalent of any termination scheme should match Figure 9 (a).

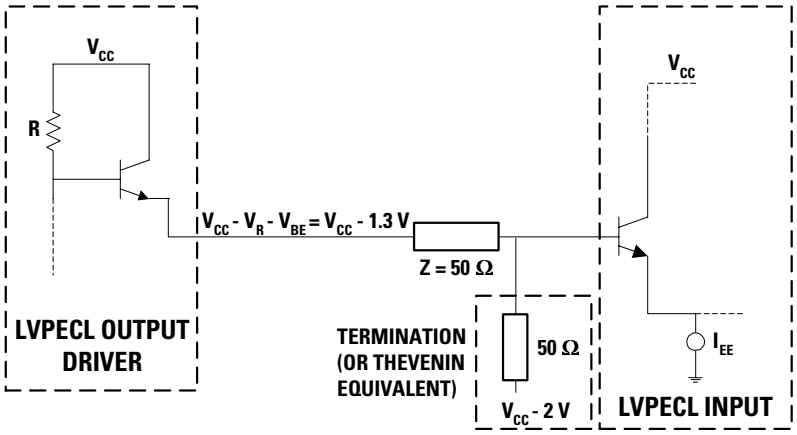
Note: 1 FDDI PMD Token Ring Physical Layer Medium Dependent (PMD) standard is ISO/IEC 93 14-3: I990 and ANSI X3.166-1990 American National Standard

For various reasons, some interface designers may prefer ac coupled LVPECL terminations. Figure 9 (b) shows that the addition of an ac coupling capacitor isolates the PECL input and output circuits and changes the Thevenin equivalent circuit. The LVPECL open emitter transistor requires a path to ground so a 130 Ω resistor is added to sink about 15 mA. At the PECL input there is no current flow through the ac coupling capacitor or through the input of the high impedance emitter follower. So, there is no dc current flow in this branch and the termination voltage of V_{CC} -1.3 V becomes the common dc voltage in this entire circuit branch. We know from Figure 8 that Standard PECL levels expect a dc bias of -1.3 V with respect to V_{CC}. Consequently, the termination voltage must be V_{CC} - 1.3 V. For Standard PECL with an ac coupling capacitor, the Thevenin equivalent of any termination scheme should match Figure 9 (b).

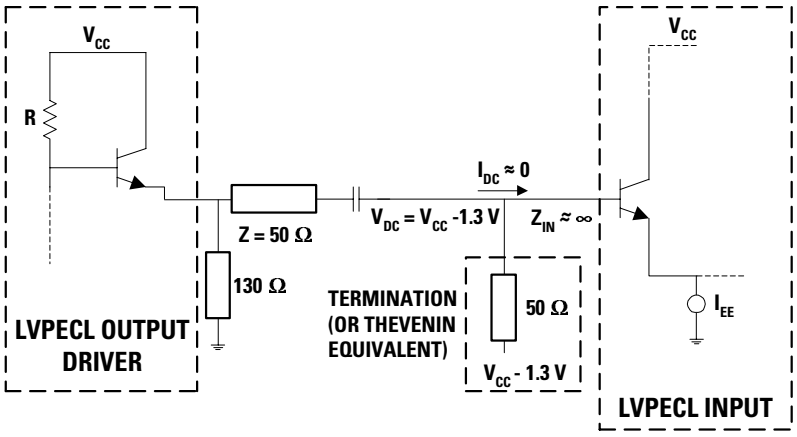
Note that there are interface ICs that have Nonstandard LVPECL levels and require ac coupling in order to interface with Standard LVPECL. In these cases, Standard LVPECL termination can be used on one side of the ac coupling capacitor and the supplier recommended Nonstandard LVPECL termination on the other side.

Recommended LVPECL Terminations

Two termination schemes are presented in this section. Figures 10 and 11 are recommended terminations and, the trade-offs of circuit complexity and reliability will have to be decided by each designer. Both termination schemes assume that the fiber optic transceiver and interface ICs require a power supply voltage of +3.3 V. In addition, both termination schemes are the Thevenin equivalent of Figure 9 (a). Note that wide design latitude can be given to the Signal Detect (SD) LVPECL termination as the assert and deassert times are in microseconds. One recommended termination that has a Thevenin equivalent of 50 ohm to V_{CC} -2 V, is shown in Figure 11.



(a) 'STANDARD LVPECL' TERMINATION, DC COUPLED



(b) 'STANDARD LVPECL' TERMINATION, AC COUPLED

Figure 9. 'Standard LVPECL' Terminations

Figure 10 shows one termination scheme that is widely used with +3.3 V transceivers. This recommendation requires that both input and output devices use Standard LVPECL. The 130 Ω resistor sinking about 15 mA of dc current at the output of the open emitter transistor is typical of LVPECL outputs. The 100 Ω resistor across the differential inputs is equivalent to two of the Thevenin equivalent circuits shown in Figure 9 (b), that is, two sets of 50 Ω resistors and termination voltages terminated to V_{CC} -1.3 V.

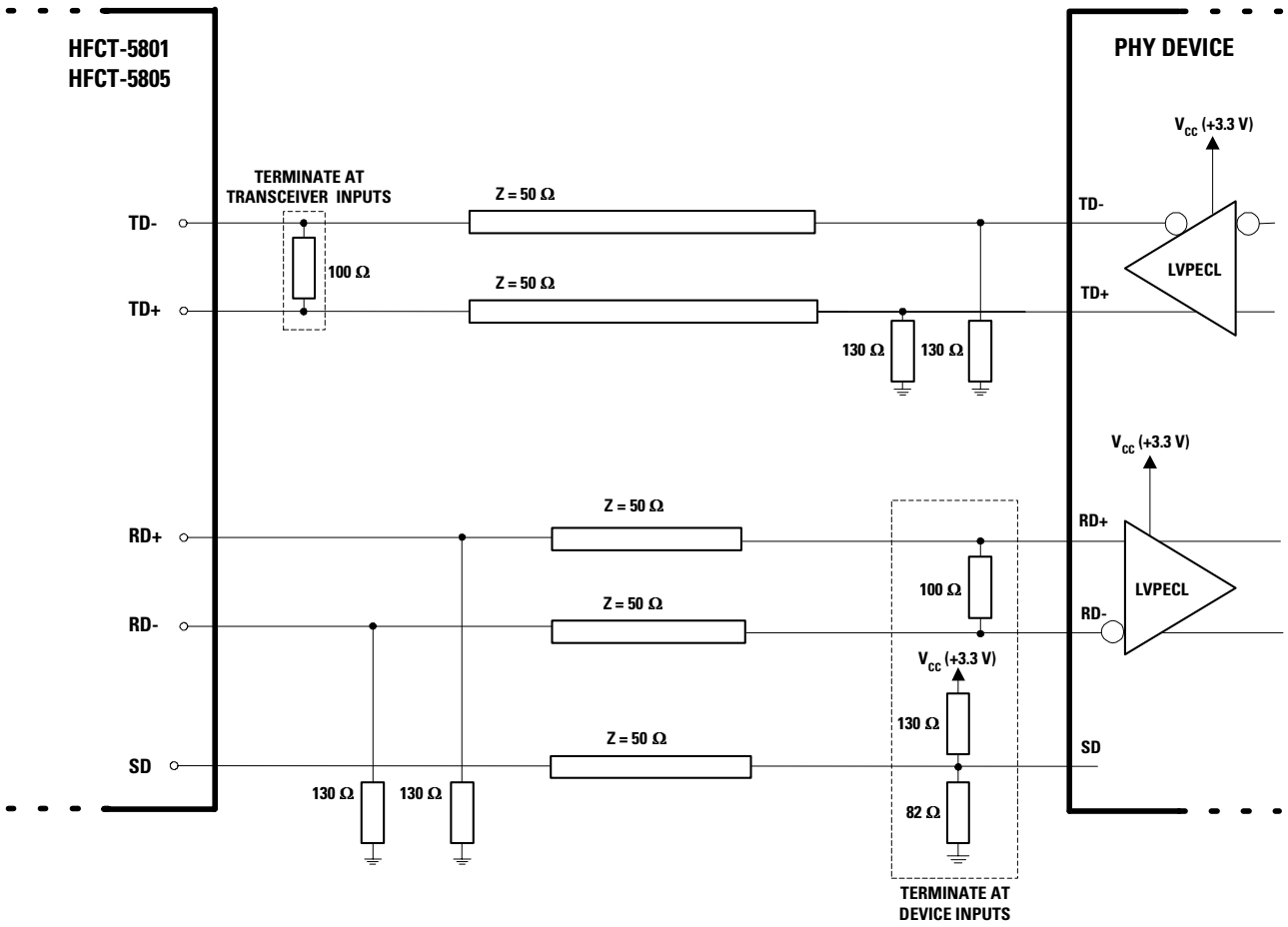


Figure 10. LVPECL Optical Transceiver Interface: Standard LVPECL to Standard LVPECL

Many interface designers may be familiar with the termination scheme in Figure 11. This termination circuit was recommended on the widely used Agilent 1 x 9 SC Duplex 125 Mb/155 Mb multimode fiber optic transceiver. This termination scheme, sometimes referred to as a split load or parallel termination, uses one more resistor than the previous set up and may have some worthwhile advantages as determined by the interface designer. Referring to the worst case voltage levels in Figure 8 and the termination voltage in Figure 9 (a), there is an extreme case where the cumulative effects of a lower than expected $V_{OL_{MIN}}$ and a higher than expected V_{CC} would cause the LVPECL open emitter output transistor to enter cutoff mode. This would occur when $V_{OL_{MIN}}$ falls below the termination voltage of V_{CC} -2 V resulting in no positive current flow across the 50 ohm termination resistor. Some designers may prefer extra margin to ensure that this extreme case does not occur. The termination scheme of Figure 11 allows $V_{OL_{MIN}}$ to be less susceptible to a non-optimal V_{CC}. From the Thevenin equivalent, the termination voltage is V_{CC} -2 V. Intuitively, it can be seen from Figure 11 that any change in termination voltage of V_{CC} -2 V is a ratio of the change in V_{CC}, that is, $\Delta V_{TERMINATION} = (82/[82+130]) \Delta V_{CC} = 0.4 \Delta V_{CC}$. So, a -5 percent change in V_{CC} would cause a -2 percent change in $V_{TERMINATION}$. Since the termination voltage is less susceptible to changes in power supply voltage, there is increased margin for $V_{OL_{MIN}}$. Another advantage of this termination scheme is that the dc bias current flows in the termination resistors only, reducing the power dissipated by the IC and increasing its reliability.

Adequate decoupling to the supply rails must be provided as close to the termination resistors as possible. Care must be taken to choose a large enough capacitor to give the required low frequency cutoff. The frequency is defined as $1/2 \pi RC(Hz)$ where R is the termination resistor. The low frequency cutoff should be set to approximately a factor of 10 below the lowest frequency content of the transmitted signal. A 0.1 µF capacitor is recommended.

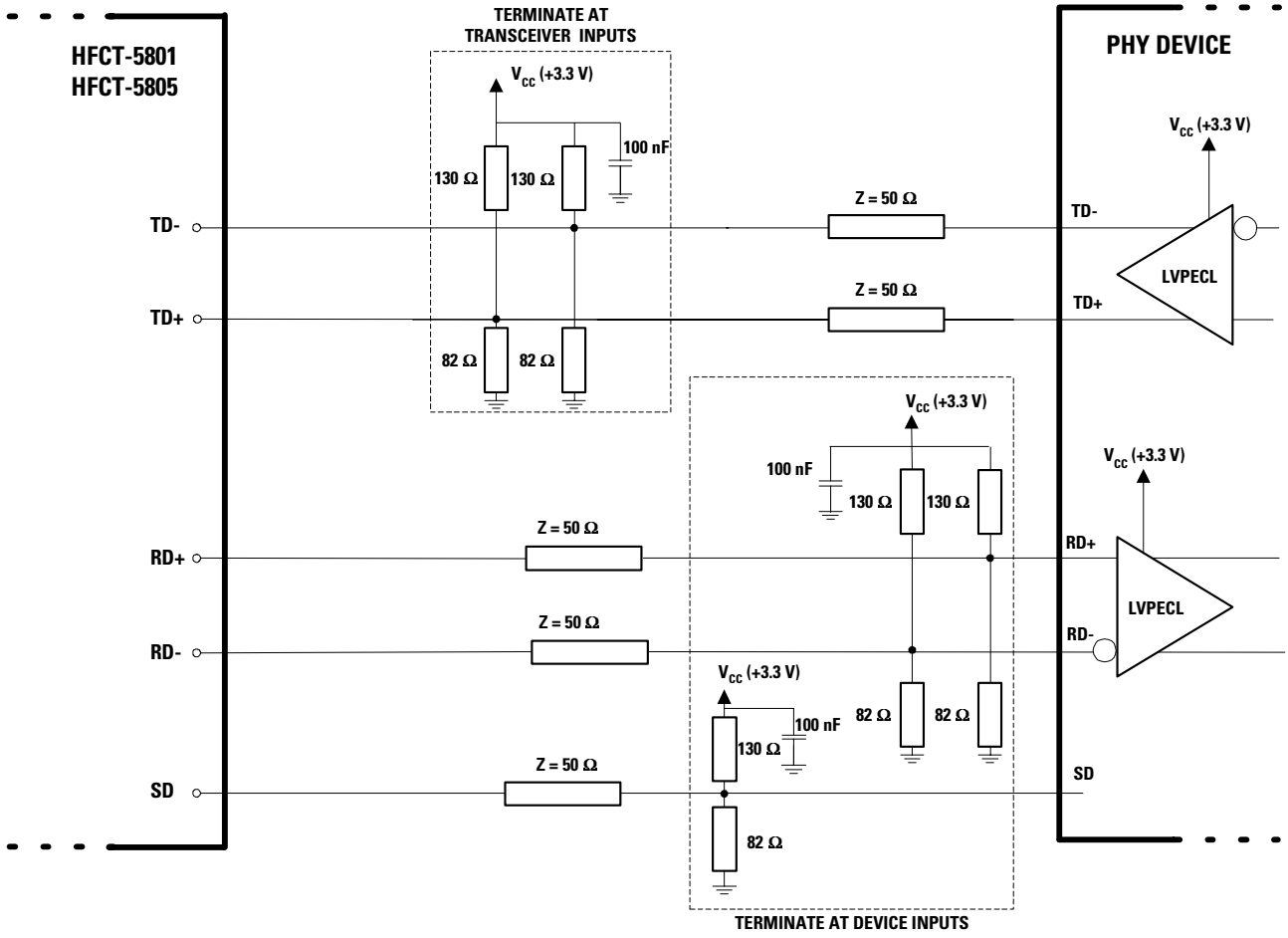


Figure 11. Alternative LVPECL Optical Transceiver Interface: Standard LVPECL to Standard LVPECL

Alternative PECL Terminations

There are many other versions of PECL terminations possible especially when considering the mixing of Nonstandard and Standard PECL. For this reason, only two other termination schemes will be presented. The first is a PECL interface from LVPECL to +5 V PECL. The second PECL termination scheme is shown in Figure 14 for the HFCT-5800 evaluation board.

Figure 12 summarizes the interface between a 3.3 V optical transceiver and a +5 V physical layer IC. On the 3.3 V optical transceiver side of the ac coupling capacitor, the split load terminations shown were discussed previously. On the +5 V Interface IC side, the split load resistor values are adjusted for +5 V but are still the Thevenin equivalent of Figure 9 (b). The output of the +5 V PECL IC is given as 330 Ω, resulting in an output current of about 11 mA.

Figure 12 also shows that the Signal Detect (SD) output requires a level translator when interfacing LVPECL to PECL. Since SD is a near static voltage level, ac coupling cannot be used. To increase the output level from LVPECL to PECL, a voltage level translator circuit is required.

Layout

Due to the relatively high frequencies and low noise levels involved, it is important that good RF techniques are used for the PCB layout. The use of ground planes and 50 ohm transmission line interconnects is required for the LVPECL outputs.

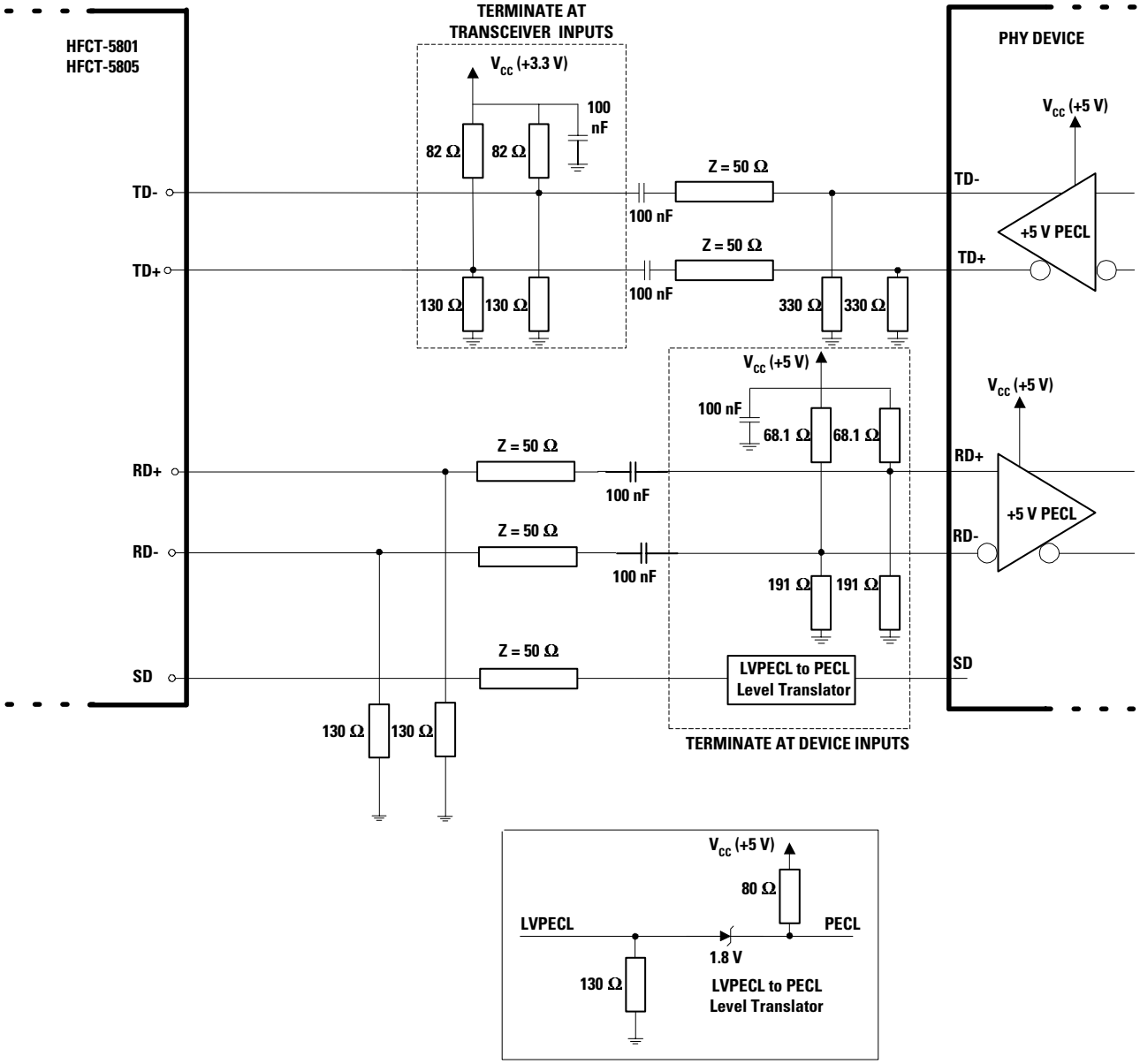


Figure 12. Optical Transceiver Interface: LVPECL to +5 V PECL, ac Coupled

Evaluation Board and Pin Out Designations (Part No. HFCT-5800)

Agilent can supply an evaluation board, as shown in Figure 13, to provide power and interface connections to the devices listed in Table 1.

The evaluation board operates at +3.3 V bias. On the evaluation board, SMA connections are provided for differential LVPECL interfacing. The required termination resistors are provided.

For products with a 2 x 9 pinout the transmitter is normally enabled if no connection is made to the disable pin 7. With no connection, the disable input is internally pulled to V_{EE} with a 16 kΩ resistor. The disable switch on the evaluation board will connect pin 7 to V_{CC} to disable the module when in position (1) indicated on the switch.

Figure 14 shows the HFCT-5800 Evaluation Board Schematic layout. Table 2 gives the modules pin out, functionality and connection information.

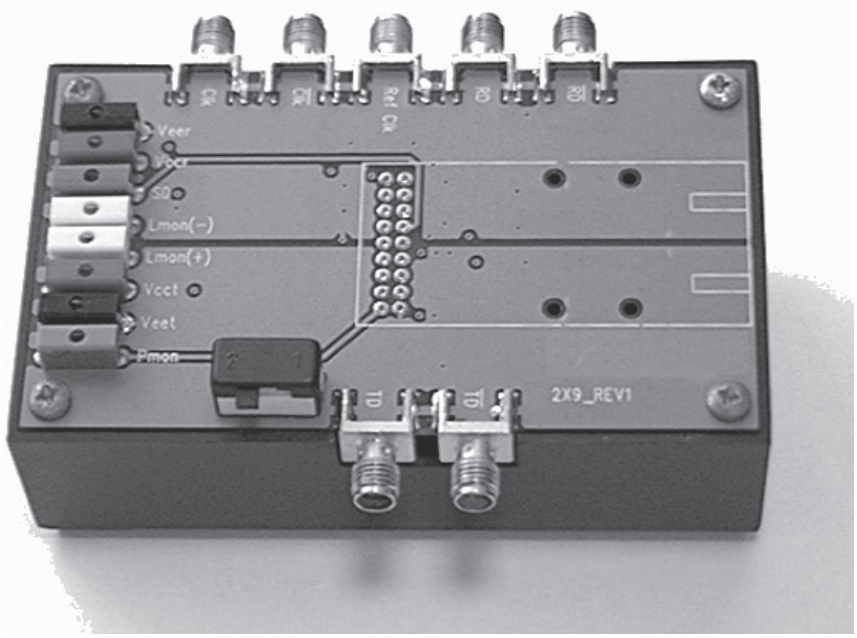


Figure 13. HFCT-5800 Evaluation Board

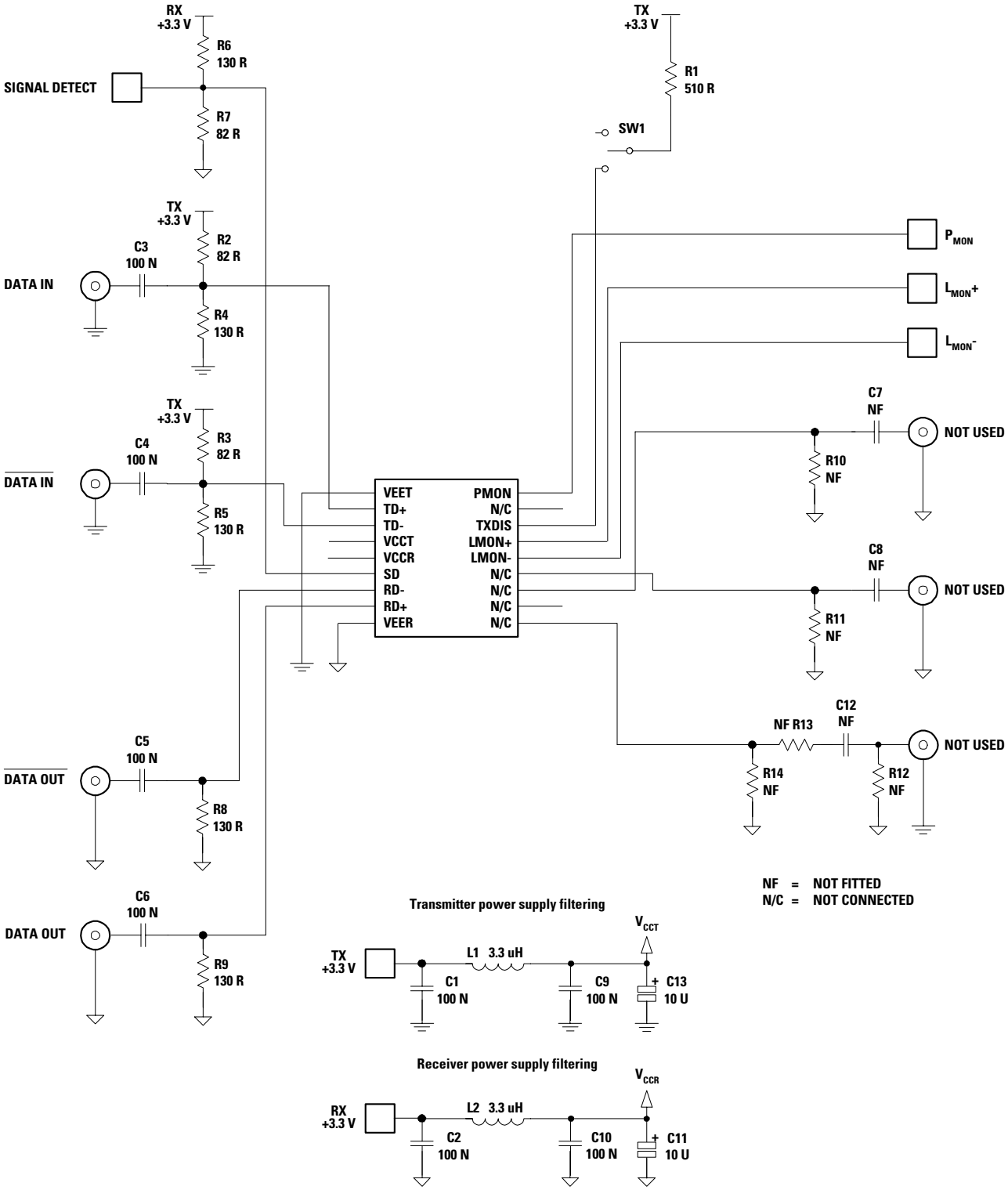


Figure 14. HFCT-5800 Evaluation Board Schematic

Table 2. Pin Out Table (Refer to Figure 11)

Pin Out			
1 x 9	**2 x 9***	**Symbol**	**Functional Description**
NP	1	N/C	Not Connected
NP	2	N/C	Not Connected
NP	3	N/C	Not Connected
NP	4	N/C	Not Connected
NP	5	$L_{MON}(-)$	Laser Bias Monitor (-) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
NP	6	$L_{MON}(+)$	Laser Bias Monitor (+) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
NP	7	Tx_{DIS}	Transmitter Disable at +3.3 V Supply Transmitter Output Disabled : 2.0 V $\leq V_7 \leq V_{CCT}$ Transmitter Output Uncertain: 1.175 V $\leq V_7 \leq$ 2.0 V. Transmitter Output Enabled: $V_{EET} \leq V_7 \leq$ 1.175 V or open circuit.
NP	8	N/C	Not Connected
NP	9	P_{MON}	Power Monitor The analog voltage measured at this high impedance output provides an indication of whether the optical power output of the Laser Diode is operating within the normal specified power output range per the following relationships: High Light Indication: $V_9 \geq$ 1.78 V. Normal Operation: $V_9 \cong$ 1.28 V. Low Light Indication: $V_9 \leq$ 0.78 V.
9	10	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.
8	11	TD	Transmitter Data In Terminate this high-speed, differential Transmitter Data input with standard LVPECL techniques at the transmitter input pin.
7	12	$\overline{TD}$	Transmitter Data In Bar Terminate this high-speed, differential Transmitter Data input with standard LVPECL techniques at the transmitter input pin.
6	13	V_{CCT}	Transmitter Power Supply Provide +3.3 V dc via the recommended power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
5	14	V_{CCR}	Receiver Power Supply Provide +3.3 V dc via the recommended power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
4	15	SD	Signal Detect Normal input optical levels to the receiver result in a logic "1" output. Low input optical levels to the receiver result in a fault indication shown by a logic "0" output. SD is a single-ended, LVPECL output and may be terminated as in Figure 11. The SD output can be used to drive a LVPECL input on an upstream circuit, such as, SD input, Loss of Signal-bar input. SD can be used as a low-power LVPECL output by completing the interconnection of SD output with other LVPECL inputs. If SD output is not used, leave it open-circuit.

NP = Not present
* 2 x 9 = HFCT-5801A/B/C/D

Table 2. Pin Out Table (continued)

Pin Out		Symbol	Functional Description
1 x 9	2 x 9*		
2	16	$\overline{RD}$	Re-timed Receiver Data Out Bar Terminate this high-speed, differential, LVPECL output with standard techniques at the follow-on device input pin.
3	17	RD	Re-timed Receiver Data Out Terminate this high-speed, differential, LVPECL output with standard techniques at the follow-on device input pin.
1	18	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
Mounting Studs			The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the non-conductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.

* 2 x 9 = HFCT-5801A/B/C/D

Cleaning of Optical Subassemblies

Solvents should not be used to clean the transmitter optical subassembly (TOSA) or receiver optical subassembly (ROSA).

The TOSA connector interface is a single-mode physical contact, the ROSA is a nonphysical contact and in both cases cleanliness is extremely important.

It is recommended that an NTT international 'Cletop Stick-Type' cleaner , or similar lint-free swab is used for quick cleaning of the ferrule endface and SC ports. Using a dry 'Cletop Stick' every time, insert into SC port and rotate and remove.

Regulatory Compliance
These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various regulations governing Certification of Information Technology Equipment as specified in the product data sheet.

Electromagnetic Interference (EMI)
Most equipment designs utilizing these high-speed transceivers from Agilent will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

All transceiver products have been characterized without a chassis enclosure to demonstrate the robustness of the part's integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity
Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well-designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Table 3. Regulatory Compliance - Typical Performance

Feature	Test Method	Performance
Electromagnetic Interference (EMI) HFCT-5805 and HFCT-5801	FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Typically provide greater than 11 dB margin below 1 GHz to FCC Class B when tested in a GTEM with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz dependent on customer board and chassis designs.
Immunity HFCT-5805 and HFCT-5801	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 27 MHz to 1 GHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
Eye Safety	FDA CDRH 21-CFR 1040 Class 1 IEC60825-1 Amendment 2 2001 - 01	Accession Number: 9521220-36 License Number: 933/510031/03

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