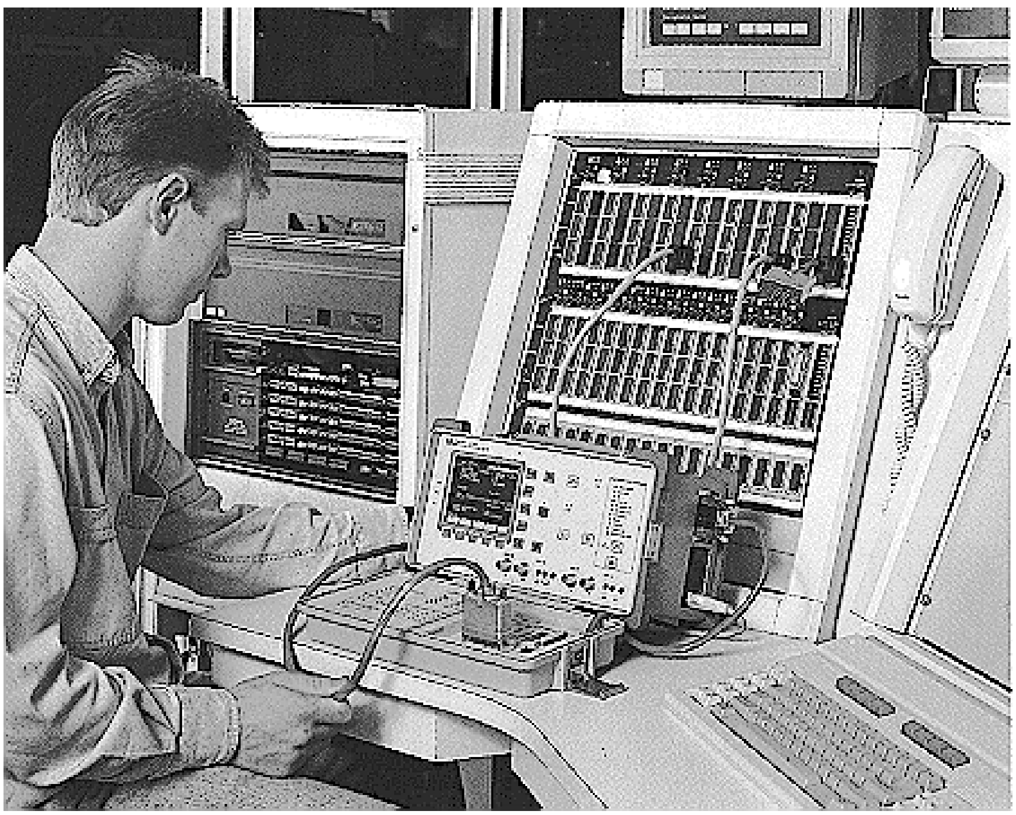
HEWLETT PACKARD

Maximizing revenue with in-service testing – introduction

Application note 1237-1



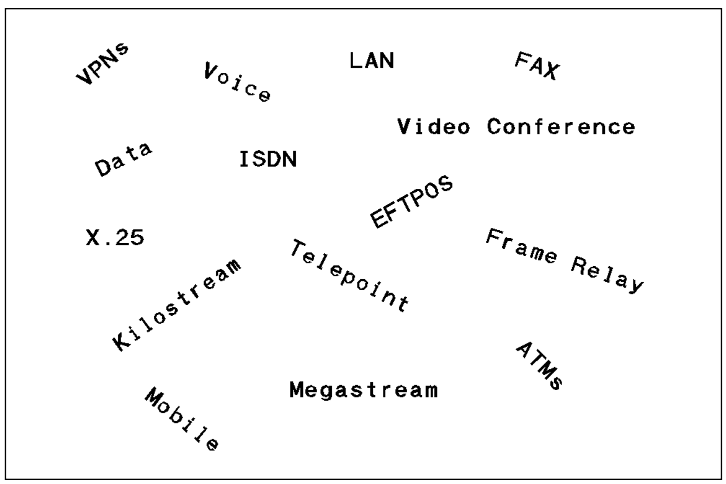
This is the first booklet in a series of Application Notes dealing with Maximizing Revenue with In-service Testing. It is intended to provide background information for use when referring to the other booklets.

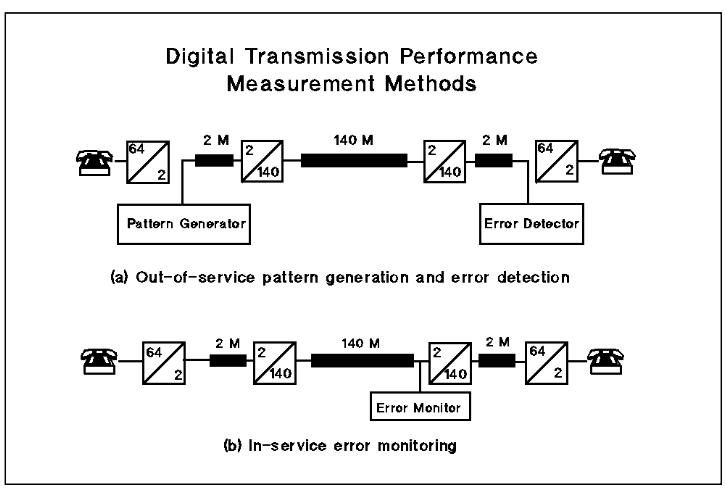
Contents

Introduction

In recent years, there has been a dramatic expansion in the number and variety of services carried via digital communication networks. For an additional cost, customers are now prepared to lease lines of a guaranteed transmission quality and availability. This means that PTTs must analyze more frequently a link's performance, but at the same time minimize downtime.
Traditionally, error performance tests meant taking the link out of service for extended periods of time which, as well as being wasteful of capacity, lost the network operator valuable revenue.

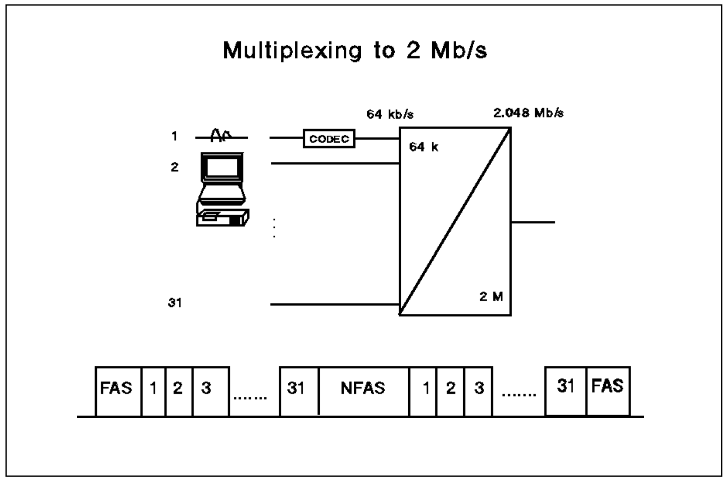
In today's world of privatized and more profit-orientated PTTs, the emphasis is on maximizing capacity and minimizing downtime due to faults. A preventative maintenance strategy based on in-service monitoring provides the solution to both of these problems.





European digital transmission hierarchy

The European digital transmission hierarchy is based around the primary data rate of 2 Mb/s. The 2 Mb/s frame structure is defined in CCITT recommendations G.704 and G.706. Each 2 Mb/s frame contains 32 timeslots, each of 8 bits, at a repetition rate of 8000 frames per second. The first of these 64 kb/s timeslots (TS0) is reserved for framing, error checking and alarm signals. The other 31 timeslots can be used for traffic (voice or data) although sometimes a timeslot (usually TS16) is reserved for signaling information. The start of the 32-timeslot frame is indicated by the frame alignment signal (FAS) in TS0 of alternate frames.



Sixteen frames are grouped together in a multiframe as shown above. TS0 in alternate frames contains the Frame Alignment Signal (FAS) as well as one of the Cyclic Redundancy Checksum (CRC4) bits. In frames not containing the FAS (ie, the NFAS), the first bit is used to transmit the CRC multiframe alignment signal which defines the start of the SMF. The 4-bit CRC check is calculated on all 2048 bits of the previous sub-multiframe (SMF) and is sent as C1, C2, C3 and C4. At the receiving end, the CRC remainder is calculated for each SMF and the result compared with the CRC4 bits received in the next SMF. This CRC check provides an indication of block errors within the 2 Mb/s signal on both directions of a link.

2 Mb/s CRC Structure

Multiframe	Sub-multiframe SMF	Frame Number	TS0 Bit 1 2 3 4 5 6 7 8	
I	I	0	CRC_1	FAS
		1	0	NFAS
		2	CRC_2	FAS
		3	0	NFAS
		4	CRC3	FAS
		5	1	NFAS
		6	CRC_4	FAS
		7	0	NFAS
	II	8	CRC_1	FAS
		9	1	NFAS
		10	CRC_2	FAS
		11	1	NFAS
		12	CRC_3	FAS
		13	E	NFAS
		14	CRC4	FAS
		15	E	NFAS

CRC = CRC4 bits   E = CRC Error bits   001011 = CRC Alignment Signal

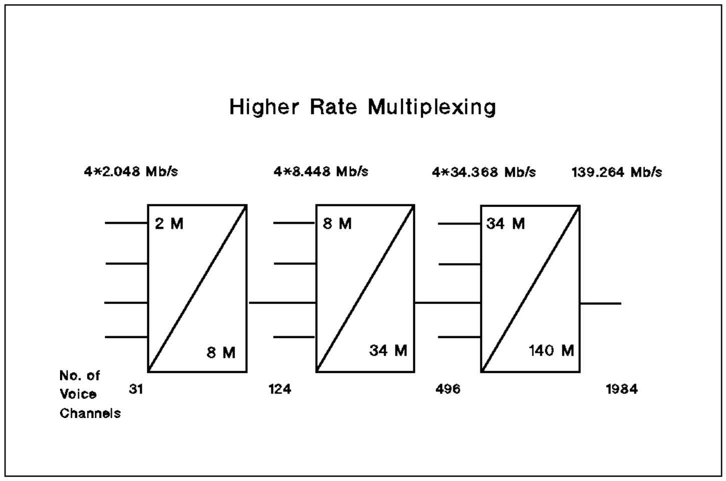
The E bits are used to indicate to the sending equipment that an error has been detected between the sent CRC and the CRC calculated at the receive end.

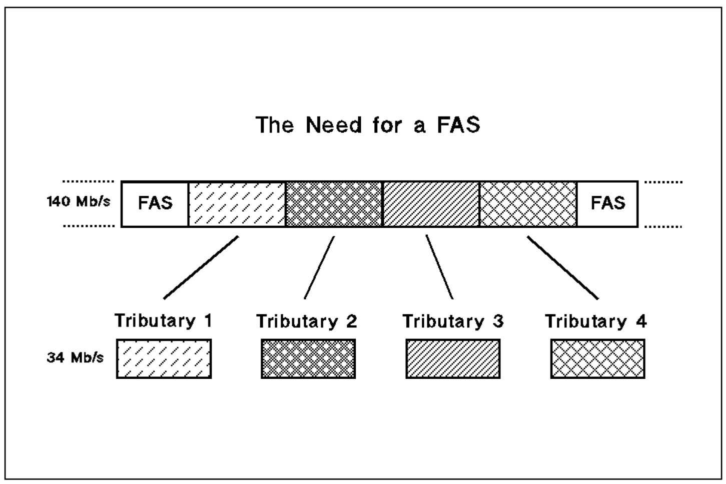
Higher rate multiplexing

At each of the higher transmission levels in the network, four lower rate tributaries are combined by Time Division Multiplexing (TDM) to produce one higher rate signal. This multiplexing process is used to transmit a large number of digital circuits over the same physical path. As an example, consider the fourth layer in the multiplexing structure where the 140 Mb/s signal contains 1984 individual 64 kb/s channels.

You may notice that at each stage when the four tributaries are combined, the resulting bit rate is slightly higher than four times the input bit rate – that is, 4 x 2048 kb/s = 8192 kb/s, but the actual rate is 8448 kb/s.

These extra bits are overhead, introduced as part of the multiplexing process. They are required for the following purposes; Framing Structure, Justification Process, Remote Alarm Information and Spare Bits.





Framing structure

A framing structure is required at each level in the digital hierarchy to enable demultiplexing equipment to extract or switch the lower rate tributaries. By synchronizing to this Frame Alignment Signal (FAS), the demultiplexer then knows the position of the bits carrying the tributary information.

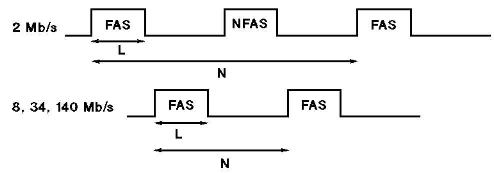
The criteria for frame alignment loss and recovery are laid down in CCITT recommendations G.704, G.732, G.742 and G.751, as shown in the table.

Frame Alignment Criteria

Bit Rate (Mb/s)	CCITT Standard	Frame Alignment	Frame Loss
2.048	G.704/732	FAS, NFAS, FAS (bit 2)	3 consecutive errored FAS
8.448	G.742	3 consecutive correct FAS	4 consecutive errored FAS
34.368	G.751	3 consecutive correct FAS	4 consecutive errored FAS
139.264	G.751	3 consecutive correct FAS	4 consecutive errored FAS

In the days when the network was only used to carry voice traffic, the chance of these framing patterns being imitated in consecutive frames was extremely low. Now customers also use the network for data containing repetitive patterns which can mimic the FAS and cause false frame alignment problems.

The Framing Structure

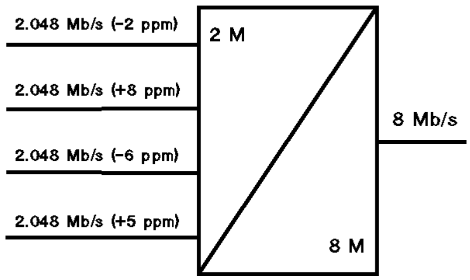


Bit Rate (kb/s)	L (bits)	N (bits)	Fas Bit Rate (kb/s)
2048	7	512	28
8448	10	848	99.6
34368	10	1536	223.7
139264	12	2928	570.7

FAS = Frame Alignment Signal
NFAS = Non Frame Alignment Signal (2M only)

At each rate the FAS is a fixed sequence of L bits which repeats every N transmitted bits. By taking the ratio of L/N, relative to the bit rate, it is possible to calculate the FAS bit rate at each level. This is the rate at which this fixed, known sequence is transmitted within the overall bit stream and is the bandwidth available for in-service error testing. Since the FAS consists of a fixed repetitive sequence, it is possible to detect, in-service, any bit errors affecting it.

The Need for Justification



Justification process

The second source of the extra bits added during the multiplexing stage is the justification or “bit stuffing” process. As mentioned previously, each stage in the multiplexing hierarchy combines four lower-rate tributaries by Time Division Multiplexing (TDM) and generates one higher-rate bit stream. The TDM process relies upon receiving four equal input bit rates before combining them, in a bit-interleaved fashion, into a higher rate signal. In practice, this creates additional complications within the network. Each of these four tributaries may originate from a different piece of equipment, with a different timing source, and hence may have small bit rate fluctuations with respect to each other.

The tolerance on bit rate at equipment interfaces, according to CCITT recommendation G.703, is given as parts per million offsets from the standard rates. All multiplexing equipment must therefore be able to deal with inputs which differ with respect to each other, up to and beyond the rates shown in the table.

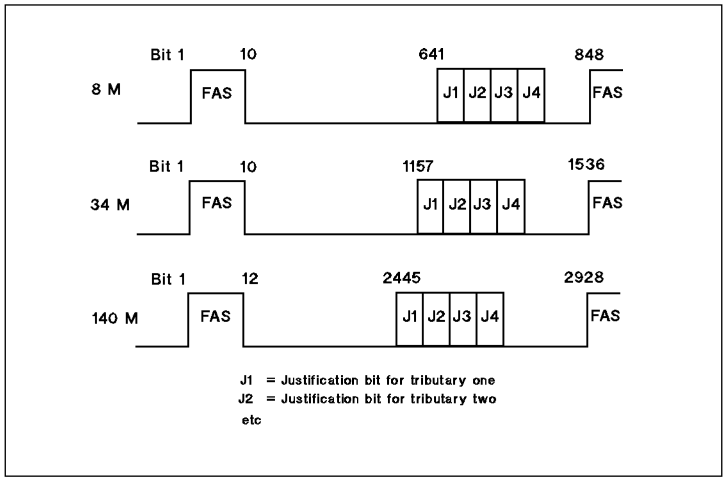
CCITT line rate tolerance

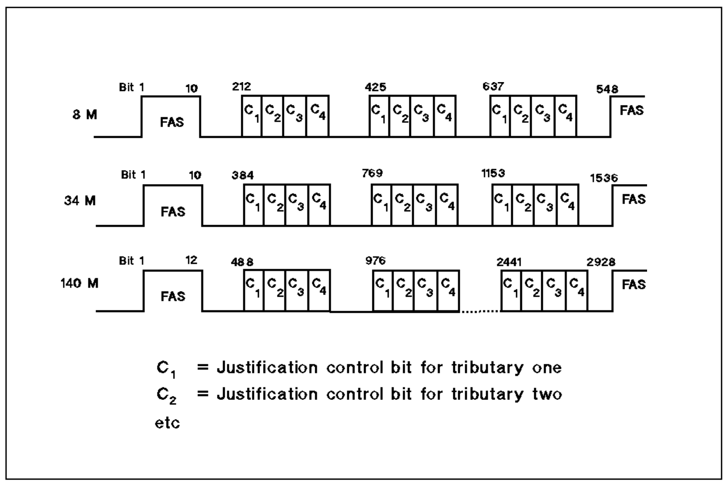
2.048 Mb/s	**± 50 ppm**
8.448 Mb/s	**± 30 ppm**
34.368 Mb/s	**± 20 ppm**
139.264 Mb/s	**± 15 ppm**

This problem is dealt with by adding justification (or stuffed) bits into each input tributary and bringing them all to a slightly higher, but equal, bit rate. Only then does the TDM take place. Within each higher rate signal, there are four opportunities per frame (one per tributary) to insert a stuffed bit. This is called positive justification.

If the opportunity to insert a justification bit into a particular tributary is taken, then the demultiplexing equipment must be made aware of when this has happened and, as part of the reverse process, remove the "stuffed bits" (de-justification).

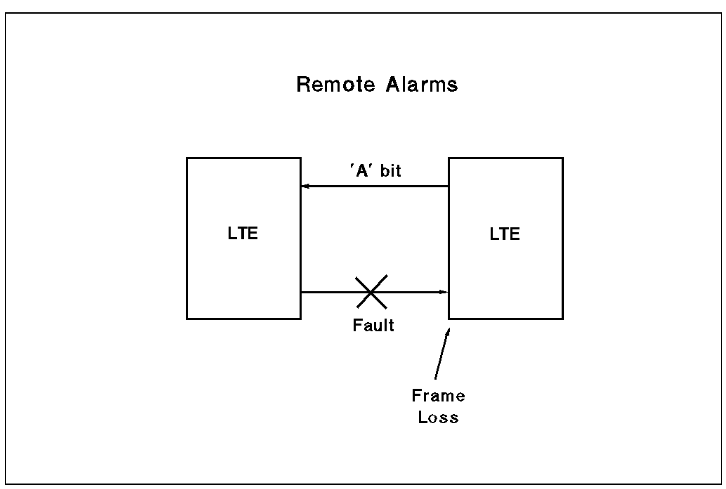
Justification control bits within each frame indicate whether the justification (stuffed) bit for the corresponding tributary has been inserted or not. To minimize the effect of bit errors on the justification control bits, they are repeated three times throughout the frame (five at 140 Mb/s) and at the demultiplexer they vote on a majority basis (2 out of 3, or 3 out of 5) as to whether the stuffed bit has been inserted (1 = yes, 0 = no).



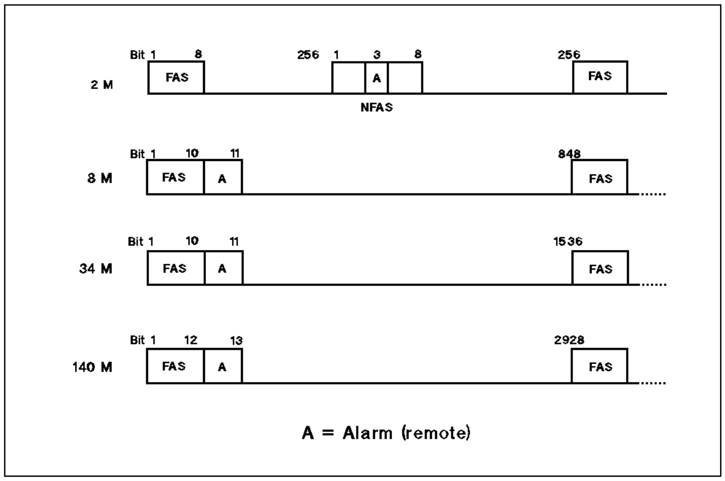


Remote alarm information

The third category of extra overhead bits is Remote Alarm Information. Within each of the frame structures one bit is allocated on the return path to indicate to sending equipment that a fault exists on the downstream path.

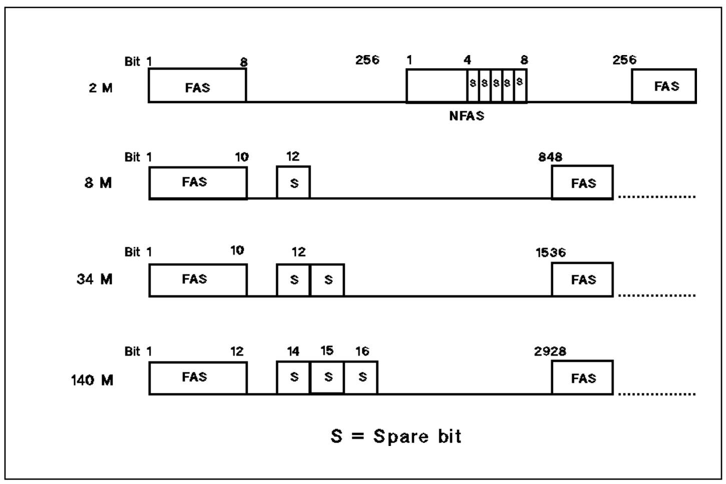


The position of the Alarm (A) bit is immediately following the FAS at 8 to 140 Mb/s, and at 2 Mb/s it occupies bit 3 of the NFAS signal.



S bits

The final category of additional overhead bits are the “spare” or S bits. In each of the frame structures, certain positions are left to be used as required by individual PTTs for parity checking schemes, etc.



Summary

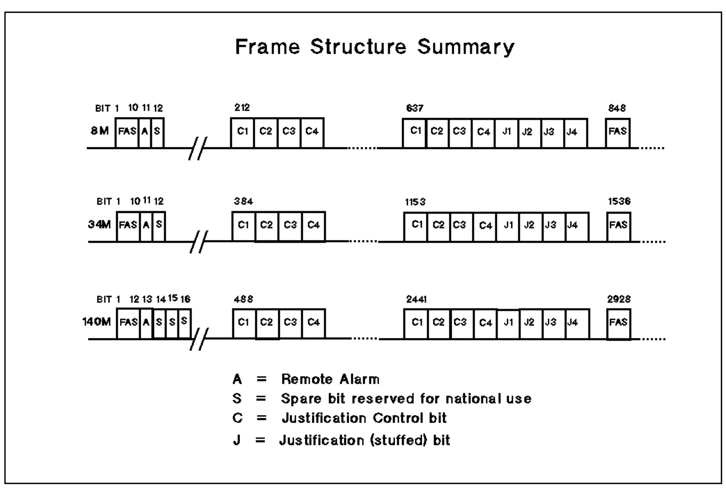
Having dealt with all the components of the overhead at each rate, we now look at the final frame structure at each level. At each stage, it consists of the four tributaries combined from the lower level plus some overhead bits. The overhead bits consist of:

1. The FAS – for frame synchronization.

2. Justification bits – to cope with slight variations in tributary input bit rate. Justification control bits – to indicate the presence of a justification bit.

3. Remote alarm – to indicate a downstream fault to sending equipment.

4. Spare bits – for use as required by individual PTTs.



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