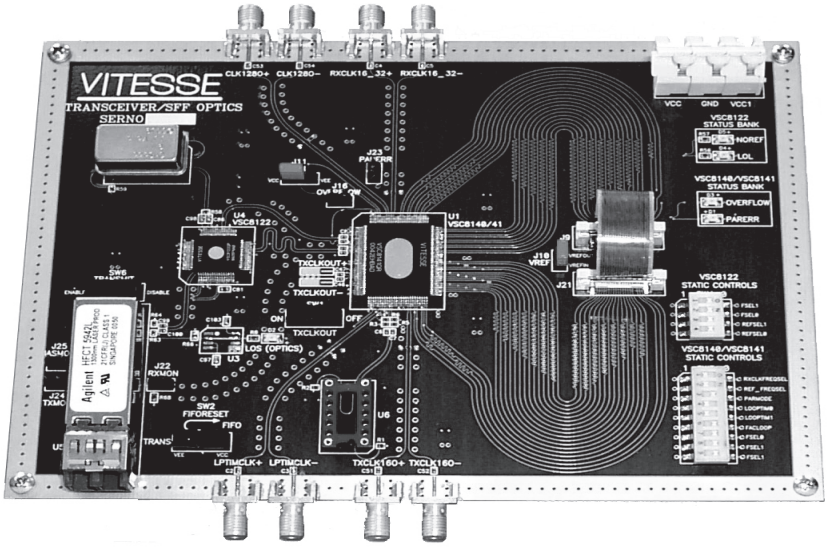
OC-48 Agilent Small Form Factor Transceiver HFCT-5942 with Vitesse VSC8122 and VSC8141 Multi-rate Chip Set Reference Design

Application Note 1247



Evaluation Board Introduction

The purpose of the Multi-rate Small Form Factor (SFF) evaluation board is to demonstrate interoperability between Vitesse IC's VSC8122 (CDR), VSC8141 (Serdes) and Agilent SFF transceivers HFCT-5942. The board requires only an external +3.3 V supply to operate. It allows the user to connect to the optics module for interoperability testing or to characterize equipment for jitter and Tx eye mask evaluations.

Description

Components on this evaluation board include:

the Vitesse VSC8122, a multi-rate clock and data recovery IC capable of OC-3/12/48 SONET or Gigabit Ethernet rates.

the Vitesse VSC8141, a multi-rate 16-bit serializer/deserializer capable of OC-3/12/48 rates. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards.

the Agilent HFCT-5942, a OC-48 optical transmitter and receiver contained within a new industry standard 2 x 10 DIL style package, with LC fiber connector interfaces. The transceiver performs all light-to-logic and logic-to-light functions in conformance with SONET/SDH transmission standards.

For more information on these components reference should be made to the Agilent HFCT-5942, Vitesse VSC8122 and VSC8141 Data Sheets.

Agilent Technologies

Switch Settings

- SW1: TXCLKOUT
Disables/Enables the TXCLKOUT signal from the VSC8141

- SW2: FIFORESET
Used for resetting the FIFO within the 16-Bit Transceiver in the event of an overflow condition.

- SW3: SC8140/VSC8141
Static controls

RXCLKFREQSEL
Sets the rate of the RXCLK16_32 clock output that is available via SMA connections.
= 1 for /16 of the line rate clock
= 0 for /32 of the line rate clock

REF_FREQSEL
Selects the reference clock frequency that the transceiver will accept
= 1 for /16 of the line rate clock
= 0 for /32 of the line rate clock

PARMODE
Systems employing internal parity are supported by the VSC8140/VSC8141. On the transmit side, a parity check is performed between the TXPARITYIN input and the 16 TXIN [15:0] bits. PARMODE is used to select even or odd parity expected for these 17 bits. (TXIN[15:0] and TXPARITYIN).
PARMODE = "0" selects odd,
PARMODE = "1" selects even.
The PARERR output (parity error output) is asserted active high when the parity of the 17 bits (TXIN[15:0] and TXPARITYIN) does not conform to the expected parity designated by PARMODE. PARERR becomes available after the rising edge of TXCLK16I at test point J23.

LOOPTIM0
PLL bypass control.
= 1 to bypass the internal PLL and time the transceiver from the line rate clock (RXCLKIN). In this mode no additional reference clock is required. This mode produces the lowest jitter generation.
= 0 for normal operation utilizing the internal PLL

LOOPTIM1
Reference clock port selection
= 1 to allow the PLL reference clock to be provided at the LPTIMCLK inputs
= 0 to allow the PLL reference clock to be provided at the reference clock inputs

FACLOOP
Facility loopback mode control.
= 1 to bypass 16-bit bus, so that serial data in (RXIN) is routed to serial data out (TXOUT)
= 0 for normal transceiver operation

FSEL
Sets the line rate for the multi-rate 16-bit transceiver.
For OC-48,
FSEL0 = 0 and FSEL1 = 0
For OC-12,
FSEL0 = 0 and FSEL1 = 1
For OC-3,
FSEL0 = 1 and FSEL1 = 1.

- SW4: VCS122
Static Controls

FSEL
Sets the line rate for the multi-rate CDR, if present
For OC-48,
FSEL0 = 0 and FSEL1 = 0
For OC-12,
FSEL0 = 0 and FSEL1 = 1
For OC-3,
FSEL0 = 1 and FSEL1 = 1.

REFSEL
Sets the reference clock frequency used by the CDR (provided by a crystal in the socket at U3)
For /16 clock, REFSEL0 = 1 and REFSEL1 = 1
For /32 clock, REFSEL0 = 0 and REFSEL1 = 1
For /64 clock, REFSEL0 = 1 and REFSEL1 = 0
For /128 clock, REFSEL0 = 0 and REFSEL1 = 0

- SW5: NOT CONNECTED

- SW6: TRANSMIT
This switch allows the transmit function of the optics module to be enabled or disabled.

Clock Generator

An on-chip Phase Locked Loop (PLL) generates the 2.488 GHz transmit clock from the externally provided REFCLK input (provided by a crystal in the socket at U6). The on-chip PLL uses a low phase noise reactance based Voltage Controlled Oscillator (VCO) with an on-chip loop filter. The loop bandwidth of the PLL is within the SONET specified limit of 2 MHz. The customer can select to provide either a 77.76 MHz reference or 2 x that reference, 155.52 MHz.

Signals and Levels

All signals going into or out of SMA connectors on the board, except for RXCLK16_32, are ac coupled, allowing ease in connecting to test equipment with internal terminations of 50 ohms to GND or limited level adjustment capability. Beginning from the upper left corner of the board and going clockwise, the following signals are provided from/to the board:

CLK128O+/CLK128O-:
Divide by 128 version of the RXCLKIN clock to the 16-Bit Transceiver. Used as a utility clock to provide a reference for external needs.

RXCLK16_32+/ RXCLK16_32-:
Divide by 16 or 32 clock output derived from the received line rate clock at RXCLKIN. These outputs can be used to provide the necessary reference clock input to the MUX side of the transceiver at LPTIMCLK +/-.

TXCLK16O-/TXCLK16O+:
Divide by 16 version of the TXCLKOUT clock from the 16-Bit Transceiver. This can be used in a contradirectional clicking scheme between the transceiver and a framer/mapper.

LPTIMCLK+/LPTIMCLK-:
An alternate reference clock inputs to the 16-Bit Transceiver PLL. This clock has to be in sync with the parallel data clock feeding the mux input, so the RXCLK16_32 outputs can be used as the source of this clock. This results in the transmit and receive paths operating at the same rate. (LOOPTIM1 is set to 1 for this mode)

LED Indicators

There are five LED indicators on this board:

D1: (PARERR)
When lit, indicates that the parity of the 17 bits (TXIN[15:0] and TXPARITYIN) does not conform to the expected parity designated by PARMODE.

D2: (LOS)
When lit, indicates presence of data at the Rx input to the optical transceiver.

D3: (OVERFLOW)
When lit, indicates FIFO overflow which will result in the loss of transmitted data.

D4: (LOL)
When lit, indicates that the VCO frequency of the CDR differs by more than 1 MHz of the reference clock-based rate

D5: (NOREF)
When lit, the frequency of the reference clock is 25% above/ below the expected value, or not present at all.

HFCT-5942L Monitoring points.
Tests points are provided on the board for Laser Bias Monitor (J25), Rear Facet Monitor (J24) and Detector Bias Current Monitor (J22). The HFCT-5942L Data Sheet demonstrates how these monitoring points can be incorporated into a design.

Jitter Generation

The evaluation board fulfills the jitter generation requirements for SONET/SDH when tested with HFCT-5942. Jitter generation results in Table 1 were measured using the equipment setup shown in Figure 1.

Table 1. Jitter Generation results

Power into SFF Rx	0 dBm	-18 dBm	-23.6 dBm
rms	6 mUI	6 mUI	6 mUI
Pk-Pk	62 mUI	62 mUI	65 mUI

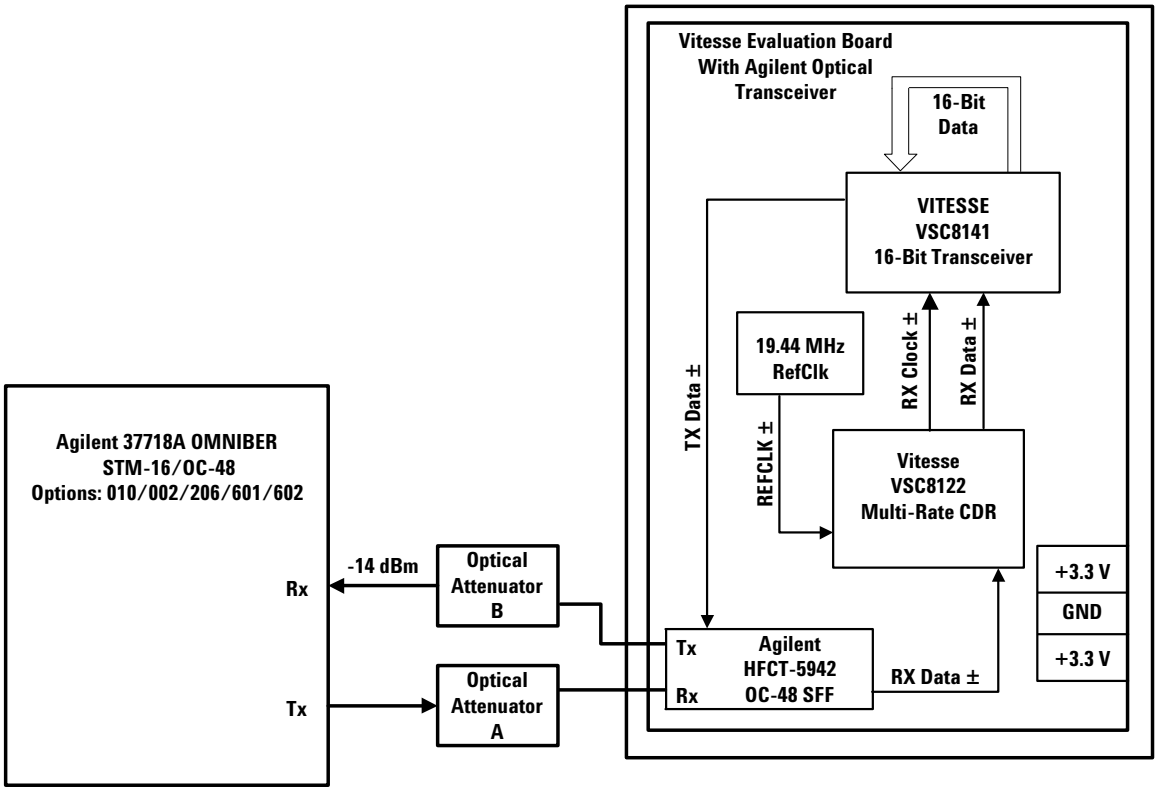


Figure 1. Jitter Generation, Tolerance and Transfer test configuration

Jitter Tolerance

The reference design fulfills the jitter tolerance requirements for SONET GR-253 when tested with HFCT-5942. Jitter Tolerance was measured with optical attenuator A adjusted to sensitivity + 1 dB (-22 dBm into Rx for sample tested). Figure 2 shows typical jitter tolerance performance from measurements made using equipment setup shown in Figure 1.

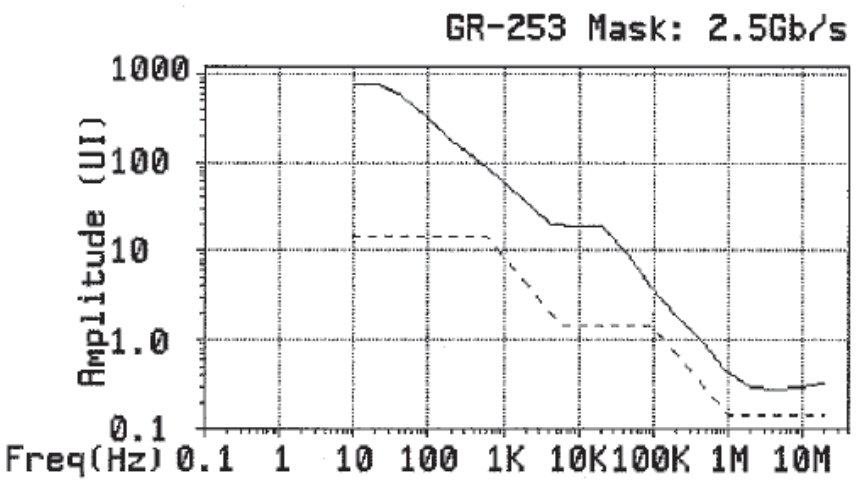


Figure 2. Typical jitter tolerance performance of the reference design board against the SONET GR-253 mask

Jitter Transfer

The reference design fulfills the jitter transfer requirements for SONET/SDH when tested with HFCT-5942. Jitter Transfer was measured with optical attenuator A adjusted to sensitivity + 1 dB (-22 dBm into Rx for sample tested). Figure 3 shows typical jitter transfer performance from measurements made using equipment setup shown in Figure 1.

Conclusions

The information presented in this application note will help the designer to quickly and successfully develop an Agilent/ Vitesse provided solution for an OC-48 SONET compliant reference design, at the first attempt.

The test data and test methods provided will aid the designer in correlating the performance of their system. Also, the layout provided will assist designers in optimizing their printed circuit board design.

References

[1] HFCT-5942 Data sheet
[2] Vitesse VSC8122 Data sheet
[3] Vitesse VSC8141 Data sheet
[4] GR-253 – CORE Generic Requirements Synchronous Optical Network (SONET) Transport Systems, 1997
[5] ITU-T Recommendation G.958 Digital Line Systems Based on The Synchronous Digital Hierarchy for use on Optical Fibre Cables, 1994

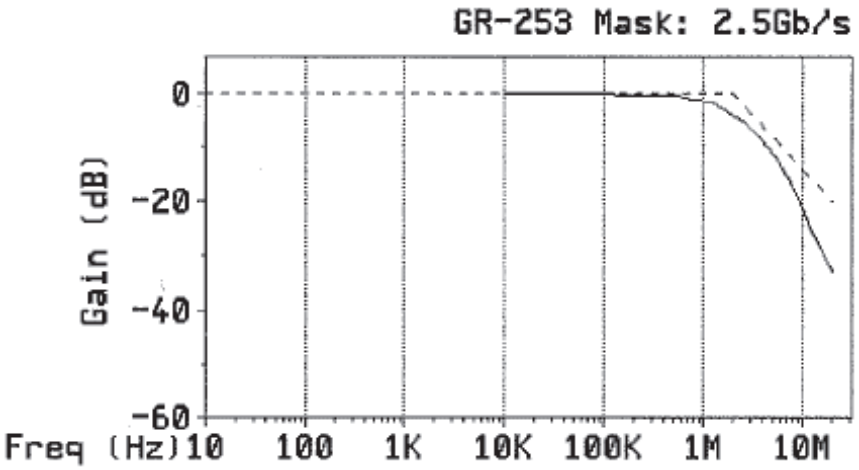


Figure 3. Typical jitter transfer performance of the reference design board against the SONET GR-253 mask

Web Sites

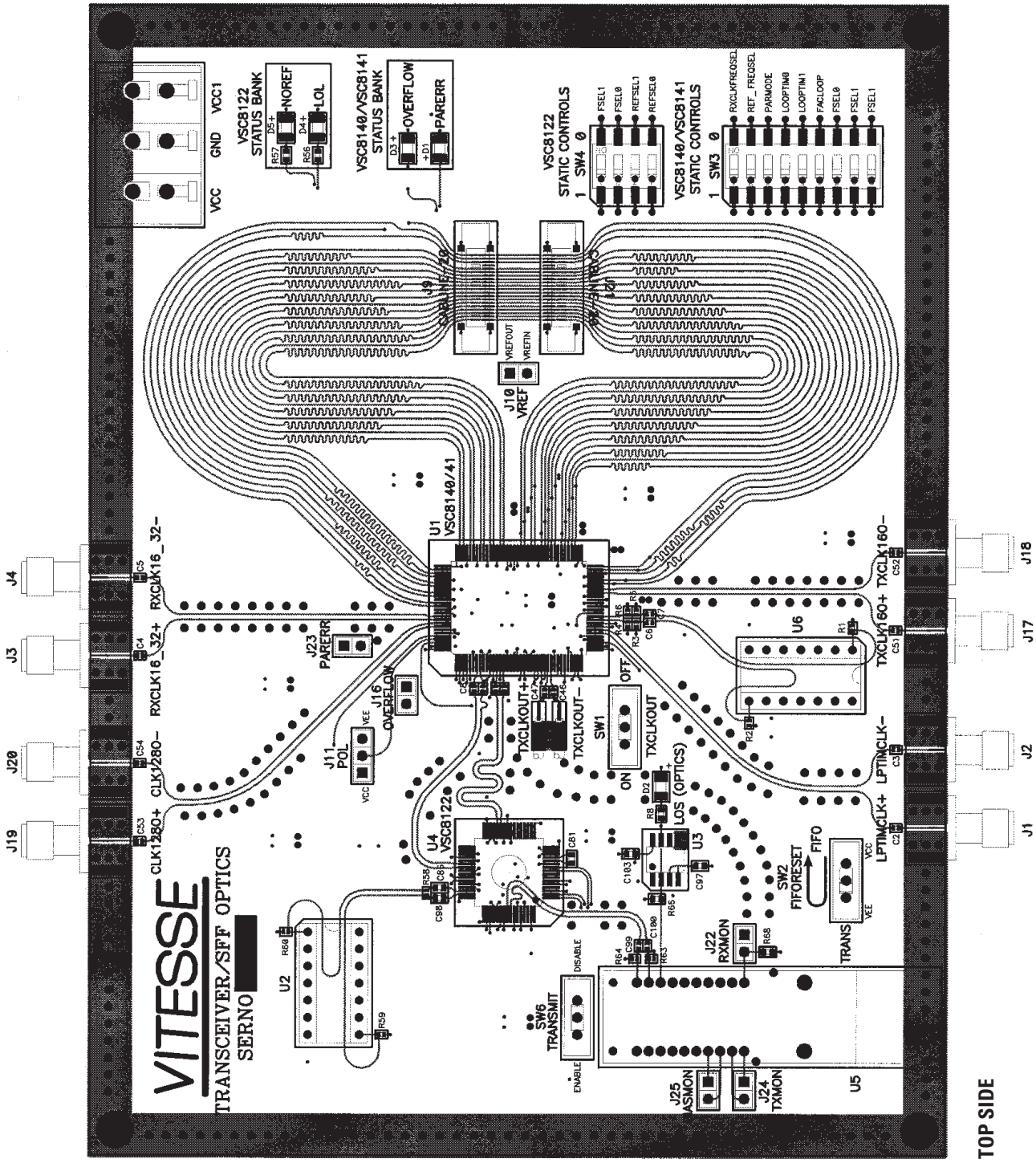
www.semiconductor.agilent.com
Agilent Technologies component information.

www.vitesse.com
Vitesse Semiconductor Corporation web site.

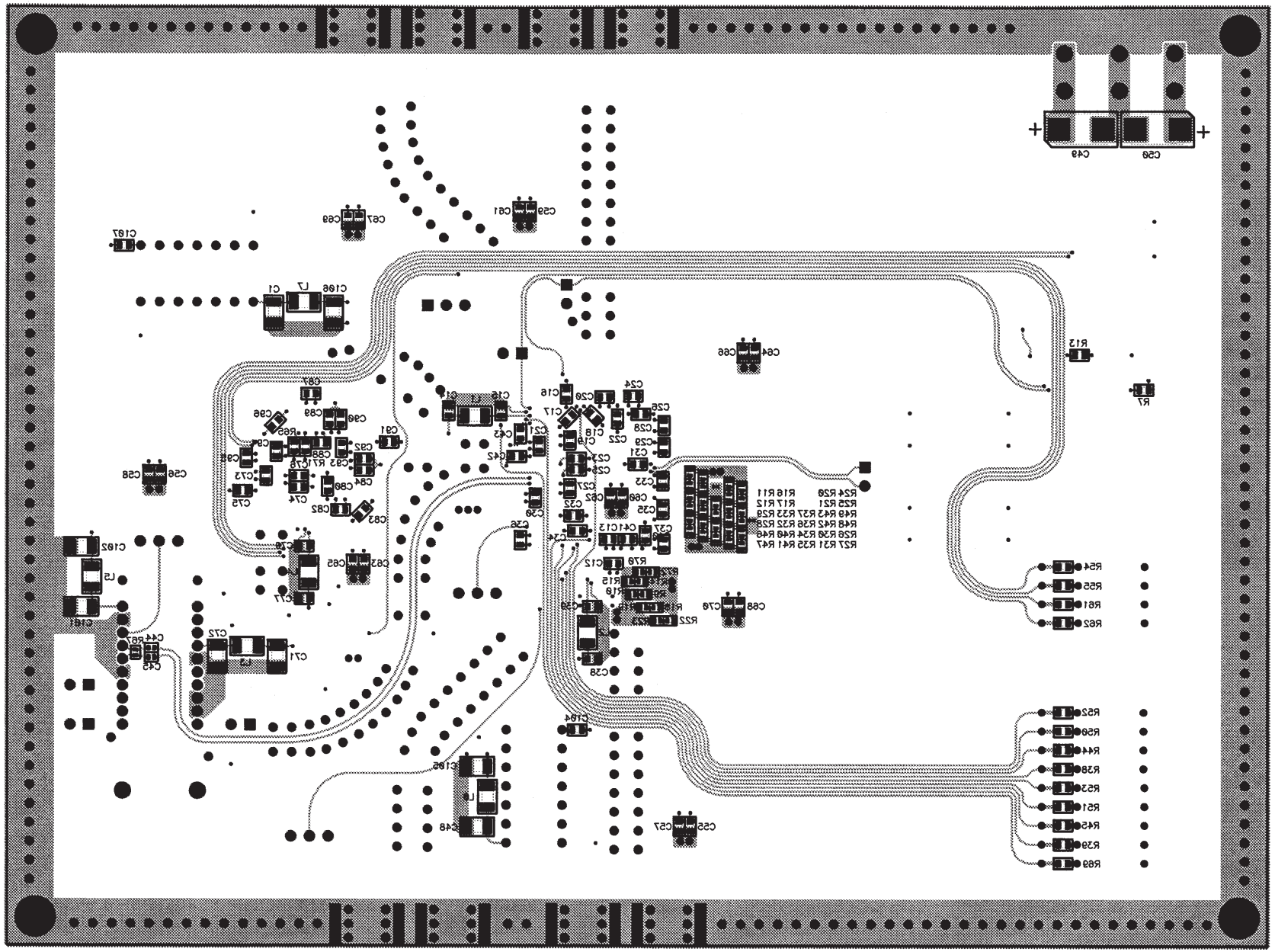
This evaluation board is intended for evaluation purposes only. Agilent does not guarantee its performance in a production environment.

Information in this application note is subject to change without notice.

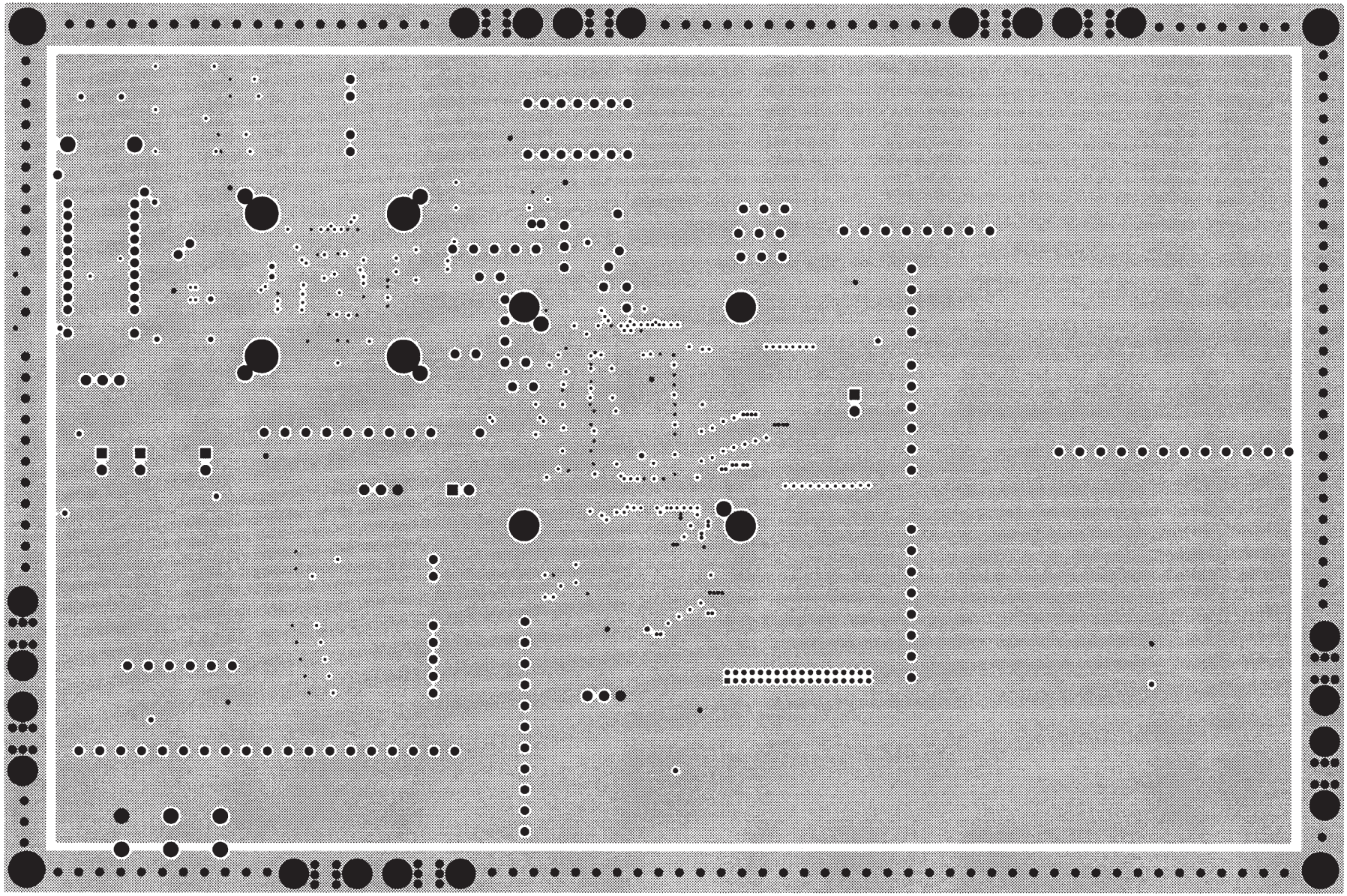
Appendix 1. Reference Board Layout



TOP SIDE



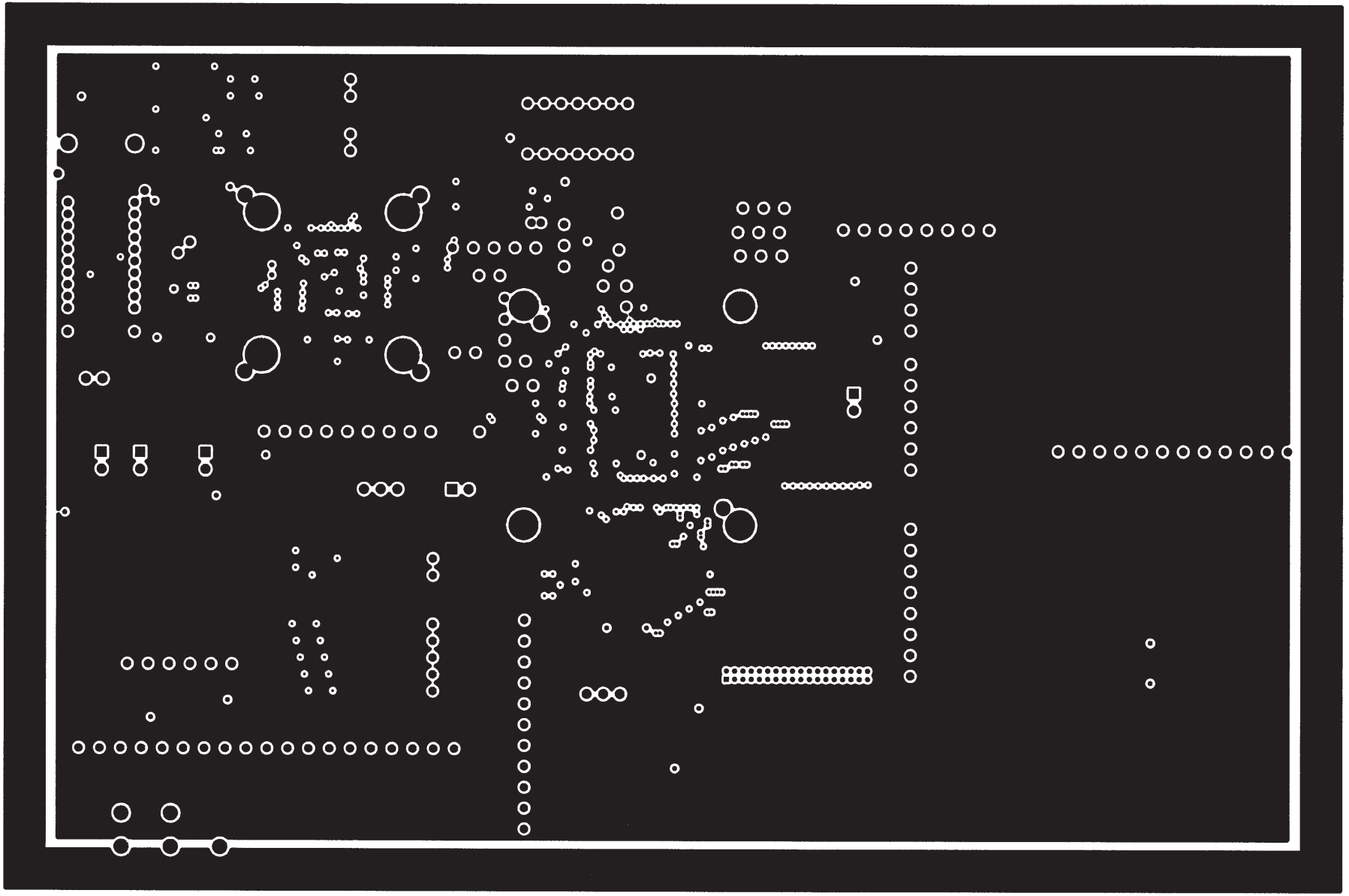
BOTTOM SIDE



V_{CC} POWER PLANE

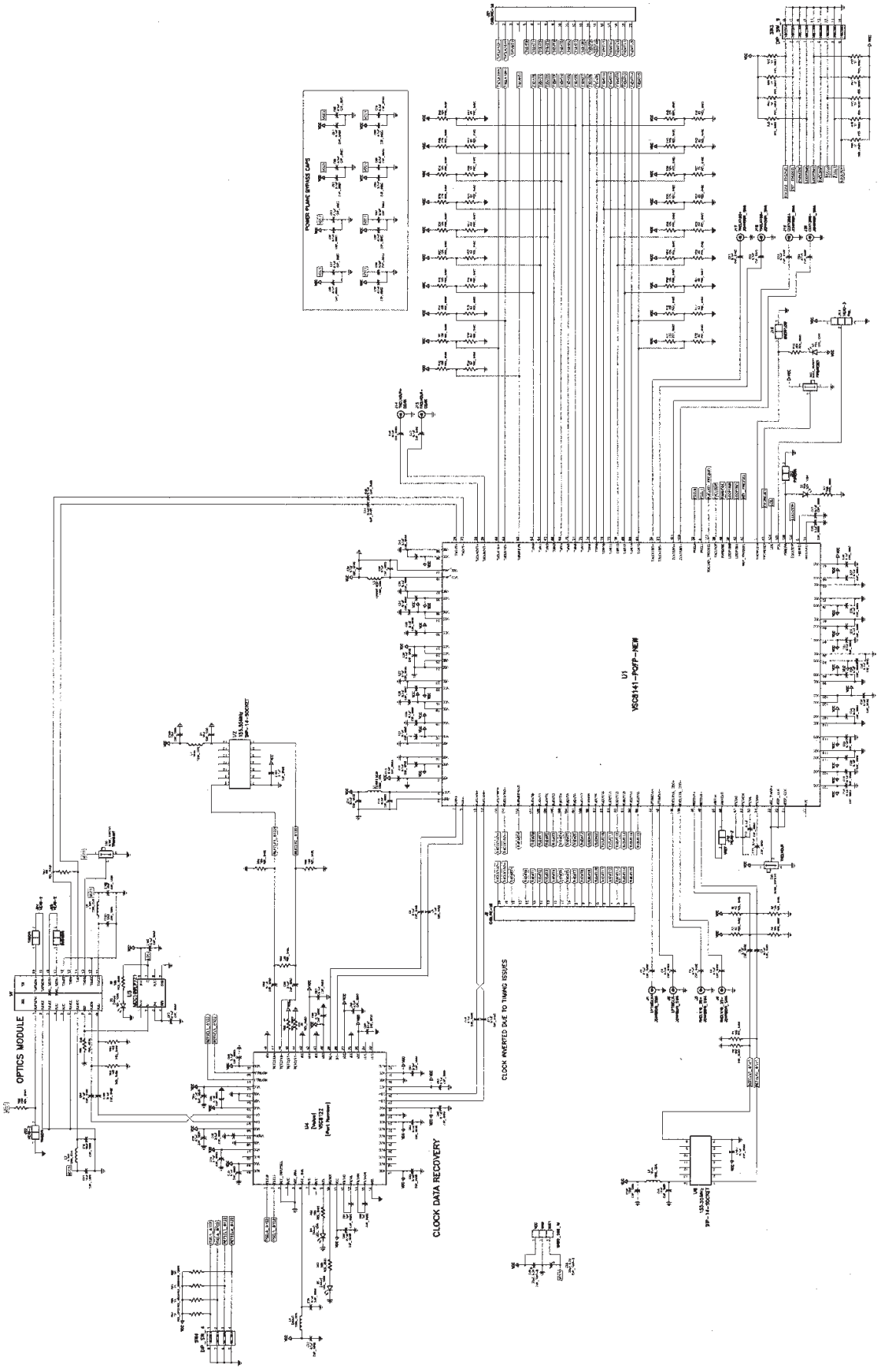
SMA GROUND PLANE

INNER SIGNAL



V_{CC2} POWER PLANE

Appendix 2. Circuit Connections



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Data subject to change.

Obsoletes: 5988-3579EN
December 10, 2001
5988-5085EN

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