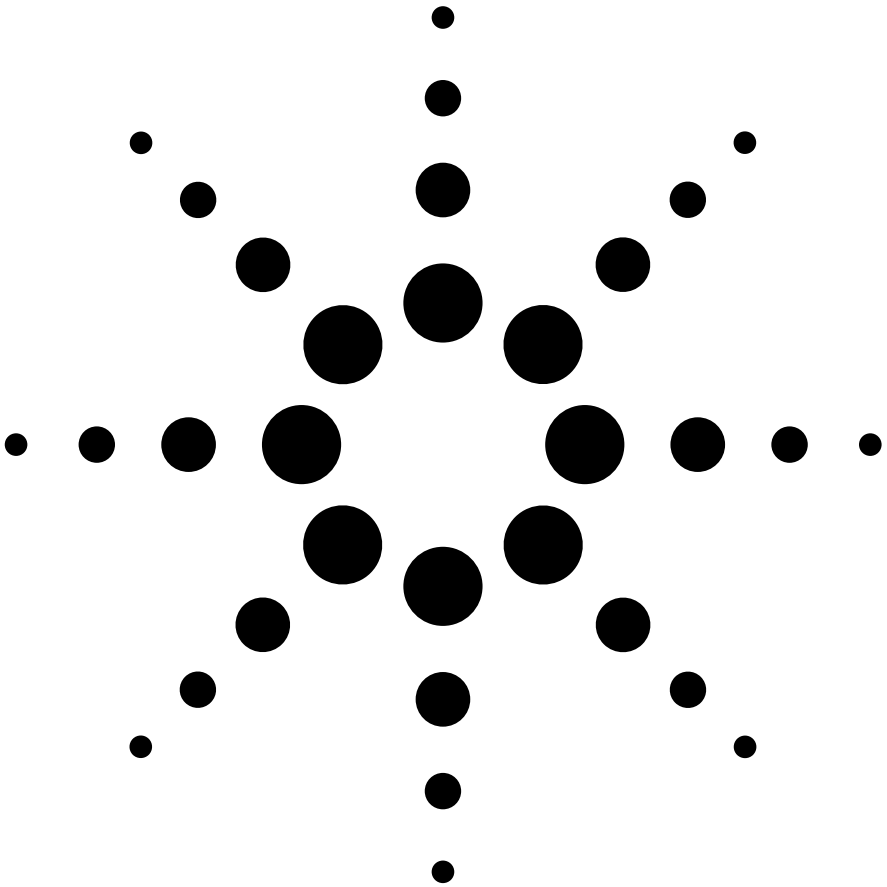
Agilent Technologies

Generating Custom, Real-World Waveforms

Integrating Test Instrumentation into the Design Process

Application Note 1360



Agilent Technologies
Innovating the HP Way

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Introduction

With pressure to be first to market, wireless system manufacturers routinely design to standards still in a state of flux. This situation highlights what has become a fundamental need–namely, allowing system, DSP, and RF designers to work together more effectively using a common simulation tool. This enables more effective performance tradeoffs and partitioning to occur between RF and DSP designs. Once the system is modeled, behavioral models are replaced with actual RF and DSP component designs to evaluate their effect on performance. This bottom-up verification provides validation that the design will meet specifications as system development progresses. This is key to ensuring first-pass success and meeting launch windows in today's highly competitive marketplace.

The ability to link test instrumentation with design software provides a new level of abstraction that is required for bottom-up design verification. In essence, design software is used to define new signal formats, which are then synthesized and analyzed using test instrumentation. System performance is validated using a combination of behavioral models, detailed circuit and DSP designs, and actual measured data from hardware using instrumentation.

This application note demonstrates how modern design software and test instrumentation can be used together to create and analyze signal waveforms for 3G (third-generation) wireless systems. For illustration, a top-level system design is modeled in Agilent's Advanced Design System (ADS) software. Using a 3G design library, a real-world cdma2000 SR3 modulated signal is created and passed through the upconverter design to evaluate the resulting signal's spectral regrowth and ACPR (adjacent channel power ratio). After analyzing the simulation results, actual performance is measured in hardware. This process reveals how a 3G-modulated signal, or any signal for that matter, can be created and analyzed using links between design software and test instrumentation.

Advanced Design Systems (ADS) – the key to complete signal path design

Advanced Design Systems (ADS) software provides the ability to model an entire signal path for a wireless communications system–from bits in to bits out. This includes the top-level system design, the RF circuit designs, and the baseband DSP designs. The ability to work within a single design environment enables tradeoffs to be made between subsystems, allowing requirements to be partitioned at the system level. It also permits detailed RF and DSP components to be incorporated back into the top-level system for bottom-up design verification.

Top-level design

It is important to quickly and accurately predict top-level system performance using parameters such as BER (bit error rate), ACPR, and EVM (error vector magnitude). The system designer assembles behavioral elements to quickly create a top-level system design that serves as a virtual scratchpad for making design tradeoffs between RF and DSP performance. Once completed, the simulated system is easily translated into specific requirements for components and subsystems.

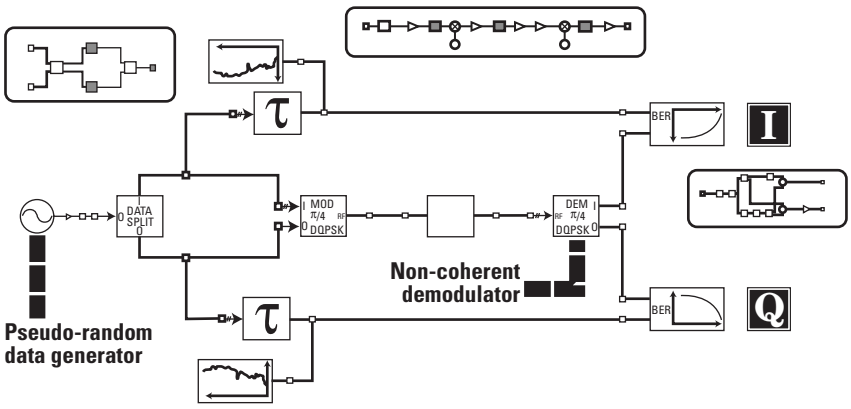


Figure 1. A robust development environment allows the top-down design to occur rapidly, as well as enabling accurate prediction of BER, ACPR, and other key performance metrics for mixed DSP/RF system designs.

After determining functional requirements for the top-level system, work can begin on designing the individual RF and DSP components. As this work progresses, the top-level system design serves as the template for evaluating the effects of specific components on the system's overall performance. This is the essence of efficient bottom-up verification.

For illustration, imagine the top-level system is an EDGE receiver with a given BER performance requirement. Unfortunately, BER specs do not intuitively translate into RF component design requirements. On the other hand, detailed RF designs such as an oscillator, are easily inserted into the top-level design, allowing the designer to quickly gauge the component's effect on the overall BER sensitivity. This ability to mix levels of abstraction enables evaluation of system performance at every stage of the design process.

The final level of abstraction is represented by the ability to link the simulated design to test instrumentation, where the measured performance of specific hardware components can be inserted back into the top-level system to evaluate their effects on overall system performance.

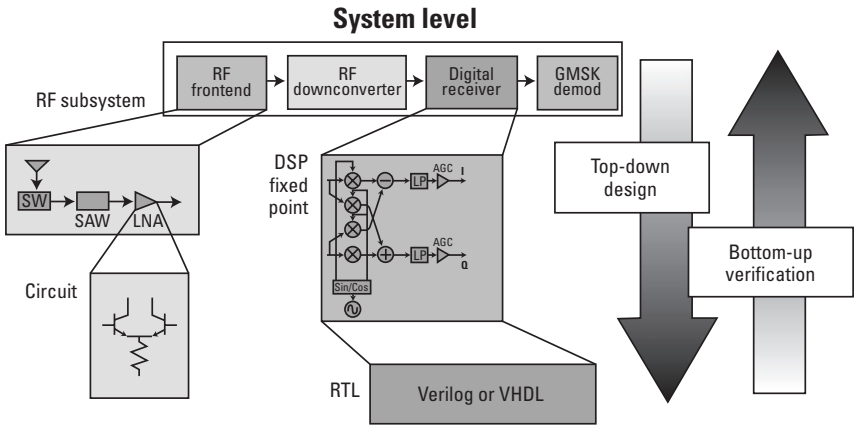


Figure 2. Effective system development demands abstraction and implementation at various levels of the design.

Linking design and test capabilities

Integrating test instrumentation with design software represents an essential new tool for system engineers. Design software that includes built-in links to signal generators, spectrum analyzers, network analyzers, and vector signal analyzers lets engineers capture real signals for use in simulations or to generate new signal formats.

The transition from design to prototype characterization is a common source of delay in a typical development schedule. Meeting this particular milestone requires all components for the prototype to be completed on time, or system testing is delayed.

Linking EDA tools and test equipment gives engineers the ability to use software models as virtual prototypes, and begin system testing before all the hardware is available.

This capability helps overcome delays in component development, speeding up the time required to reach the prototype stage. Integration between design tools and instrumentation represents the final level of abstraction in design verification, allowing the design to be continually verified as prototype hardware is built.

Links speed up conceptualization and subsystem development

Design software and test equipment links are applied to both the investigation and design phases of system development. Design conceptualization is facilitated by generating source test signals with a software simulator. This enables virtual verification of designs in the earliest phases of the project, and allows rapid evaluation of existing designs for new systems.

In the development phase, designers can carry out virtual integration of sub-systems, at the system level, long before the system prototype is fabricated. These powerful links facilitate making rapid decisions regarding system design tradeoffs–for instance, when components don't measure up to specified requirements.

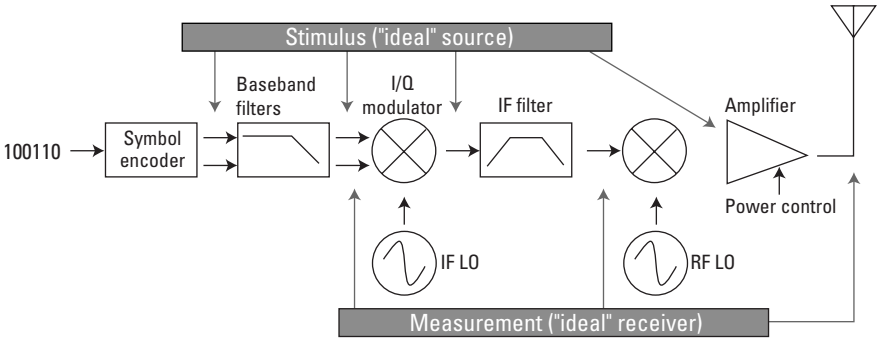


Figure 3. Design-to-test links enable simulation and measurement of individual subsystems in the "ideal" transmitter as they are completed, using complex, digitally-modulated stimulus signals.

In most cases, it is necessary to examine the transmitter system at various test points as each component or subsection is finished (figure 3). This requirement requires a stimulus signal to emulate the unfinished upstream sections. Traditionally, an unmodulated carrier signal is used. However, design-to-test links enable complex digitally-modulated stimulus signals to be used instead, providing much more realistic measurements.

Links speed design flow

Linking simulation with test equipment improves simulation accuracy and speeds up design verification. Breaking the process down into its fundamental steps (figure 4), the first phase is creating the top-level design. For example, a modern 3G wireless system is composed of a 3G source and upconverter, which are integrated together. The design is then evaluated using design software.

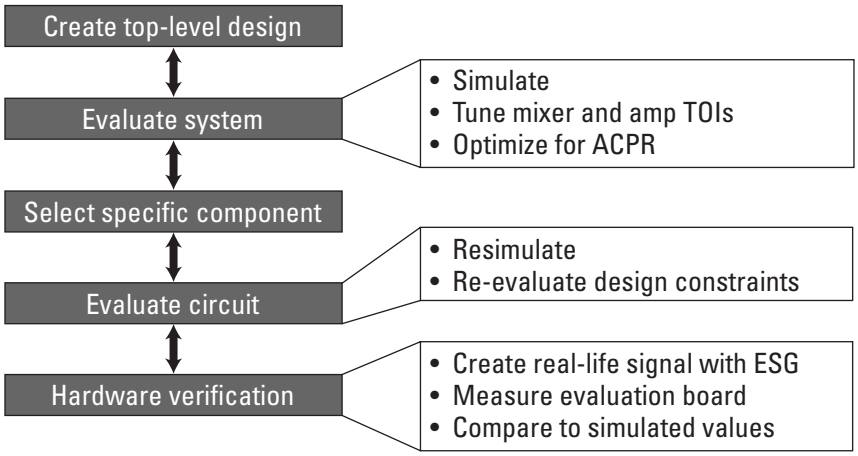


Figure 4. Fundamental steps in designing a hypothetical 3G wireless communications system.

Next, the system design must be evaluated and optimized to meet specified requirements. To accomplish this, performance optimization is used on the behavioral system design to partition design requirements. Once the design requirements are partitioned, detailed circuit designs can replace each of the behavioral elements. To illustrate this, an actual amplifier design is inserted in place of a behavioral amplifier in the top-level design. The system is then re-simulated and re-evaluated to determine whether the system still meets specifications with the final circuit implementation.

In the fifth and final phase, hardware verification of the design is performed by integrating the design software with a signal generator to create a real world signal on the bench to test the amplifier. Actual measurement results are then compared to the simulation results.

Building the top-level design

The process of assembling a top-level system begins by placing a signal source in the schematic. In this case, a cdma2000 SR3 wideband signal source is shown using the ADS cdma2000 design library (see figure 5). Design libraries typically contain all of the necessary baseband blocks to perform such functions as framing, encoding, and interleaving. In fact, RF designers can usually leverage the signal generation and measurement capabilities of standard libraries to perform simulations such as ACPR, constellation, eye, EVM, and BER measurement. DSP designers carry out similar work by simply replacing the functional baseband blocks with their own algorithms or designs, using the same simulation environment.

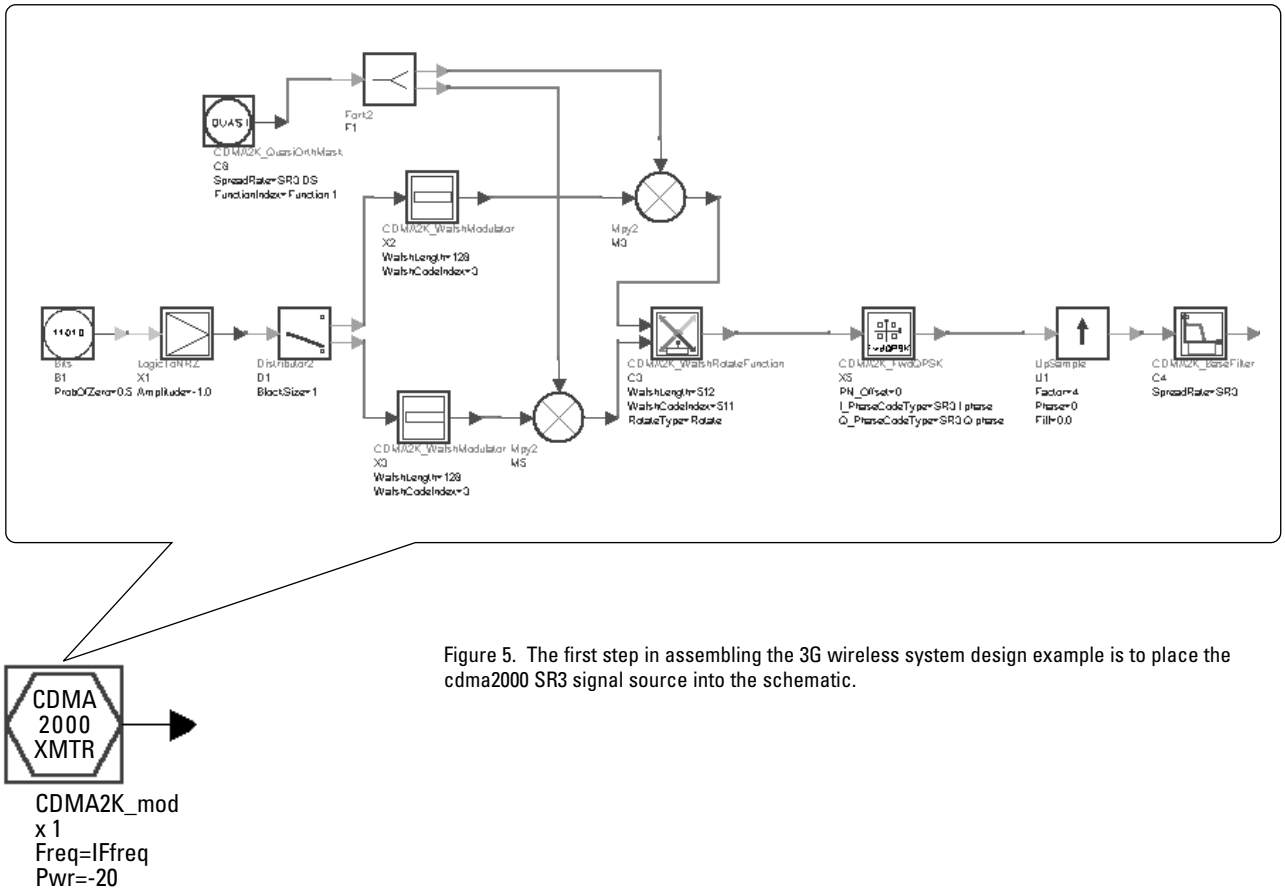


Figure 5. The first step in assembling the 3G wireless system design example is to place the cdma2000 SR3 signal source into the schematic.

Now, the rest of the preliminary top-level design is assembled. This includes adding an upconverter, which feeds the input to a driver amplifier (figure 6).

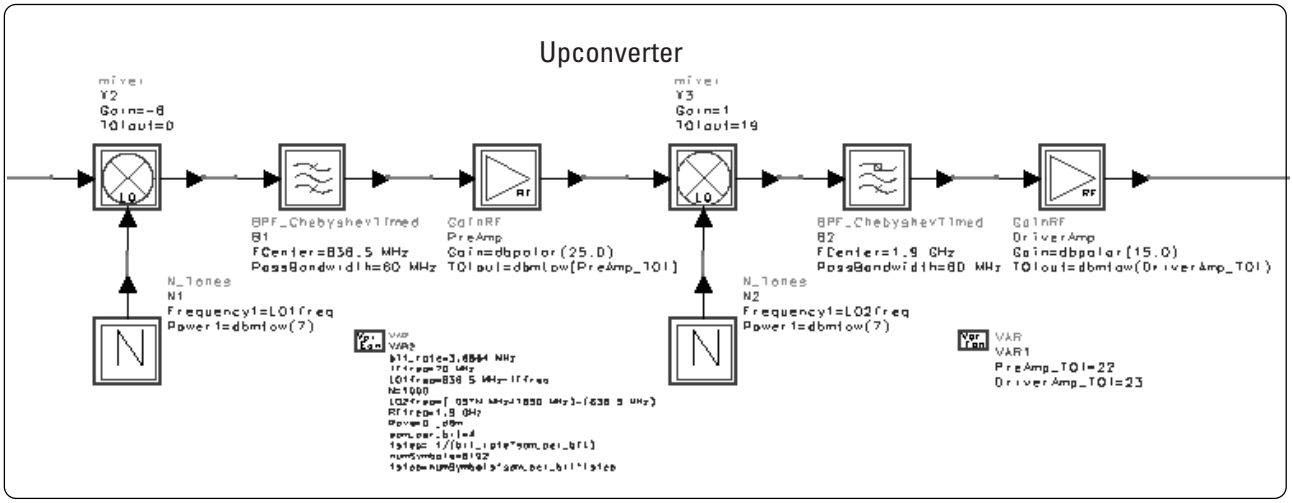


Figure 6. In the example 3G system, a 70 MHz IF is upconverted to the PCS band at 1.9 GHz using the circuit shown. Mixers, amplifiers, and filters are represented by behavioral blocks.

At this point, parameters such as gain and third-order intercept (TOI) points can be specified for the upconverter behavioral blocks. Once the component requirements are allocated, any designer working on the project can perform "what if" evaluations by replacing a behavioral block with detailed component designs. The completed top-level system example includes the cdma2000 source, upconverter, and spectrum analyzer as seen in figure 7. Now the complete system can be simulated and evaluated for spectral regrowth performance.

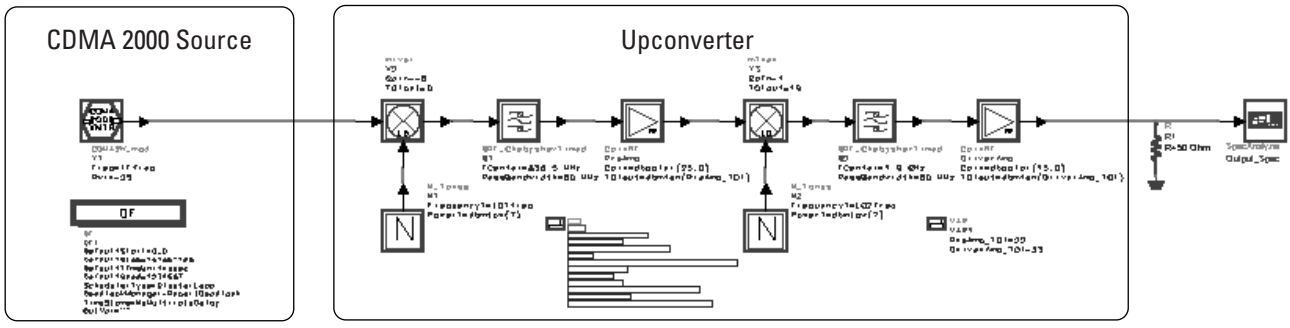


Figure 7. This is the top-level 3G wireless system design example, complete with cdma2000 source, upconverter, and spectrum analyzer.

Evaluating system performance

Simulated results clearly show spectral regrowth resulting from the TOI points of the mixers and amplifiers (figure 8). At this point, it is difficult to determine how much each component is contributing to the overall spectral distortion. Tuning the parameters of the individual components can help determine the sensitivity of the spectral distortion relative to the TOI points of each component.

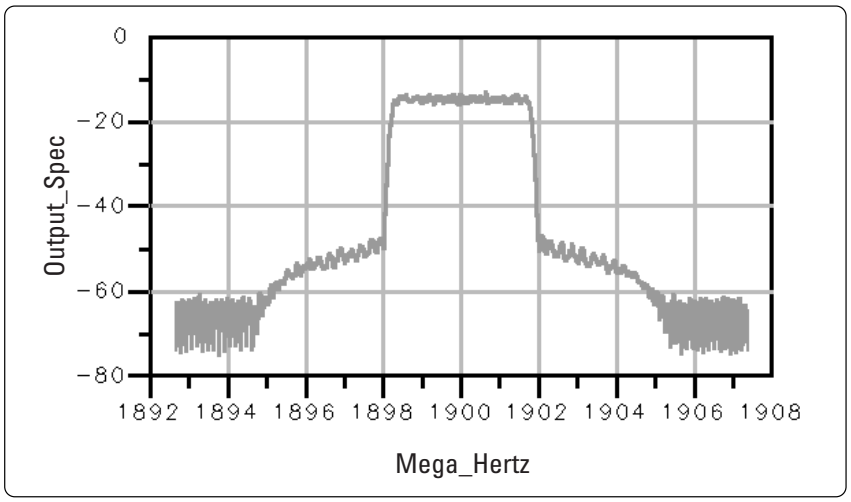


Figure 8. Initial spectral regrowth simulation results for the example 3G wireless system design. The output shows spectral distortion from the combined effect of the TOI points for all mixers and amplifiers. Without further investigation, it is difficult to determine how much each component contributes. The driver and power amplifier are typically the largest contributors to overall spectral distortion in RF transmitters. In this case, it is the driver amp, since it is the last amplifier in the upconverter.

For example, tuning the TOIs as seen in figure 9, reveals that the spectral regrowth is primarily due to the driver amplifier, which is the last amplifier in the upconverter. This is expected, since the driver amplifier and power amplifier are typically the largest contributors to overall spectral distortion.

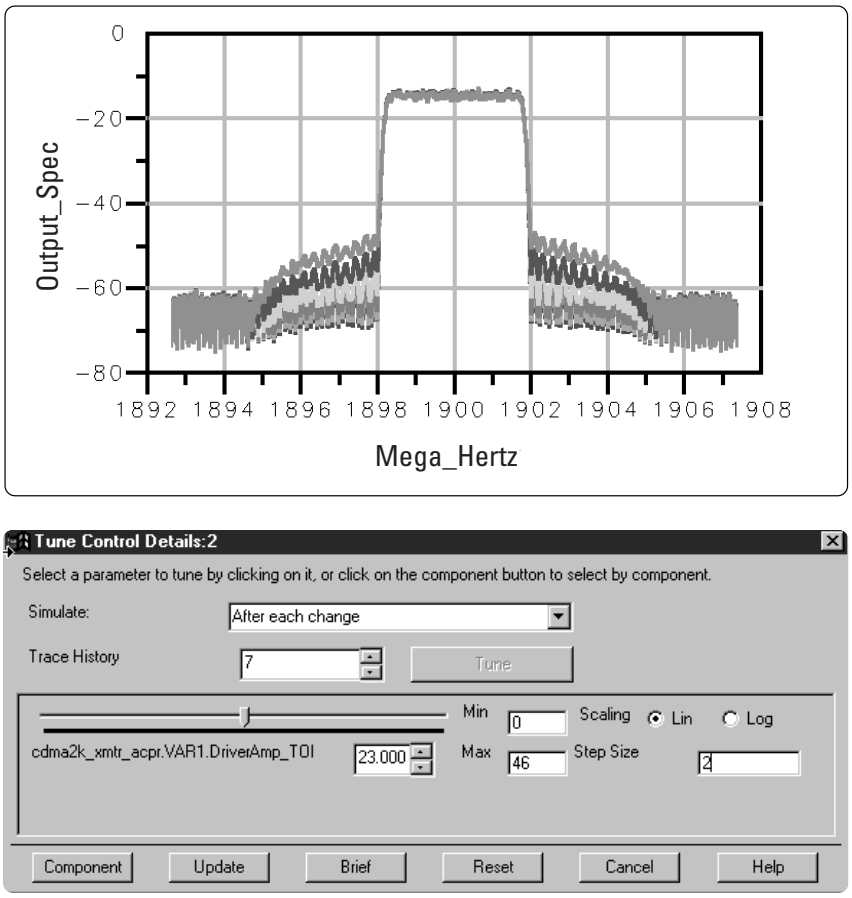
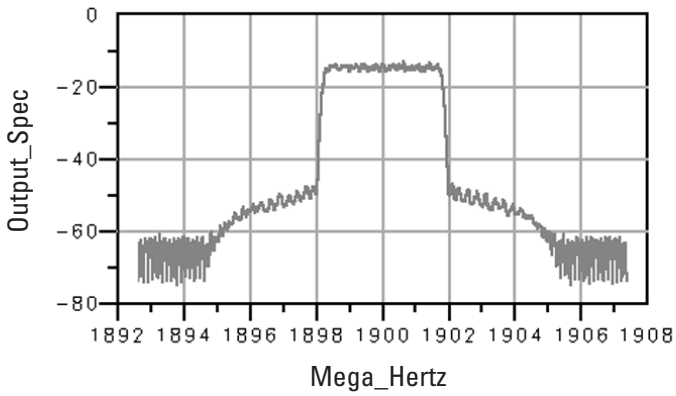


Figure 9. Tuning the mixer and amplifier third-order intercept points.

At this point, an ACPR simulation can be performed to determine the minimum TOI points to meet the required system performance. Setting this up is relatively straightforward. It consists of integrating the power between the required lower and upper frequency limits (figure 10) for the main and adjacent frequency bands and taking the difference.



Eqn main_ch_power_dBm=spec_power(Output_Spec,1900-3.6864/2,1900+3.6864/2)

Eqn upper_ch_power_dBm=spec_power(Output_Spec,1905-3.6864/2,1905+3.6864/2)

Eqn acpr_upper_dBc=upper_ch_power_dBm-main_ch_power_dBm

main_ch_power_dBm	upper_ch_power_dBm	acpr_upper_dBc
9.267	-33.159	-42.427

Figure 10. The ACPR measurement in the example wireless system integrates the main channel power over a 3.6864 MHz signal bandwidth. The upper adjacent channel power is integrated over the same 3.6864 MHz bandwidth, but with a 5 MHz frequency offset. The difference between the two powers is the ACPR, which is 42 dB in this example. Note that the frequency offsets and integration bandwidths used in this example were the preliminary numbers for cdma2000 at the time of publication, and are subject to change.

The upconverter drives a power amplifier, which is the dominant contributor to spectral regrowth. The ACPR performance of the system is -42 dB, as seen in figure 10, however, the design specification is -47 dB. Performance optimization can be used to determine the TOIs of each component to meet this goal.

Before performance improvements can begin, parameters and ranges for optimization values must be specified in the design software. In this case, they are the TOI points of the amplifiers and mixers. An example of this process is shown in figure 11.

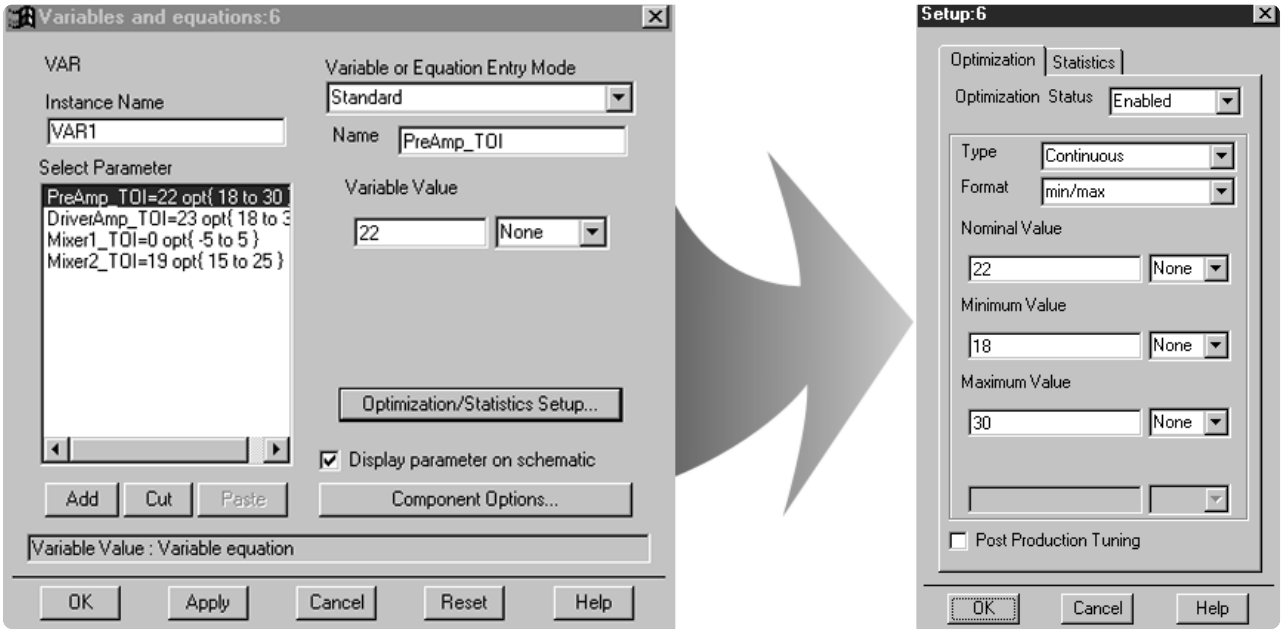


Figure 11. These interface windows are used for setting parameters and ranges prior to performance optimization in ADS. In the example system, the driver amp TOI point is optimized from 18 to 30 dBm.

Next, optimization goals and controls must be established. Measurement equations are used to calculate ACPR, which represents the optimization goal. Optimization control is established by the minimum and maximum values for ACPR, which helps determine the minimum TOI points to meet the specification (figure 12 and figure 13).

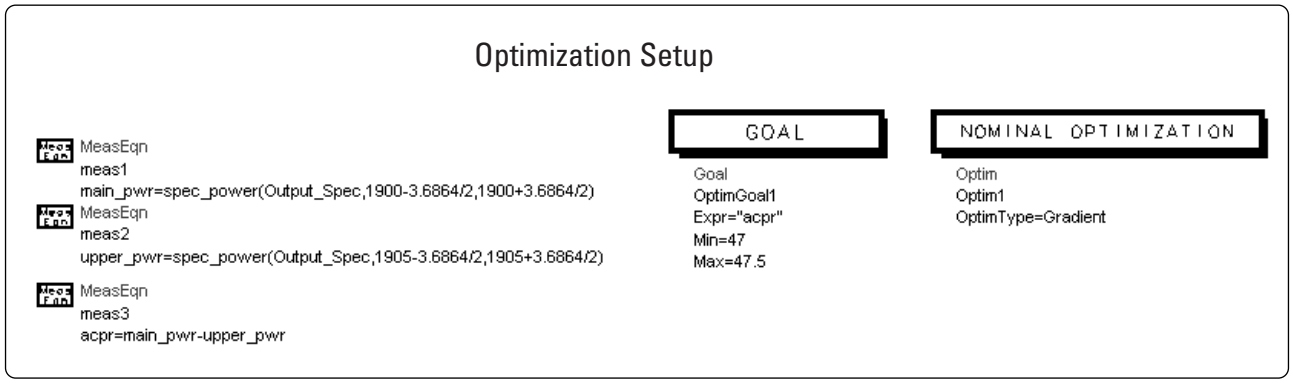


Figure 12. Setting up the simulation for optimization. In the example system, optimization setup consists of setting the minimum ACPR value to 47 dB (the desired result) and the maximum to 47.5 dB. The resulting calculation provides the minimum TOI points needed to meet the required specification.

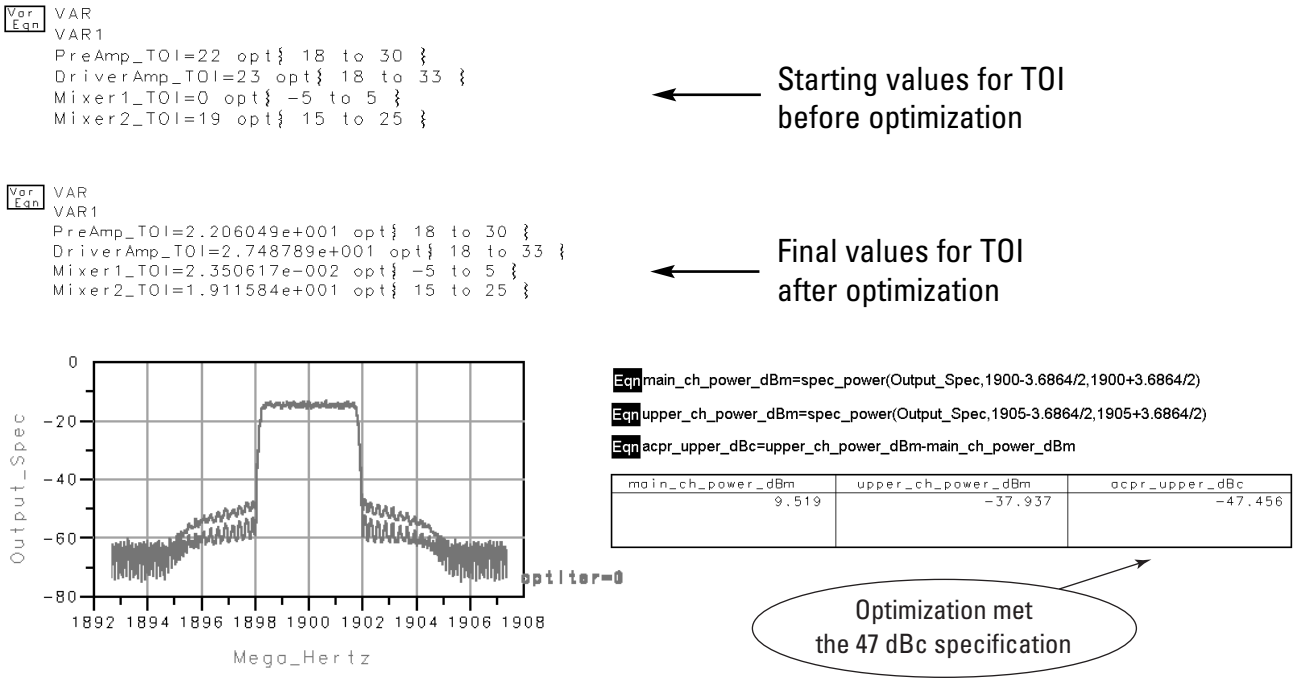


Figure 13. Here are the results of performance optimization for the example system. The variable data block at the top indicates the starting values for TOI points, while the bottom one shows the final values for TOI. Note that the driver amplifier TOI starts at 23 dBm, but is optimized to 27 dBm. None of the other TOI points changed significantly, which is expected since they do not contribute much to overall spectral regrowth. The resulting ACPR is 47.5 dB with a driver amplifier TOI of 27 dBm, which meets the desired specifications.

Component selection

Once minimum TOI points are defined that meet the required ACPR specification, components are selected or designed. For illustration, the driver amplifier is selected for the example system, because of its effect on spectral performance (figure 14).

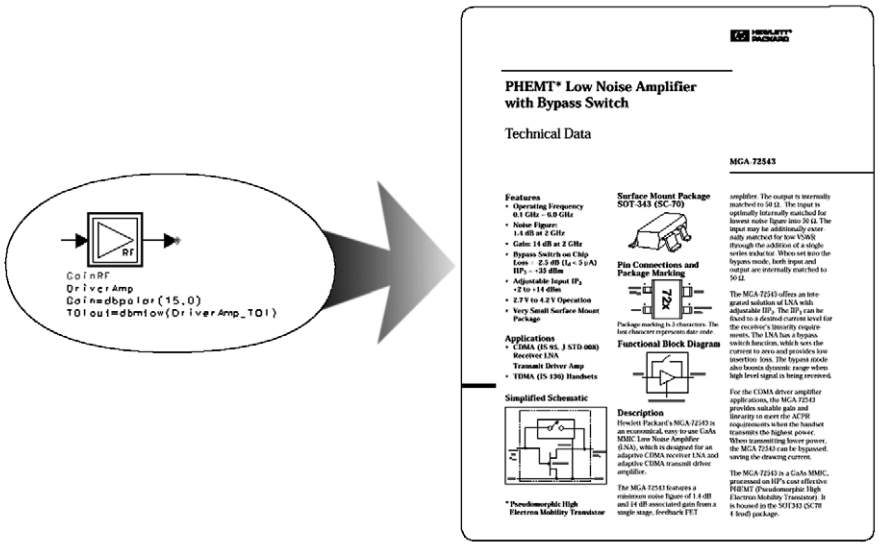


Figure 14. In the example system, Agilent's MGA-72543 PHEMT low-noise/transmit driver amplifier is selected. The TOI point of this GaAs MMIC device increases as bias current is raised, allowing it to be used as a driver amplifier for transmit applications. Also, the device can be biased at a lower current for use as an LNA for receiver applications. Furthermore, the integrated bypass switch in this device conserves current when transmitting at low power levels. The device can also be used in a dual-bias configuration, improving performance even further.

A detailed circuit model of the target amplifier device is provided by the manufacturer. A quick bias analysis is simulated to set the bias current to 40mA. Next, S-parameters and matching network requirements are analyzed for compatibility with performance specifications.

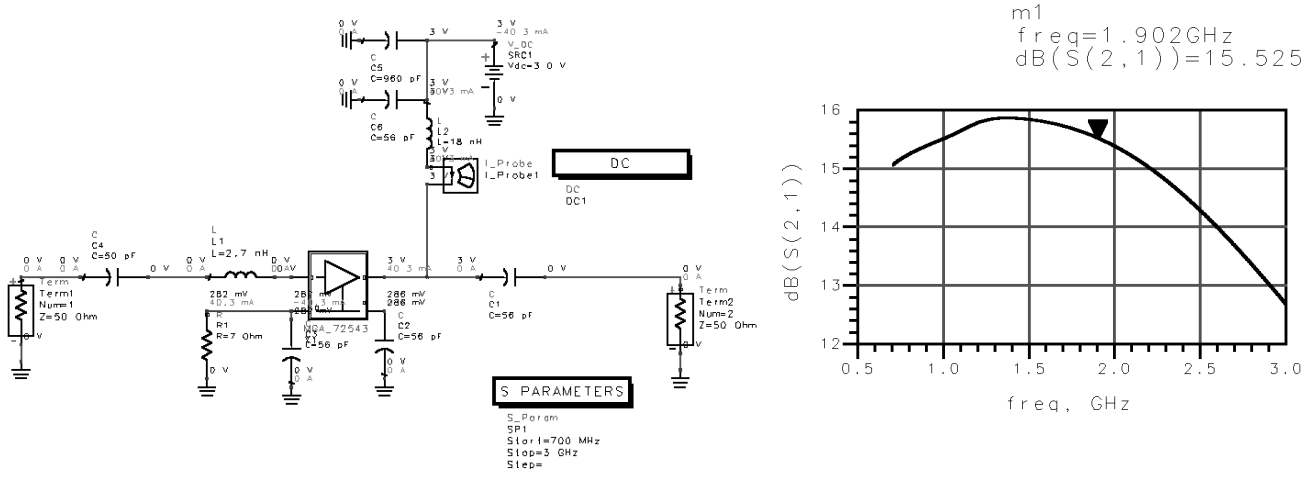


Figure 15. A quick bias analysis of the MGA-72543 amplifier results in a bias current setting of 40mA for the example system, and the device's specification reveals that an output TOI point of 27 dBm is expected given this bias condition. This should be sufficient to meet the ACPR performance goal based on the optimization results. An S-parameter analysis reveals approximately 15.5 dB of gain with a simple matching network.

Bottom-up component verification

Once a circuit is designed or an off-the-shelf component is selected for the driver amp, the detailed circuit model is inserted in place of the behavioral model in the top-level system, as seen in figure 16. A top-level system simulation is run so that the performance of the selected component can be evaluated as shown in figure 17 and figure 18. This illustrates how bottom-up verification of individual components is performed with a top-level system simulation.

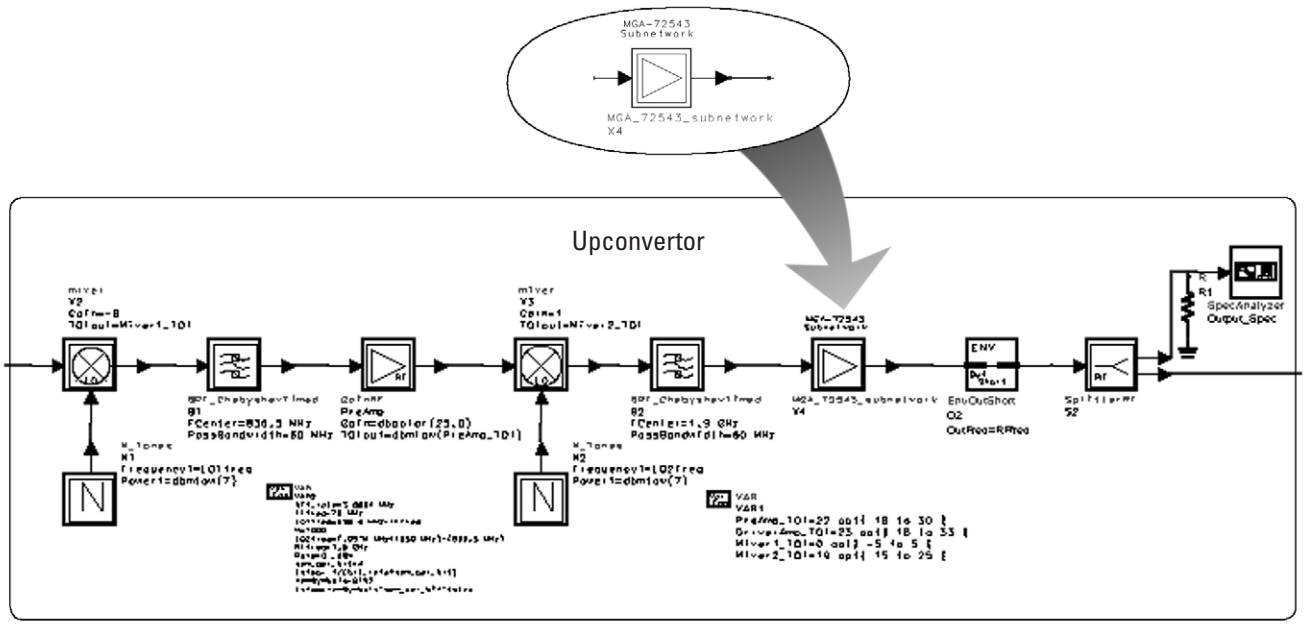


Figure 16. Once a suitable driver amp is selected, its detailed circuit model is inserted in place of the behavioral amp--the MGA-72543 in this case.

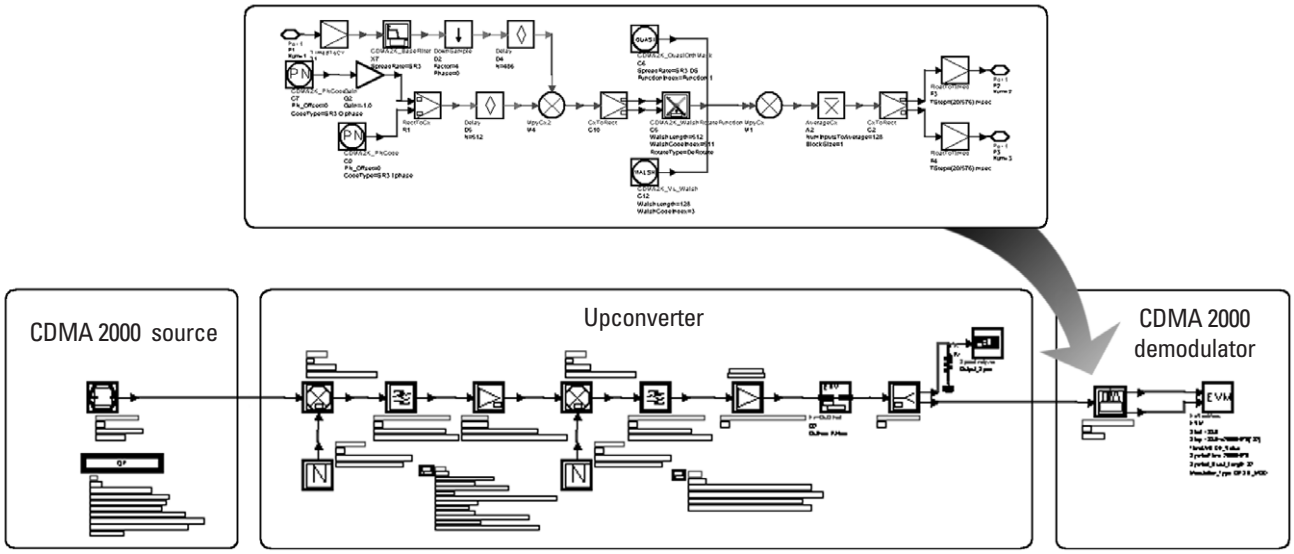
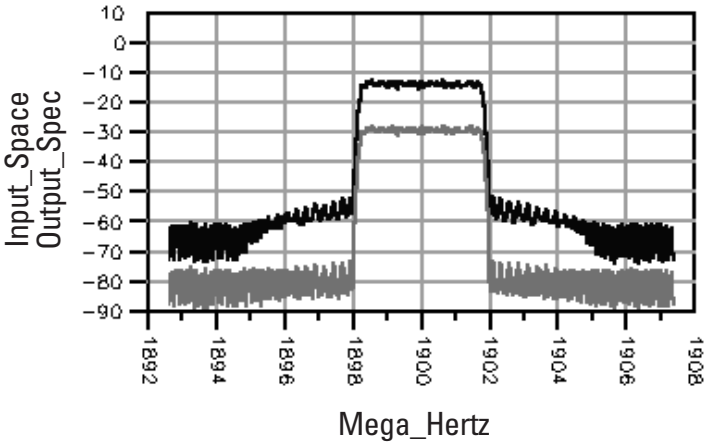


Figure 17. In the example system, the performance effect of the selected driver amp is evaluated by demodulating and decoding the signal output from the upconverter so that the I and Q symbol streams can be analyzed for EVM performance. A spectrum analyzer is connected to the output of the driver amplifier to evaluate its output spectrum.



xIndex	EVM
0.000	0.007

Eqn cable_loss=1.08

Eqn main_ch_power_dBm=spec_power(Output_Spec,1900-3.6864/2,1900+3.6864/2)-cable_loss

Eqn upper_ch_power_dBm=spec_power(Output_Spec,1905-3.6864/2,1905+3.6864/2)-cable_loss

Eqn acpr_upper_dBc=upper_ch_power_dBm-main_ch_power_dBm

main_ch_power_dBm	upper_ch_power_dBm	acpr_upper_dBc
8.967	-38.137	-47.104

Figure 18. These are the simulation results of the overall system with the MGA-72543 circuit model inserted in the top-level design of the example system. The top trace is the output spectrum, while the lower trace is the input spectrum. A small amount of spectral regrowth is exhibited, but ACPR is still better than 47 dB, which satisfies the performance goals for the example system. Also, EVM is only 0.7 percent, indicating that there is negligible distortion to waveform quality.

As further illustration of this bottom-up verification capability, say the critical system metric is BER performance–a non-intuitive specification for the RF designer. In that case, the circuit designer simply inserts an amplifier, oscillator, or mixer design into the top-level system, runs a simulation, and quickly gauges the effect the specific component has on BER performance--long before any hardware is fabricated or assembled.

Test instrumentation verification

With the top-level simulation results in hand, the component that requires evaluation can now be measured on the bench. This stage leverages links between the design software and test instrumentation to provide useful data for prototype hardware verification. In the example system, a link between design software and a signal generator enables the I and Q symbol streams to be fed into the signal generator and then synthesized as a stimulus signal for the driver amp on the bench. This setup is shown in figure 19 and figure 20.

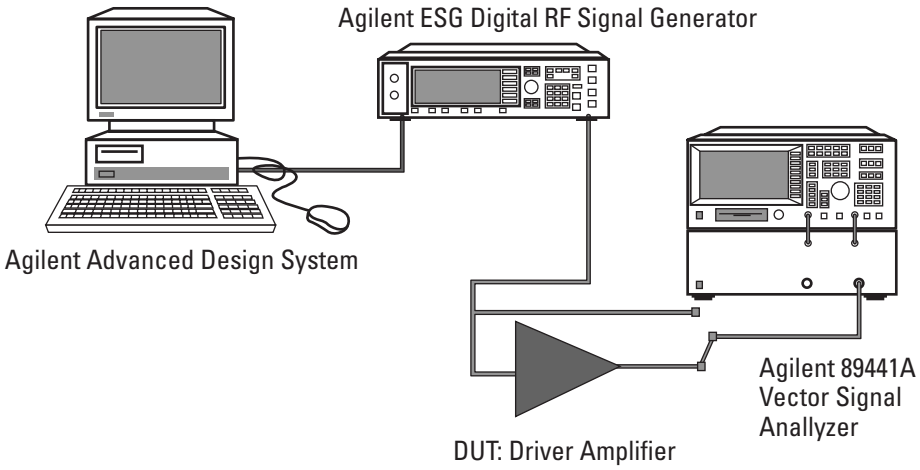


Figure 19. Verification of individual components is greatly simplified using design-to-test links. In the example system, ADS interfaces with the Agilent ESG Digital RF Signal Generator and the results are evaluated using an Agilent 89441A Vector Signal Analyzer. In this example, the signal is a cdma2000 SR3 spectrum.

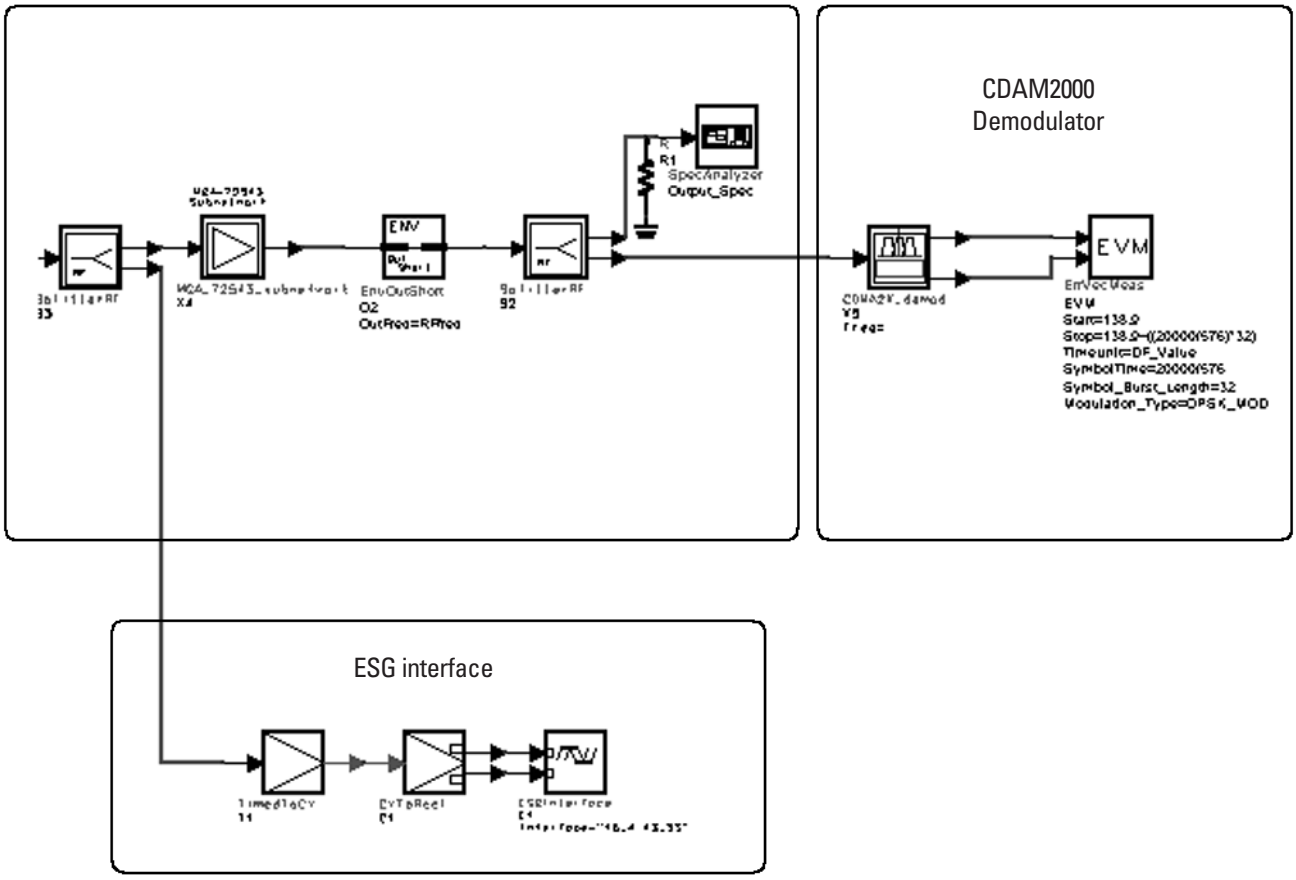


Figure 20. This schematic shows the ADS-to-ESG link in the example component verification. The I and Q symbol streams are created in ADS and sent to the RF signal generator, which synthesizes them and then modulates them onto the carrier to create a cdma2000 digitally-modulated signal. The modulated signal is then passed through the MGA-72543 driver amplifier. In this example, a LAN IP address is specified for the ESG interface. This is facilitated using a GPIB-capable LAN interface box, which gives access to the test equipment over a network–a useful feature for labs where the test equipment must be available as a shared resource.

This reveals one of the key advantages of linking design software to a signal generator. During prototype verification of an individual component, the signal synthesized by the RF signal generator includes any impairments introduced by elements (e.g., mixers, filters, amplifiers, etc.) preceding the device under test. This capability enables designers to generate the actual signal spectrum, including signal distortions that would be present at any point in the system, allowing precise analysis without the need to fabricate or build all of the hardware.

For instance, say a DSP designer wants to evaluate system performance using a proprietary Finite Impulse Response (FIR) filter. This is easily accomplished by replacing the standard baseband filter in the design with a proprietary design and then sending the resulting I and Q symbol streams to the RF signal generator. Furthermore, the link to design software provides the flexibility to generate stimulus signals for emerging standards not yet supported by the RF signal generator.

Finally, the top-level system is evaluated with the selected component inserted (the driver amplifier in the example system). Figure 22 and figure 23 show simulated versus measured results for the example system. Notice that the measured ACPR is still within the 47dB specification. At this point in the design flow, the hardware device is verified to work within specifications for the system-level design. Based on these results, the designer can be confident that the amplifier will function as specified during the system-level integration phase.

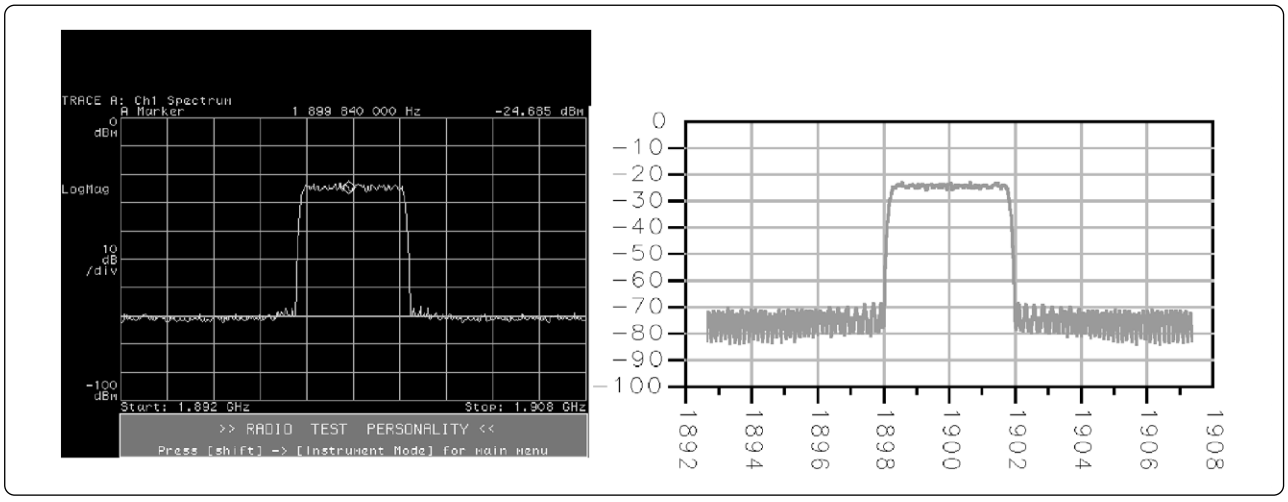


Figure 21. Output spectrum generated by the Agilent ESG RF Digital Signal Generator based on the ADS-ESG link (left), versus the simulated ADS spectrum (right), to be used for input to the MGA-72543. Excellent agreement is exhibited between the spectrums. The spectrum from the ADS-ESG link is measured with a 30 kHz bandwidth using a vector signal analyzer.

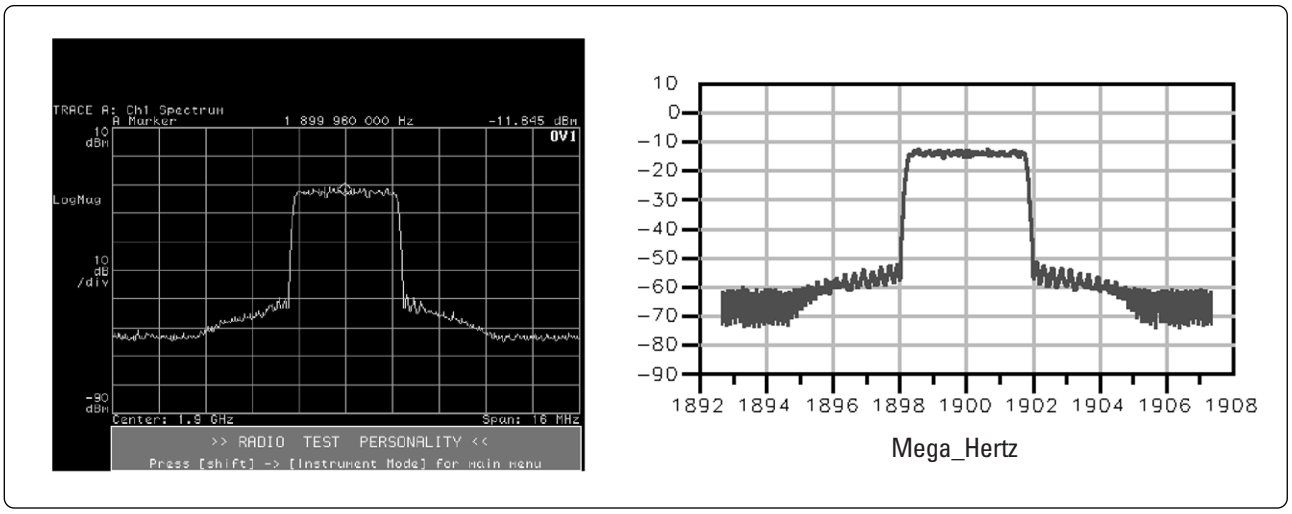


Figure 22. Here is a comparison of the output spectrum from the MGA-72543 (driven by the ADS-ESG link-generated signal) and the simulated ADS output spectrum. Some evidence of spectral regrowth is revealed, which will impact ACPR. Generally, the spectrums are very similar, which shows that the nonlinear circuit model available for the MGA-72543 closely models the actual device performance.

Finally, we'll compare measured and simulated ACPR performance. Superb agreement between the two is shown in figure 23, with an ACPR value of –47 dB.

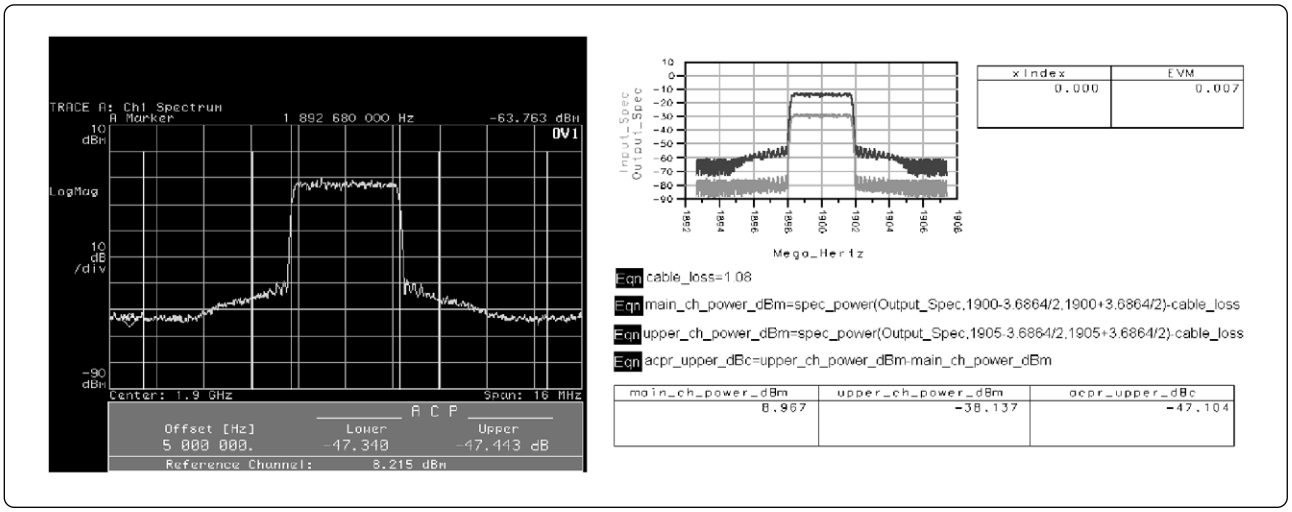


Figure 23. Output spectrum of the MGA-72543 using ADS I and Q.

If the ACPR specification had not been met, several options are available. The designer could compensate for excessive ACPR by tightening specifications for other components in the transmitter chain, selecting another vendor's amplifier, or designing their own. In any case, the decision is made early in the development process, avoiding costly delays. This highlights the real value of bottom-up verification.

Significant future developments are being considered for EDA/instrumentation integration. For instance, time-, frequency-, and modulation-domain analysis capabilities are on the drawing board already.

Other expected enhancements include:

- adding test instrument functions to design software,
- making data displays in software identical to test instruments,
- improving the interoperability of test vectors between design and test,
- integrating test and development strategies, and
- adding 3G interface capabilities.

Conclusions

This application note has shown how links between design software and test instrumentation simplify the ability to make design trade-offs and perform RF/DSP partitioning at the top-level system. Once initial RF and DSP circuit designs are completed, they are inserted in place of behavioral elements in the top-level system and simulated, enabling rapid bottom-up verification of components and sub-systems using measurements such as ACPR, EVM, and BER.

Links between design software and test instrumentation represent an enabling technology for design verification, allowing prototype hardware to be evaluated with arbitrary signals. Using this integrated design software/test hardware capability, new signal formats can easily be synthesized for the device under test, including impairments introduced by upstream components. This enables verification to be performed at every stage of the design process, including the hardware prototype stage. Integrated design and test solutions can speed up development cycles, improve accuracy of designs, and increase engineering productivity.

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