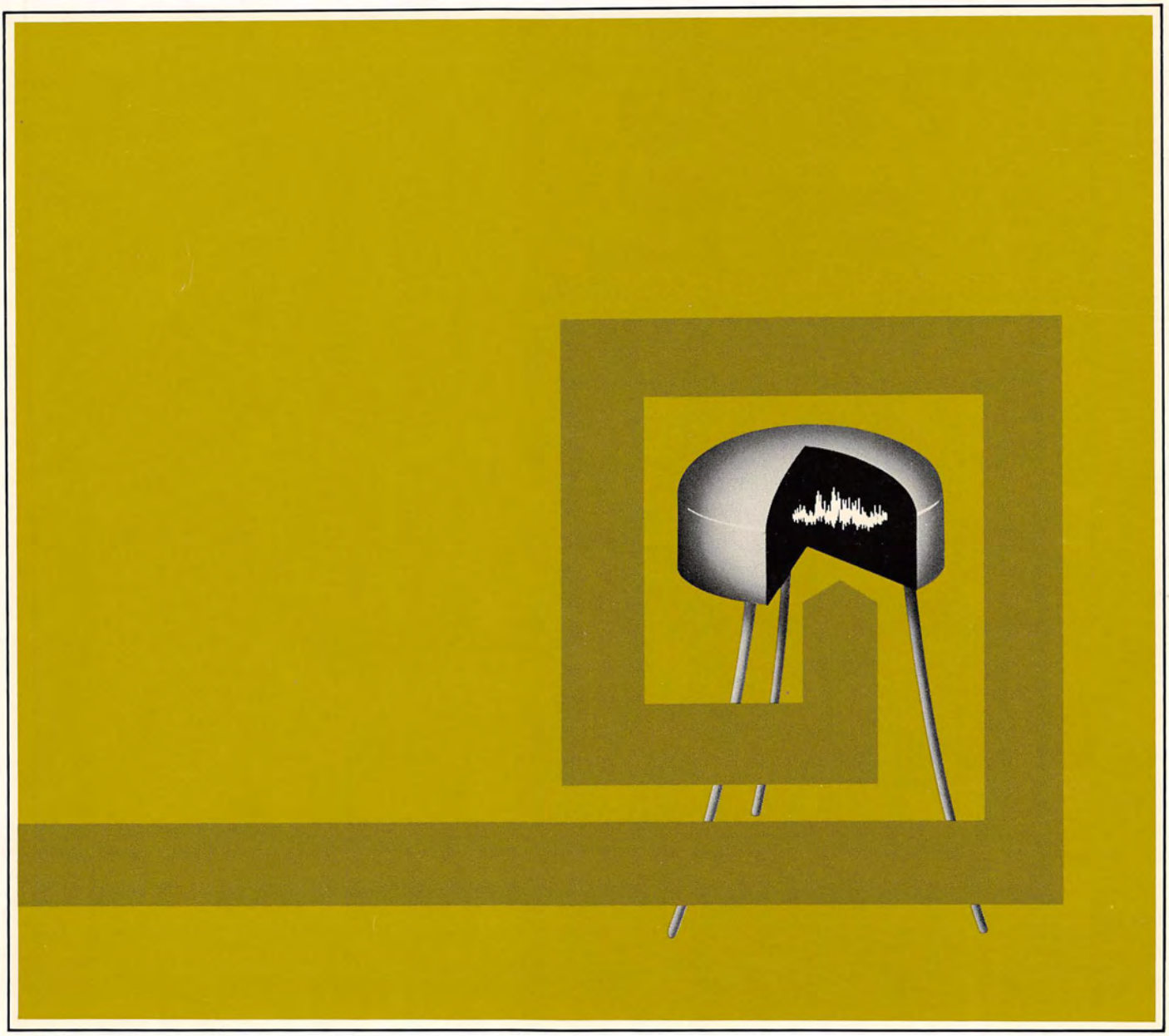
APPLICATION NOTE 137

PROBING TRANSISTOR NOISE



HEWLETT hp PACKARD

PROBING TRANSISTOR NOISE

MAY 1971

BIOGRAPHY

Takayuki Satoh received his BSEE from Hokkaido University in 1961 and joined Yokogawa Electric where he was assigned to oscilloscope development projects. He was transferred to Yokogawa-Hewlett-Packard in 1964, and joined the Model 4470A Transistor Noise Analyzer design group in 1967 where he finished the project as its leader in 1968. Mr. Satoh is continuing work on noise measurement in passive and integrated devices.

Noise Figure (NF) values for transistors can easily lead the circuit designer astray. To accurately characterize transistor noise, the designer must look beyond commonly published NF data - and pay particular attention to the transistor's noise current.

Noise Figure (NF) values, usually included on transistor data sheets, can easily invite incorrect assumptions. For example, a designer needing a low-noise transistor considers two possible candidates with different NF values. One is specified at 5 dB while the other is at a higher 7.5 dB. The NF's for both of these transistors were rated at 100Ω source resistance, 1 mA collector current and at a frequency of 1 kHz. Naturally, the designer concludes that the transistor with the lower NF value (5 dB) is best - and he proceeds to apply it in his design, however, he uses a source resistance of 10 kΩ. On checking, he learns that the selected device yields a NF of 22 dB - while the rejected device yields a much lower NF of 5.5 dB. He rightfully asks, "Of what practical use was the 100Ω noise specification?" and "Why the vast difference between devices?"

These are certainly valid questions. If the confused designer hopes to find the answers and avoid similar mistakes in the future - he will look beyond the NF data sheet and consider other parameters that will help him make the right decision.

NF LIMITATIONS

Although graphs that show NF values as a function of source resistance suggest an easy solution to the designer's device-selection problem, further difficulties in interpretation may be encountered here also.

Shown in Figure 1, the typical NF contour or family of curves poses two potential pitfalls for the designer, namely:

(1) The curve family depicts an average for the transistor type. This means that a given transistor may not lie exactly on the point of interest, nor will a second transistor of the same type necessarily match the first transistor - or the selected point. Thus a transistor yielding an NF value lying on the specified contour at one point, may not fit the contour at any other point.

(2) NF minima on the contours suggest that optimum source resistances and emitter currents are selectable directly from the contours. However, Noise Figure is a relative criterion, where in practice the designer is actually interested in the absolute value of noise performance. Therefore, the minimum noise performance could lie on a different section of the contour.

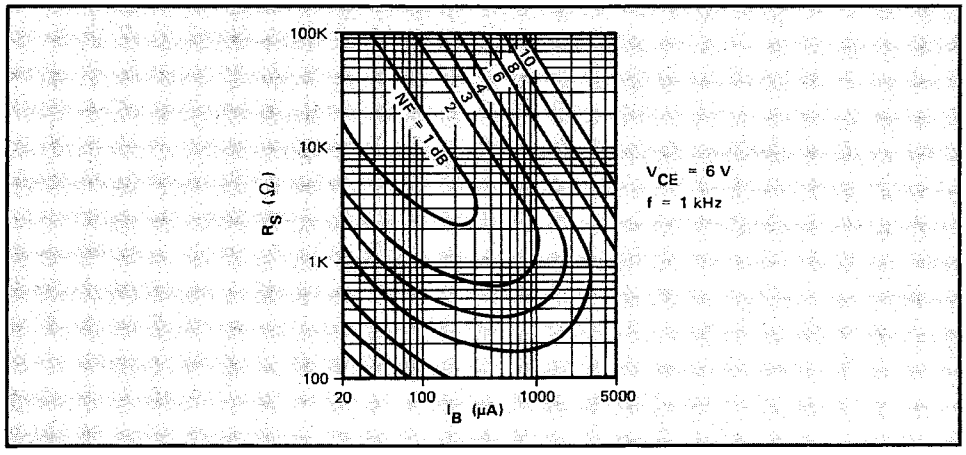


Figure 1 Typical NF contours can be misleading if the designer forgets that the family curves only depict an average for the transistor type. Furthermore, this commonly published NF data easily invites the designer to incorrectly assume that optimum source resistance and emitter currents are selectable directly from the contours.

The difference between relative and absolute noise values is graphically shown in Figure 2 - where total noise is a minimum at the low R_S point A, while point B is where the ratio of the two curves is a minimum (lowest NF).

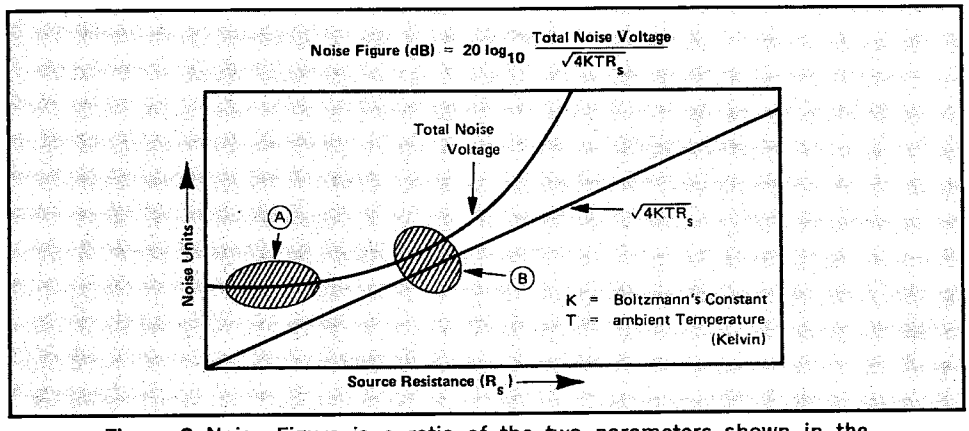


Figure 2 Noise Figure is a ratio of the two parameters shown in the above formula. Selecting a source resistance (R_S) based upon the NF contours in Figure 1 could lead the designer to select a value somewhere in area B when actually he will achieve minimum noise performance if he selects an R_S that lies within area A.

MEASURING UNPREDICTABLE NOISE CURRENT

Getting back to our confused designer - why did the rejected device (NF of 7.5 dB when driven by an R_S of 100Ω) yield a much lower NF than the accepted device when each were driven from an R_S of 10 kΩ? To answer this question, we must analyze the unpredictable "noise current" which behaves differently for each transistor. For a given transistor, the total noise may be expressed as:

$$V_n = (e_n^2 + 4KTR_S + i_n^2R_S^2)^{\frac{1}{2}}$$

where:

V_n = total noise voltage at the input.
e_n = noise voltage referred to the input. } (see Figure 3)
i_n = noise current referred to the input. }
K = Boltzmann's constant (1.38×10^{-23})
T = ambient temperature (Kelvin)
R_S = source resistance (ohms)

It can be readily seen that dependent on values of i_n and R_S, the total noise expression can vary widely from total noise based on e_n only, or on measurements neglecting the i_n contribution.

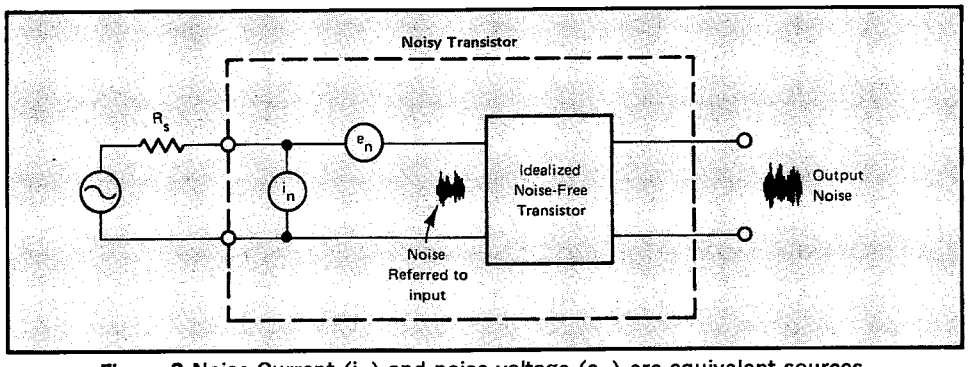


Figure 3 Noise Current (i_n) and noise voltage (e_n) are equivalent sources of noise within a transistor, referred to the input. For measurement of i_n and e_n, the transistor's input should be open and short-circuited, respectively.

The behavior of the three noise components is quite different, and that of noise current, i_n is the most interesting. Generally, for low-noise transistors of the same family, voltage noise, e_n, is fairly predictable and may be assumed constant from one device to the next, and very nearly equal to the calculable theoretical minimum noise. The thermal component, $4KTR_S$, is predictable of course, but the i_n component is not. Noise current values vary widely from device to device and measured values can exceed the predictable minimum by wide margins. Figure 4 depicts the behavior of the three components that make up a transistor's total noise.

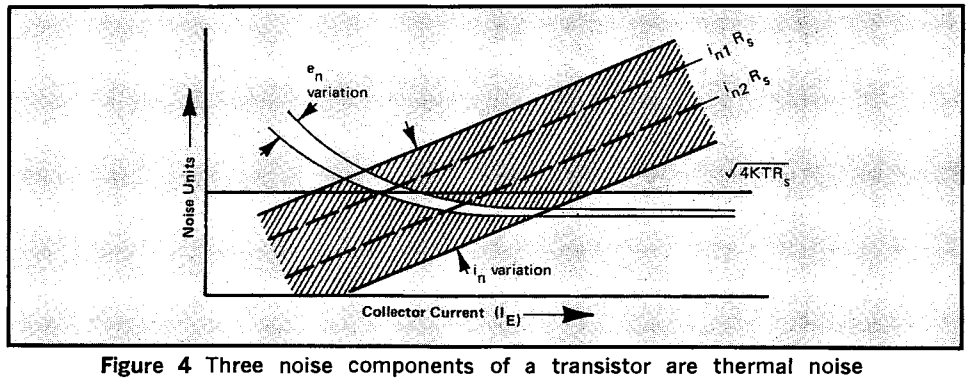


Figure 4 Three noise components of a transistor are thermal noise ($4KTR_S$), noise voltage (e_n) and noise current (i_n). As shown above, $4KTR_S$ and e_n are predictable because their values do not change appreciably from device to device of the same type. However, i_n does vary widely and is therefore unpredictable.

Although transistor noise measurement has been traditionally associated with NF and noise-voltage testing, measurement of i_n is by far the most useful. Noise current values provided accurately and without calculation can significantly aid the circuit designer in maximizing the performance of low-noise transistors in given applications. The measurement of i_n, as performed by Hewlett-Packard 4470A/B Transistor Noise Analyzer is illustrated in Figure 5.

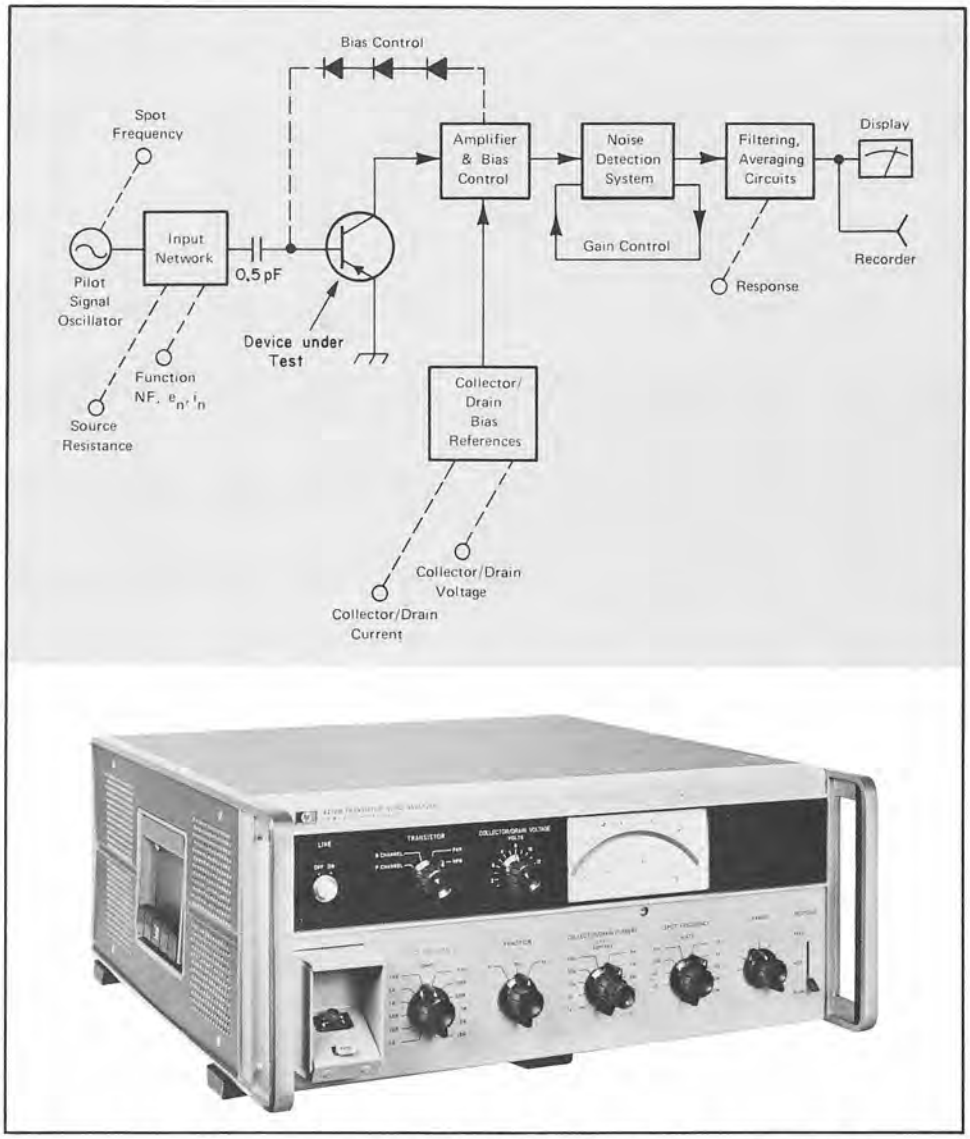


Figure 5 Transistor Noise Analyzer (HP 4470B) gives direct readings of NF, e_n and most importantly, i_n - thus giving complete device noise performance. Measurements are made within a 4 Hz bandwidth at 9 spot frequencies between 10Hz and 100kHz.* The block diagram depicts the major functional elements of the 4470A/B; its operation can be briefly described as follows: Given that i_n is the noise generator seen effectively at the transistor input under open-circuit conditions, a unique biasing and input-impedance control system provides signal input and operating voltage to the device under test at selectable frequencies. The diode chain provides positive and negative bias values for both device polarities while maintaining input impedance at relatively high values. The signal is injected at the 0.5 pF coupling capacitor by the pilot oscillator, which in the i_n measuring mode is seen by the device under test as a high-impedance constant-current generator. Stray capacities are minimized at the input and transistor socket of the analyzer.

*(4470A has 11 spot frequencies between 10 Hz and 1 MHz).

TOTAL NOISE IN AN AMPLIFIER CHAIN

Total noise contribution of an amplifier chain will normally be of greatest interest to the circuit designer. The individual noise contributions of each transistor within an amplifier chain may be measured or derived in terms of e_n and i_n and total noise performance predicted for the overall circuit. Normally, in low-noise circuit design the input stage of a simple, cascaded amplifier will be of most importance due to the amplifying effects of succeeding stages (see Figure 6). To minimize the noise contribution of this input stage it is essential to make an optimum low-noise transistor selection.

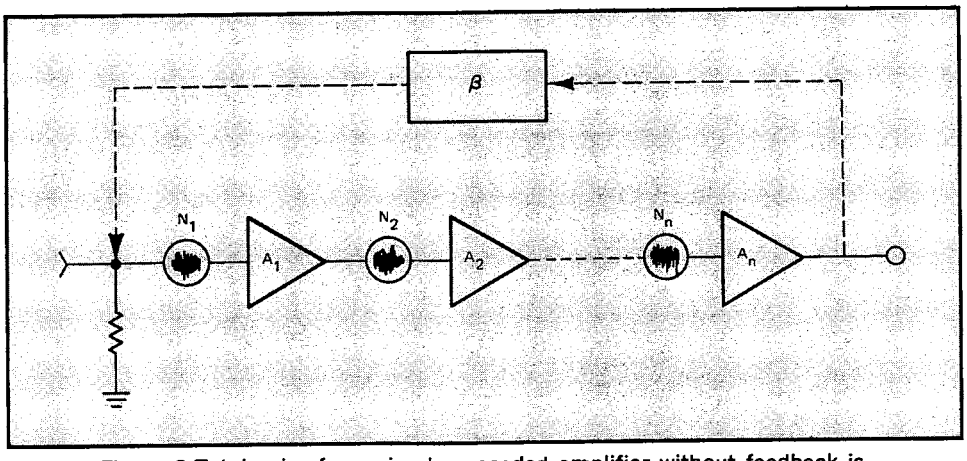


Figure 6 Total noise for a simple cascaded amplifier without feedback is given by:
$N_t = [(N_1A_1A_2 \ldots A_n)^2 + (N_2A_2A_3 \ldots A_n)^2 + \ldots + (N_nA_n)^2]^{\frac{1}{2}}$
Minimizing the noise of the input stage is essential to achieve low-noise performance because of the input stage's amplifying effects on succeeding stages.

Total noise-voltage spectral density referred to the input of an amplifier is:

$$\left[N_1^2 + \frac{N_2^2}{A_{v1}^2} + \frac{N_3^2}{(A_{v1}A_{v2})^2} + \cdots\cdots + \frac{N_i^2}{(A_{v1}A_{v2} \cdots A_{vi})^2}\right]^{\frac{1}{2}}$$

where N_i is the total noise voltage spectral density due to the ith stage referred to its input and with the source impedance it sees in the circuit. A_{vi} is the voltage gain of the ith stage. Traditionally, maximizing A_{v1} has been accepted as the most direct route to minimizing the contribution of the second term, N_2/A_{v1} but the second stage input noise voltage spectral density, N_2, can be expressed as:

$$N_2 = (4KTR_{L1} + e_{n2}^2 + i_{n2}^2R_{L1}^2)^{\frac{1}{2}} \cdot \frac{R_{in2}}{R_{L1} + R_{in2}}$$

where R_{L1} = collector resistance of first stage
R_{in2} = input resistance of second stage
e_{n2} = noise voltage of second stage
i_{n2} = noise current of second stage

And if i_{n2} is large, the $i_{n2}^2R_{L1}^2$ term becomes most significant, and the other two terms are negligible by comparison, thus:

$$N_2 = (i_{n2}R_{L1}) \frac{R_{in2}}{R_{L1} + R_{in2}} \quad \text{and} \quad \frac{N_2}{A_1} = \frac{(i_{n2}R_{L1}) \dfrac{R_{in2}}{R_{L1} + R_{in2}}}{gm \cdot \dfrac{(R_{L1})(R_{in2})}{R_{L1} + R_{in2}}}$$

Thus, minimizing second-stage noise current can be more useful than increasing first-stage gain.

MINIMIZING NOISE BY SELECTION

After determining what parameters must be fixed for a particular design, the wise designer will carefully select the variable parameters so as to minimize the transistor's total noise. Following are three possible cases that a designer might encounter:

CASE A: Fixed Source, Selectable Currents

Given a specific value of source resistance, the transistor user may be free to select or optimize values of emitter/collector current. To do so, values of e_n and i_n describing the device under consideration can be extremely useful. The plots of $i_n R_s$, e_n and thermal source noise in Figure 7a for a PNP silicon device shows the criteria for selection in this case.

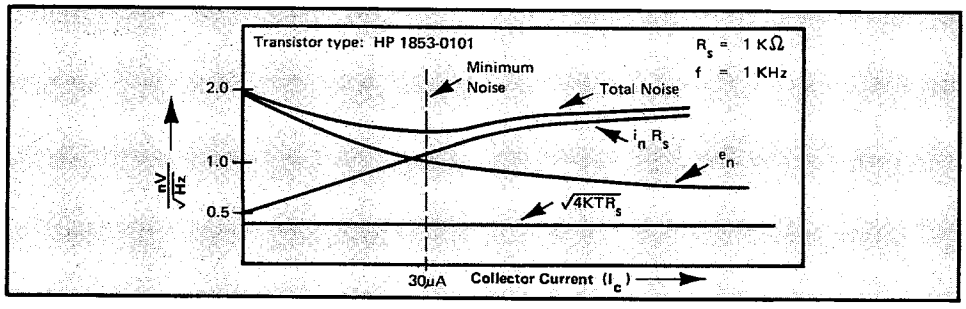


Figure 7a Optimum collector current can be selected, given sufficient e_n and i_n data. Total noise for a transistor is $e_n^2 + i_n R_s + 4KTR_s$.

CASE B: Fixed Current, Selectable Source Resistance

Selection of optimum source resistance is often a function of other considerations namely stability, biasing requirements, and impedance matching, but the obvious benefits of a minimum R_s are shown in Figure 7b. Note that if the i_n data had been neglected, a higher resistance value would be selected and a higher resultant noise value designed into the circuit.

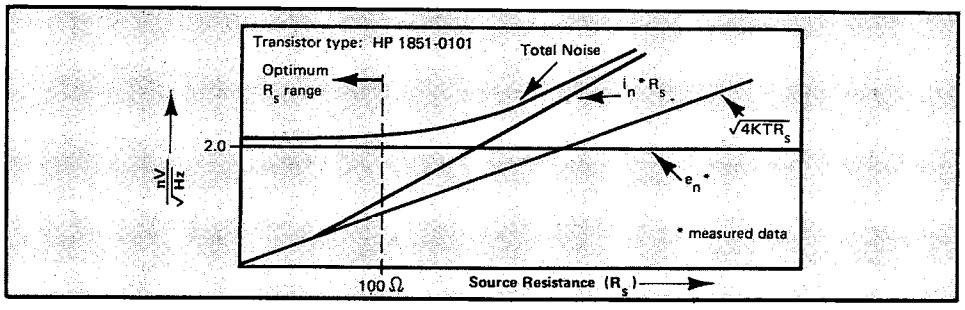


Figure 7b Optimum source resistance is 100Ω or less as determined from data read with the 4470B analyzer.

CASE C: Selectable Current and Source Resistances

Given that any values of source resistance and collector current are usable for a given design, optimum low-noise device selection can be made by an iterative process of two or three steps. Given a potentially usable transistor, a plot of voltage noise is obtained, providing a "ball-park" value for current selection, as in Figure 7c. Using the

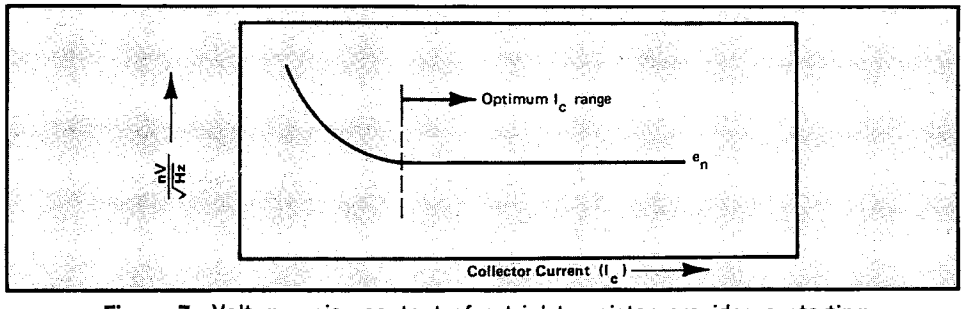


Figure 7c Voltage noise content of a trial transistor provides a starting point for optimum selection of both collector current and source resistance.

value of collector current selected, the process of CASE B is developed, in R_S (measured at the collector current value selected above) and $4KTR_S$ are plotted as functions of R_S. This provides a reasonable fix on R_S. This value of R_S is used (as in the "fixed source" CASE A) to further optimize current, and the two parameters are stabilized at an optimum point. Normally, in selecting a specific transistor from a batch of the same type, the aggregate of thermal and voltage noise will remain fairly constant, and measured values of i_n will be seen to vary widely. Rapid selection is thus enabled through a single current value (see Figure 4).

TEST CIRCUIT AIDS RAPID SELECTION

To facilitate rapid selection of low-noise transistors for a particular application, a test circuit can be quite useful. The test circuit shown in Figure 8 was used to rapidly check the low-noise performance of transistors for the typical design example (see boxed information).

In the Figure 8 test circuit, Q1 is the transistor being checked for its contribution to the amplifier's output noise. Amplifier gain from Q1 input through Q2 output is 4000; noise contributed by Q2 is negligible, and the true rms voltmeter indicates total noise across the amplifier band.

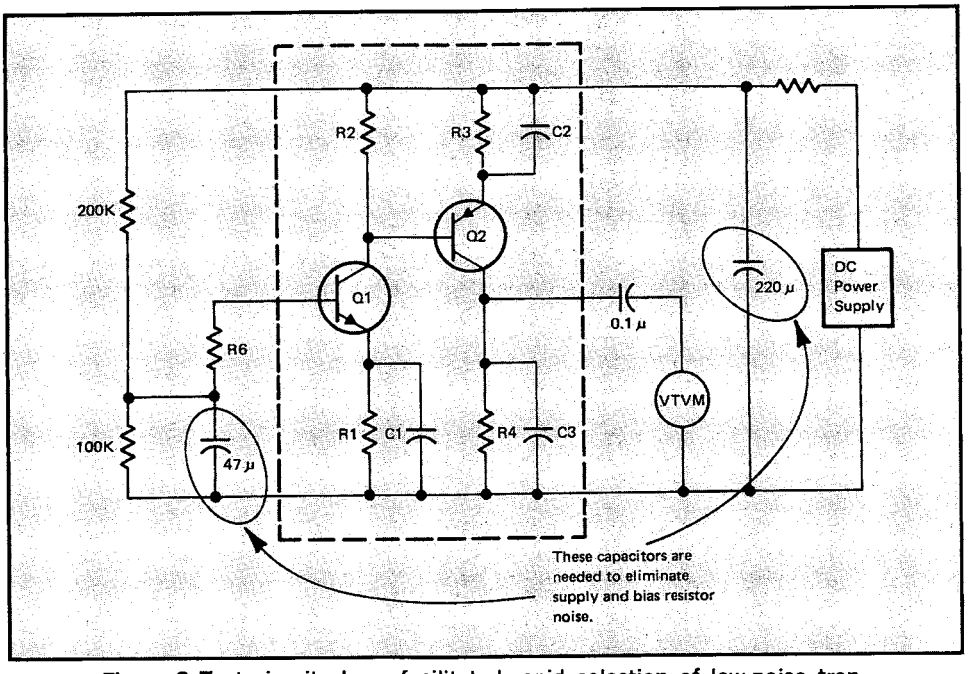


Figure 8 Test circuit above facilitated rapid selection of low-noise transistors for the application discussed boxed information titled "Typical Design Example."

Five samples of the same transistor type, randomly selected, were checked in the test circuit. The readings obtained were:

Sample No.:	1	2	3	4	5
Amplifier Output Noise:	5.1 mV	6.3 mV	4.0 mV	6.8 mV	4.6 mV

It was concluded that only two of the five devices met the design requirement, namely samples No. 3 and No. 5. It is also noteworthy that no two values were the same. NF tests made on all five devices at the specified 500Ω, 1 kHz and 1 mA yielded 3 dB readings for all five devices. The more practical differences in actual noise contribution in the above readings are due to the varying noise current contribution at the 10 kΩ source resistance.

In the typical design example, source resistance was given - however, there was no constraint placed on the collector current. Therefore we may vary the collector current to further reduce the total noise of the selected transistor type.

Following the techniques discussed under CASE A earlier, measurements of e_n and i_n were made on the five test transistors, and plotted. The results are shown in Figure 9. As expected, samples No. 3 and No. 5 gave best results, and the differences in total noise from device to device correlated directly with the differences in noise current. By inspection, the optimum collector current for low-noise performance ranged from 10 μA through 100 μA. A value of 75 μA was tried, and all five devices gave test circuit results below the 5 mV requirement.

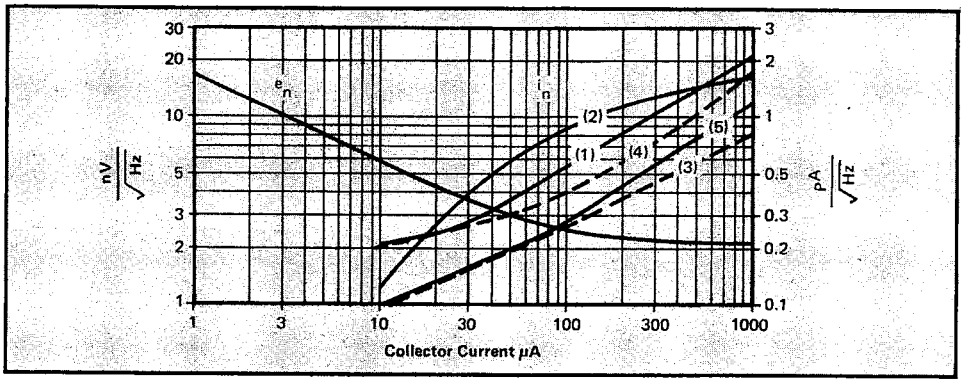


Figure 9 e_n and i_n are plotted for five devices of the same type. This data graphically emphasizes the wide variation of i_n from device to device - while e_n on the other hand, remains relatively constant for each device.

Assuming that source resistance could also be made selectable, the 10 kΩ value was discarded and noise performance further optimized by selecting the best source resistance value. Using the techniques of CASE B, a value of 300Ω for source resistance was found to give a total noise for all five devices of less than 1 mV!

DATABANK

1) "Direct Measurement of Transistor Noise Voltage, Noise Current and Noise Figure" by Haruo Itoh and Knud L. Knudsen.
2) "Sources of Noise in Transistors" by Nilardi R. Mantena.
Both of the above articles appear in the Hewlett-Packard Journal, October 1969.

TYPICAL DESIGN EXAMPLE

Optimizing an amplifier design for low-noise performance is best shown through an example. Consider the following:

A transistor is to be selected for use in an amplifier operating over a power bandwidth of 300 Hz to 2 kHz. Maximum noise output over this range should not exceed 5 mV rms maximum. The amplifier should provide a voltage gain of 4000 and will be driven from a 10 kΩ source. The available transistor has the following published specifications:

$$V_{CEO} = 30\ V$$
$$h_{FE} = 500, I_E = 1\ mA$$
$$NF = 4\ dB\ (I_E = 1\ mA,\ f = 1\ kHz, R_s = 500\Omega)$$

The 10 KΩ NF value is checked at the nominal value of 1 mA on the NF contours and is found to be about 5 dB, and is quickly checked on a transistor noise analyzer at approximately 6 dB. Using the 6 dB measured value, the rms output voltage over the required bandwidth is calculated:

(a) Spot Noise:

Since $NF = 20 \log_{10} \dfrac{\text{Noise Voltage Spectral Density}}{\sqrt{(4KTR_S)}}$

$= 6$ dB, or a voltage ratio of 2.

$\sqrt{(4KTRs)} = \sqrt{4 \times 1.38 \times 10^{-23} \times 293^\circ \times 10\ k\Omega}$

$= 12.6\ nV/\sqrt{Hz}$

Total Spot Noise $= 12.6\ nV \times 2$

$= 25.2\ nV/\sqrt{Hz}$

(b) Total Noise, 300 Hz to 2 kHz:

Total noise $= \sqrt{(2\ kHz - 300\ Hz)} \times 25.2\ nV/\sqrt{Hz}$

$= 41.2 \times 25.2\ nV$

$= 1\ \mu V$

Since this is total noise referred to the transistor input, output noise is determined by multiplying by the gain requirement, $4000 \times 1\ \mu V = 4$ mV.

The selected device, then is apparently adequate for the task.

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