Low-Voltage Differential Signaling (LVDS)

Application Note 1382-6

by Stephen Kempainen, National Semiconductor

Who Should Read This Application Note?

Digital designers utilizing low-voltage differential signaling (LVDS) for high-speed data transmissiom.

LVDS Provides Higher Bit Rates, Lower Power, and Improved Noise Performance

Due to the Internet's tremendous growth, data transfers are increasing dramatically in all areas of communications. In addition, data streams for digital video, HDTV, and color graphics are requiring higher and higher bandwidth. The digital communications deluge is the driving force for high-speed interconnects between chips, functional boards, and systems. The data may be digital, but it is analog Low-Voltage Differential Signaling (LVDS) that designers are choosing to drive these high-speed transmission lines. LVDS's proven speed, low power, noise control, and cost advantages are popular in point-to-point applications for telecommunications, data communications, and displays. LVDS uses high-speed analog circuit techniques to provide multi-gigabit data transfers on copper interconnects.

Wherever you need high-speed data transfer (100 Mb/s and higher), LVDS offers a solution. There are many applications in many market segments that use LVDS for data transmission. These include:

- stackable hubs for data communications
- wireless base stations and ATM switches in telecommunications
- flat-panel displays and servers in the computer market
- peripherals like printers and digital copy machines
- high-resolution displays in industrial applications
- flat-panel displays in the automotive market

In these applications, high-speed data moves within and between systems. Moving data within a system (intrasystem data transfer) is the main use for LVDS solutions today. Moving information between systems (intersystem data transfer) requires standard communication protocols such as IEEE 1394, Fibre Channel, and Gigabit Ethernet. Since the hardware and software overhead for intersystem protocols is too expensive to use for intrasystem data transfers, a simple and low-cost LVDS link is an attractive alternative. Thus, LVDS solutions move information on a board, between boards, modules, shelves, and racks, or box-to-box. The transmission media can be copper cables or printed circuit board (PCB) traces. In the future, LVDS will also carry protocols for inter-system communication.

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Generic LVDS

Low-voltage differential signaling is a generic interface standard for high-speed data transmission. The ANSI/TIA/EIA-644-1995 standard specifies the physical layer as an electronic interface. This standard defines driver and receiver electrical characteristics only. It does not define protocol, interconnect, or connector details because these details are application specific. The LVDS Standard's Working Group chose to define only the electrical characteristics to ensure that LVDS becomes a multipurpose interface standard. Therefore, each application that uses LVDS should also reference the appropriate protocol and interconnect standard.

The equivalent circuit structure of the LVDS physical layer is shown in figure 1. In the driver, a current source limits output to about 3 mA, and a switch box steers the current through the termination resistor. This differential driver produces odd-mode transmission: equal and opposite currents flowing in the transmission lines. The current returns within the wire pair, so the current loop area is small, and therefore generates the lowest amount of EMI (electro-magnetic interference). The current source limits any spike current that could occur during transitions. Because there are no spike currents, data rates as high as 1.5 Gb/s are possible without a substantial increase in power dissipation. In addition, the constant current driver output can tolerate transmission lines shorted together, or to ground, without creating thermal problems.

The differential receiver is a high-impedance device that detects differential signals as low as 20 mV and then amplifies them into standard logic levels. The signal has a typical driver offset of 1.2 V, and the receiver accepts an input range of ground to 2.4 V. This allows rejection of common-mode noise picked up along the interconnect of up to ±1 V.

In addition, hot plugging of LVDS drivers and receivers is possible because the constant current drive eliminates damage potential. Another feature is the receiver's failsafe function, which prevents output oscillations when the input pins are floating.

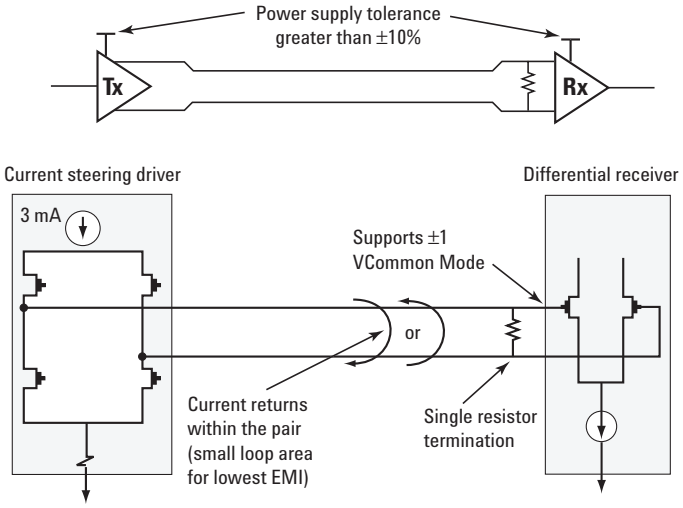

Figure 1. The equivalent circuit structure of the LVDS physical layer.

Multiple Technologies and Supply Voltages

When choosing the signal-level voltages for drivers and receivers, the standards committee considered LVDS implementation in technologies such as Bipolar, BiCMOS, CMOS, and even GaAs. In addition, the working group targeted a wide range of power supplies (such as 5 V, 3.3 V, and 2.5 V) for implementing LVDS, to ensure that LVDS would be the interface of choice for future generations of products.

Low-voltage signals have many advantages, including fast bit rates, lower power, and better noise performance. Design engineers have previously used full-swing CMOS and LVTTL (low voltage transistor-transistor logic), but as bit rates increase, these solutions become unattractive. More recently, designers have turned to reduced-swing technologies such as SSTL and GTL to gain speed, save power, and reduce noise. LVDS increases these advantages by lowering voltage swings to about 300 mV. To increase noise immunity and noise margins even further, LVDS uses differential data transmission. Differential signals are immune to common-mode noise, the primary source of system noise. Because its voltage change between logic states is only 300 mV, LVDS can change states very fast. An LVDS signal also changes voltage levels without a fast slew rate. Slowing the transition rate decreases the radiated field strength. Slower transitions reduce the problem of reflections from transmission-path impedance discontinuities, decreasing emissions and crosstalk problems. Low voltage swing reduces power consumption because it lowers the voltage across the termination resistors and lowers the overall power dissipation.

The diagram in figure 2 emphasizes the advantage of a low voltage swing for higher performance. For example, when the signal level changes 300 mV in 333 ps, the slew rate is only 0.9 V/ns, which is less than the 1 V/ns benchmark slew rate commonly acceptable for minimizing signal distortion and crosstalk. If you use the old benchmark that the rise and fall times should be no more than two thirds of the bit width, then signals with 333-ps transitions can operate as high as 1 Gb/s with plenty of margin.

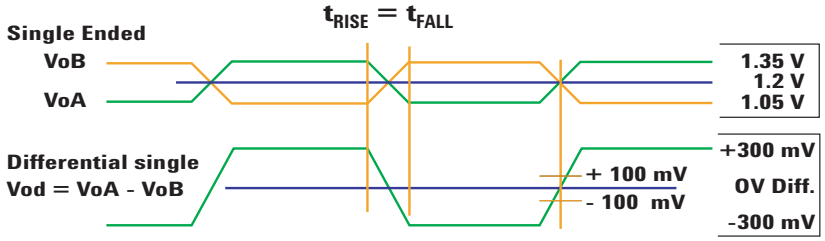

Figure 2. The lowered voltage swing maintains high speed without excessive slew rate.

Gigabits at Milliwatts

The simple phrase “Gigabits at milliwatts!” conveniently describes the benefits of an LVDS system. These benefits are high-speed data throughput, power-miser operation, noise control, low cost, and higher integration.

LVDS system features, such as serializing data, encoding the clock, and low skew, all work together for higher performance. Skew is a big problem for sending parallel data and its clock across cables or printed circuit board traces. The problem is that the phase relation of the data and clock can be lost due to different travel times through the link. However, the ability to serialize parallel data into a high-speed signal with embedded clock eliminates the skew problem. The problem disappears because the clock travels with the data over the same differential pair of wires. The receiver uses clock and data recovery to extract the embedded clock, which is phase aligned to the data.

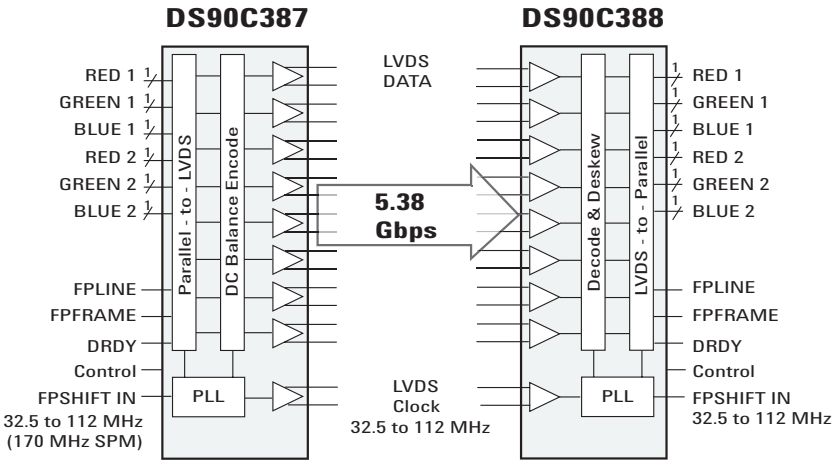

Figure 3. The OpenLDI (Open LVDS Display Interface) chipset is an example of LVDS’s high performance.

An example of LVDS’s high performance is the OpenLDI (Open LVDS Display Interface) chipset that supports 24-bit color and provides throughput of over 5 Gb/s using only 8 data pairs and a clock pair (figure 3). The chipset serializes a 48-bit TTL interface down to the 8 pairs and then deserializes it at the receiver. The chipset supports TTL clock rates up to 112 MHz. To do this, each LVDS data channel serializes 6 TTL lines, plus a DC balance bit, into a single high-speed LVDS pair. That pair operates at 784 Mb/s with a data throughput of 672 Mb/s. The OpenLDI chipset can also operate at TTL bit rates as low as 33 Mb/s.

Gigabits at Milliwatts (continued)

Besides giving tremendous throughput, the chipset reduces the interconnect width and provides other system benefits. The cable and connector are smaller and lower cost; the cable is more flexible, and the connector has fewer pins.

The beautiful eye pattern in figure 4 is taken at the end of a 5-meter cable between the transmitter and receiver of the OpenLDI chipset. The transmitter drives a Pseudo Random Bit Sequence through the cable, and the receiver recovers the signal. The markers show the bit width to be 1.275 ns, indicating a data rate of 784 Mb/s. Each of the 8 pairs carries this raw data rate, resulting in an aggregate bandwidth of almost 6.3 Gb/s. This data rate includes overhead for DC balance, so the actual payload bandwidth is 5.38 Gb/s.

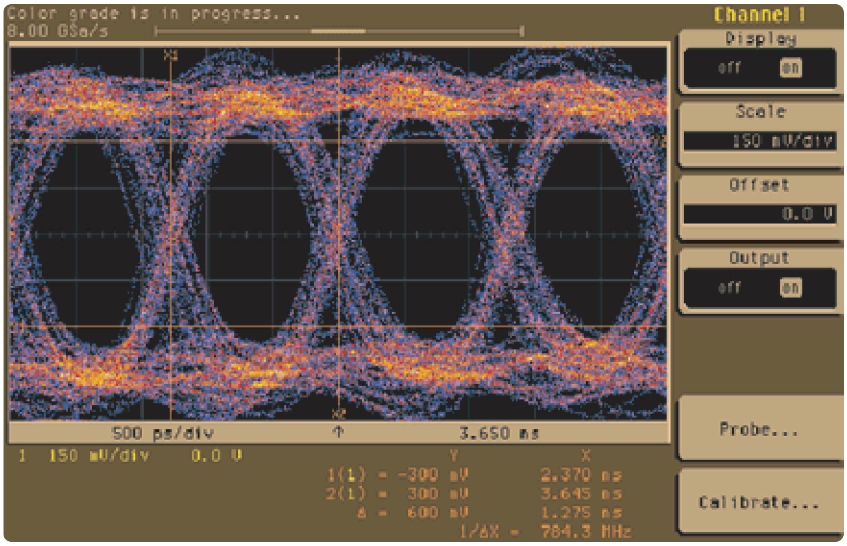

Figure 4. Eye pattern measured at the end of a 5-meter cable between the transmitter and receiver of the OpenLDI chipset.

Flat Supply Current vs. Operating Frequency

A significant advantage of LVDS technology is the lower power requirement. The graph in figure 5 shows LVDS's supply current remaining flat as the operating frequency increases, whereas the supply current for CMOS and GTL (gunning transistor logic) technology increases exponentially as frequency increases. LVDS benefits because it uses a constant-current line driver rather than a voltage-mode driver.

The load power calculation (3.3 mA times the 330-mV drop across the 100-Ω termination resistor) means LVDS has only 1.1-mW load power consumption. By comparison, GTL consumes 40 mA of load current through a 1 V drop across the load resistor, which is a whopping 40-mW load power dissipation. LVDS also has low power requirements compared to Pseudo ECL (PECL). The DS90CO31 is an LVDS pin-compatible replacement part for the Pseudo ECL 41L Quad Differential Line Driver. The LVDS part consumes 16 times less supply current than the PECL part (3 mA compared to 50 mA). Furthermore, the low power consumption inherent in LVDS technology eliminates the need for either heat sinks or special packaging. This benefit also reduces the system cost of gigabit data transfers.

Another advantage of LVDS is its low electromagnetic-interference (EMI) generation. The reasons LVDS generates low emissions are its low voltage swing, slow edge rates, the odd-mode differential signals, and the minimal I_{cc} spikes from constant current drivers. High-frequency signal transitions flowing through a transmission path create electromagnetic fields that radiate emissions. The field's strength is proportional to the energy carried by the signal. By reducing the voltage swing and the current energy, LVDS minimizes these fields. However, even the reduced electromagnetic fields can cause radiation problems.

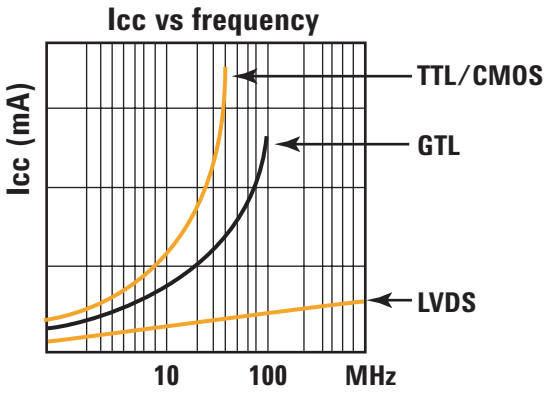

Figure 5. LVDS's supply current remains flat as the operating frequency increases.

Low Electromagnetic Interference

Differential signal paths reduce the harmful effects of these fields to further minimize these radiation problems. Balanced differential lines have equal but opposite currents, called odd-mode signals. When the fields created by these odd-mode signals are closely coupled, they tend to tie each other up and thus cannot escape to cause harm. Therefore, it is important to maintain a balanced and closely-coupled differential transmission path to reduce emission of electromagnetic interference. Differential signals also have the advantage of tolerating interference from outside sources such as inductive radiation from electric motors or crosstalk from neighboring transmission lines. When the differential transmission lines are closely coupled, the induced signal is common-mode noise that appears as a common-mode voltage at the receiver input. The differential receiver responds only to the difference between the plus and the minus inputs, so when the noise appears commonly to both inputs, the input differential signal amplitude is undisturbed. This common-mode noise rejection also applies to noise sources such as power supply variations, substrate noise, and ground bounce.

The LVDS flat panel display (FPD) Link standard shown in figure 6 demonstrates the low noise-generation characteristics for LVDS while targeting LCD applications for notebook and sub-notebook computers. The FPD link moves large amounts of display data from the notebook PC to the display panel. The system designers had to solve the problem of twisted-pair cables or flex circuit carrying high-speed data through the panel hinge without creating EMI problems. They chose to use LVDS technology because it has better EMI performance than all other interface technologies.

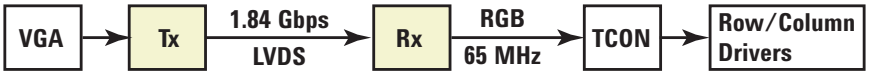

Figure 6. The LVDS Flat Panel Display Link moves large amounts of data from the notebook PC to the display panel.

Cost Benefits

All of the LVDS advantages discussed so far also benefit system cost. There are even more system cost savings from using LVDS. The first is LVDS's ability to tolerate minor impedance mismatches in transmission paths. As long as the differential signal passes through balanced discontinuities in closely coupled transmission paths, the signal can maintain integrity. The effect of non-impedance-controlled connectors, printed circuit board vias, and chip packaging is not as detrimental to differential signals as it is to single-ended signals. In addition, it is possible to use fewer circuit board layers because of the relative immunity to crosstalk that is inherent in differential signals.

LVDS requires only a simple termination resistor, which can be integrated onto the chip. This costs much less than using multiple resistor and capacitor components for each transmission line. In addition, LVDS requires no termination or V_{ddq} voltage supply, a big cost savings over technologies such as GTL, LVTTL, and SSTL.

Because LVDS is capable of handling the high-speed data that results from serializing many parallel bits into a single data stream, LVDS chips commonly integrate serializers and deserializers. This saves about 50 percent of the cabling, connector, and printed circuit board costs when compared to a parallel interconnect. The FPD-Link chipset demonstrates this system cost savings. The chipset takes the 18- or 24-bit-wide RGB (Red/Green/Blue) bus and the VSYNC, HSYNC, and Data Enable control lines and multiplexes them down to only 4 or 5 pairs. This low-cost 4- or 5-pair link passes data through the hinge to the panel where it is demultiplexed. Typical interconnects range from about 8 cm to 40 cm in length and use low-cost flex circuit or twisted-pair cabling.

The final LVDS system benefit is its integration capability. Because it is possible to implement high-speed LVDS in a standard CMOS process, integrating complex digital functions with LVDS's analog circuits is very beneficial. Integrating serializers and deserializers is only the beginning to mixed-signal LVDS chips.

Many Channels per Chip

LVDS's low power consumption enables integrating many channels per chip. For example, it is possible to serialize a 128-bit, on-chip parallel bus down to 8 differential channels. This narrower link dramatically reduces pin count and total link cost.

Integration also benefits from differential signals. These signals tolerate high levels of switching noise, so they can be reliably integrated with large-scale digital circuits. In addition, LVDS generates very little noise due to the constant-current nature of the output structures. Therefore, complete interface Systems-on-a-Chip are feasible. Digital blocks for integration include DC balance, clock embedding, clock recovery, encoders and decoders, and de-skew blocks. Higher-level digital functions such as hardware protocol assist, management and statistics counters, and routing decision logic are also using LVDS on-chip as the interface of choice. Further integration of the blocks shown in the FPD-Link chipset (figure 6) is already happening. Obvious candidates for integration are the LVDS transmitter with the VGA (video graphics adapter) controller and the LVDS receiver with the timing controller.

The OpenLDI chipset supports cable lengths up to 10 meters by integrating special functions. These functions are transmitter pre-emphasis, DC balance coding, and cable deskew. They all work to extend the reach and bandwidth of OpenLDI interconnects to flat-panel-monitor applications that may require longer cables.

DC Balance for Longer Cables

The OpenLDI chipset implements a simple DC balancing scheme that reduces inter-symbol interference (ISI). This demonstrates integrating digital functions onto the same chip as the LVDS interface. Without DC balance, a long cable can result in ISI for a single bit transition and cause a bit error. This happens because a single bit transition, after a long string of no transitions, may not contain the energy necessary to change the stored charge through the entire cable. The term "disparity" describes the stored charge on the cable. If the disparity magnitude is large, then the single bit transition cannot overcome the inter-symbol interference at the end of the cable. The OpenLDI part provides DC balance on a frame-by-frame basis. During the frame, the transmitter monitors the input signal for transitions. If no transitions occur, the transmitter inverts the next frame to maintain balanced cable charge, thus keeping the disparity between plus 10 and minus 9. The 7th LVDS data bit indicates whether the data in the payload is "true" or "inverted".

This simple DC balance scheme keeps the signal eye diagram wide open at the receiver end. In addition, it provides enough DC balance to satisfy fiber-optical interconnect requirements, allowing the OpenLDI chipset to interface with standard parallel fiber-optical products.

Another integrated enhancement to the OpenLDI chipset is the transmitter pre-emphasis feature. Without pre-emphasis, the signal coming out of a cable loses the sharp transition edges due to the cable's high-frequency filter effect. With pre-emphasis, the driver accentuates the transitions to compensate for the filter effect at the end of the cable.

The pre-emphasis feature is user selectable. When pre-emphasis is selected, the transmitter has two current drive levels. It delivers additional dynamic current during transitions to overcome the cable's filtering, and supplies a lower drive current after the transition. It opens the signal eye diagram by overcoming cable distortion of the signal.

LVDS is now spawning follow-on technologies that expand its applications. The first follow-on is Bus LVDS, which allows the low-voltage differential signals to work in bi-directional and multi-drop configurations. Another LVDS derivative, ground referenced LVDS (GLVDS), is progressing through the standardization process. GLVDS moves the differential signal's common-mode voltage close to ground, which allows chips operating from very low supply voltages to communicate over a high-speed standard interface.

Bus LVDS

A review of bus topology helps in understanding the development of Bus LVDS (BLVDS), the first offspring of LVDS. The top two buses in figure 7 show multidrop configurations. The top configuration is unidirectional because there is a single driver at one end of the bus. This simple multidrop bus requires only a single termination that is on the opposite end of the bus from the driver, to stop reflections of the driven signal. Each of the attached receivers reduces the loaded bus impedance. The loading amount depends on the connector, vias, packaging, and receiver input capacitance. If these factors are well designed to keep the loading small, plain LVDS can drive this configuration.

The second multidrop bus differs from the first because it is driven from the center rather than the end of the bus. This configuration is useful for reducing flight-time variations from the driver to all receivers. However, it requires a termination resistor at each end of the bus to prevent reflections. Furthermore, the larger the capacitive loads and the less space between them, the lower the bus's loaded impedance. Because the termination resistors must match this lower impedance to stop reflections, they can be as low as 54Ω in a heavily loaded bus. The two termination resistors are seen in parallel by the driver, so the driver must source as much as three times the current of point-to-point LVDS to drive this bus to a given differential voltage level as it would for the unidirectional bus.

The third bus is a multipoint, bidirectional bus because it has multiple drivers and receivers (transceivers). This is the most difficult bus to design for high performance because of the variable driver positions, which cause various reflections that depend on where the signal originates in the bus. It also must be terminated on both ends to prevent reflections.

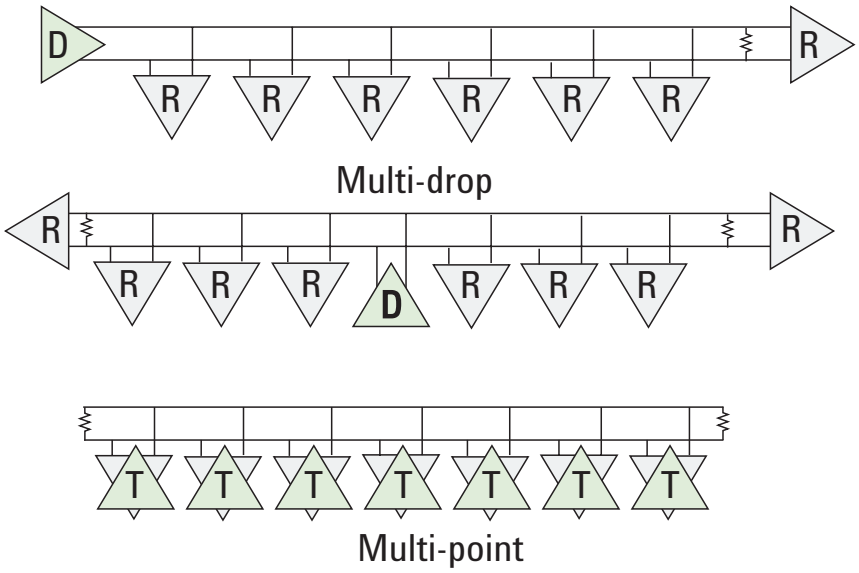

Figure 7. Multidrop and multipoint bus topologies are useful in BLVDS applications.

Signal integrity in a heavily loaded backplane is a very complicated problem due to the many impedance discontinuities inherent in the backplane environment. The worst-case situation in bus signaling occurs when a card in the middle of the bus drives a signal into the backplane and the card in the adjacent slot looks to receive the signal. The edge rate from the driving card is very fast as the signal leaves it and travels down the backplane. The adjacent cards see the fast edge propagate into the signal stub. This fast edge rate causes reflections on the stub that can glitch through the receiver threshold region. (The most important factor for high-speed performance in all bus topologies is keeping each receiver's non-terminated stub very short, minimizing reflections from that stub.)

BLVDS uses the same basic schematic as LVDS, but extends LVDS's point-to-point and simple multidrop applications to true multipoint busing functionality. It does this by boosting the drive current to 10 mA to drive double terminations on heavily loaded buses, and by providing driver output impedance that matches the line impedance to reduce reflections from driver outputs.

One of the essential features required in a multidrop bus is the ability to insert cards into the bus without powering it down. The optimal hot-insertion capability is to insert cards without stopping or disturbing the data traffic on the bus. BLVDS supports this optimal hot-insertion capability, as the signal glitch caused by inserting the capacitive load of the plug-in card occurs equally on each of the differential lines that have a low impedance connection between them. Therefore there is no change to the differential signal.

Serializer/Deserializer Example

An application example of Bus LVDS technology is the serializer/deserializer chipset. The transmitter serializes a 10-bit parallel LVTTL interface into a single BLVDS data channel, and also embeds the clock in the serial stream. The BLVDS receiver recovers the clock and data to deserialize them back into the 10-bit parallel interface.

This chipset distributes data over a serial channel in multidrop distribution systems. One serializer can drive many deserializers in either of the multidrop configurations shown in figure 7. Multipoint application is also possible with certain limitations due to PLL lock time. The limitations arise when a new driver begins to drive the bus and all the receivers must lock to that driver's clock signal. In addition, the chipset works in point-to-point applications. The chipset supports TTL clock rates from 16 to 66 MHz. For example, the chipset transfers a 660-Mb/s payload over a 10-meter cable when the 10-bit interface operates with a 66-MHz clock.

The chipset's waveform has a 10-bit payload surrounded by two embedded clock bits. The actual serial bit rate with a 40-MHz clock is 480 Mb/s, but the throughput is 400 Mb/s. The receiver uses the embedded clock edges to lock onto the inbound serial stream and to align the data at the parallel output. It provides greater system benefits than other LVDS parts by eliminating the cost of a cable or PCB differential pair for the clock signal.

LVDS in Low-Power Applications

LVDS is also being adapted for very low-power applications, such as a remote base station depending on wind- or sun-generated power. This is ground-referenced LVDS (GLVDS), which is a proposed standard interface. The JEDEC JC-16 committee for low-voltage interface standards is considering the standard. The proposed standard has transmitter output voltages between 0 V and 0.5 V, and receiver input sensitivity of at least 100 mV. The very low transmitter output voltage provides for low power consumption by the interface. This lower power consumption is an advantage this technology brings to the LVDS family of standards.

The simplified GLVDS schematic shown in figure 8 is very similar to both LVDS and BLVDS. One of the few differences is the circuit from the middle of the receiver termination to the receiver's ground. The GLVDS name refers to this ground reference for the receiver termination. GLVDS requires termination to be on-chip rather than an off-chip option, as is the case with LVDS and BLVDS.

Another important feature of this technology is the ability for chips with far different power supplies—from 5 V down to 0.5 V—to communicate with each other. This is possible because all of these power supplies use ground as a common reference. That common ground is the common voltage level where GLVDS signals are working.

The GLVDS standard does not specify any transmitter drive current. The intention is to leave that open to the individual applications that use the interface technology. This would allow the driver to provide a small current (for example, 1.5 mA to 3 mA) for chip-to-chip applications that have short interconnects. For applications that need to drive long cable lengths, the driver would have to supply a larger current output (8 mA to 15 mA).

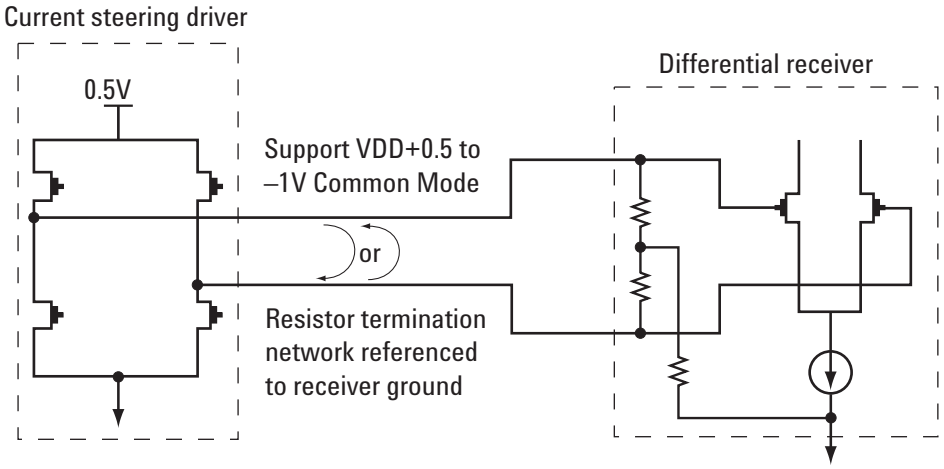

Figure 8. The simplified GLVDS schematic shows its similarity to both LVDS and BLVDS.

Test and Evaluation Considerations

There are many considerations with testing and evaluating high-performance LVDS devices. For example, the test equipment needs the two clock rates that result from serializing the parallel data into high-speed signals. The test system must be able to generate and analyze the data at both clock frequencies. Testing the receiver of the Open LVDS display interface (OpenLDI) chipset can demonstrate some performance issues.

Figure 9 shows a block diagram of the setup for the OpenLDI DUT interface board. The Agilent 81200 data generator/analyzer is a complete test system capable of 1.32-Gb/s testing (although the system works at a frequency of up to 2.67 Gb/s). The data generator/analyzer achieves 1.32 Gb/s by multiplexing two of the 660-Mb/s channels into one generator or analyzer channel. The test fixture uses an OpenLDI chipset DUT board. The characterization software components (CSC) takes the raw test data and converts it to an easy-to-understand visual format.

The data generator/analyzer uses ports to identify groups of generator and analyzer signals. In the OpenLDI deserializer test example, there are two generator ports and two analyzer ports. The generator ports, Port 1 and Port 3, supply the two frequencies required for testing the LVDS deserializer. The analyzer ports, Port 2 and Port 4, sample the data.

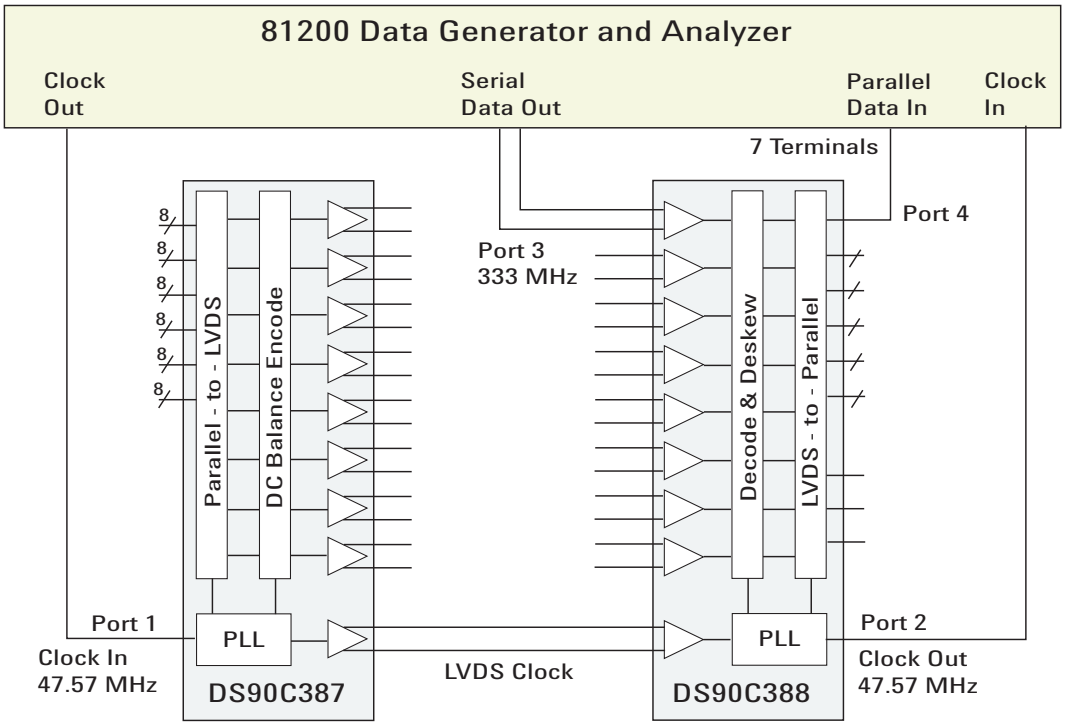

Figure 9. The test setup for the OpenLDI DUT interface board.

For the first set of tests, the data generator/analyzer creates the high-frequency serial data at 333 MHz, which corresponds to 333-Mb/s NRZ (nonreturn to zero) data generation. The generator also provides the serializer's input clock at 1/7 the serial data rate. The serializer then generates the LVDS clock input to the deserializer. The analyzer monitors the clock out from the deserializer and samples the data off of the seven parallel data terminals.

The first analysis that uses the visual display capability of the CSC shows the actual recoverable bit width of the serial data. Sweeping the serial data delay and checking the BER at the parallel Port 4 allow the data bit width to be displayed.

Figure 10 shows the delay vs. BER for the first two of the seven parallel bits. The bit width at 333 Mb/s is nominally 3 ns, but as the BER graph shows, the recovered bit is about 2.4 ns wide. On each side of the valid-data window, the BER increases to a nonzero value. The BER is a constant value for each of the serial bits preceding and following the bit being checked for correctness. The values are constant but not at 1 because of the repetitive bit pattern used in this test. If the bit pattern had instead been a PRBS pattern, then the BER for each of the other bits would be 0.5, which means there is an equal, and random, chance that the bit would be either 1 or 0.

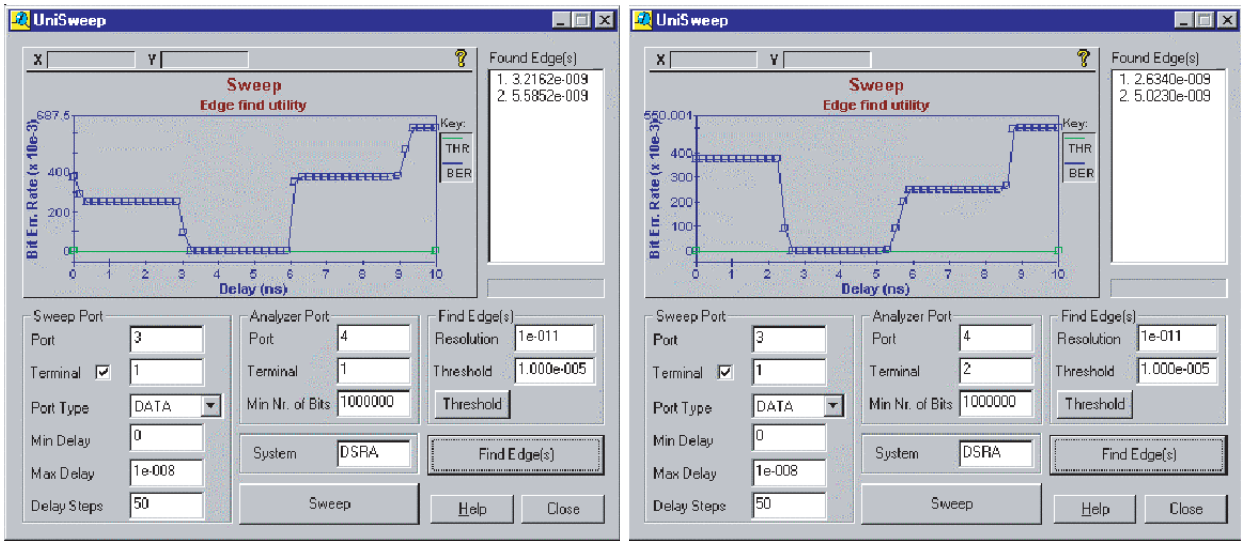

Figure 10. The delay vs. the BER for the first two of seven parallel bits shows the recoverable bit is about 2.4 ns wide.

BER Eye Diagram

The next analysis tool is the BER eye diagram. The CSC (computer software component) generates this diagram by sweeping the sampling delay and the threshold of the analyzer on Port 4. The graph displays the BER as a color at each sampling point. The result is an eye pattern with the black center representing the correctly sampled data. Other colors show the increasing errors as the sample point moves further away from the window (figure 11).

This eye pattern differs from an oscilloscope eye diagram because it does not simultaneously show multiple transitions. An oscilloscope eye diagram displays signal-integrity information such as overshoot, undershoot, and edge jitter. A BER eye diagram demonstrates the valid-data window for the recovered bits, which ultimately depends on receiver sampling performance in addition to signal integrity.

Figure 11 visually emphasizes the useable portion of the serial bit width that was also shown in figure 10. The BER eye width for Port 4, terminal 1, at 333 Mb/s shows the same 2.4-ns bit width as in the serial-port delay vs. BER graph.

The BER eye diagram for the 666-Mb/s serial data shows how the bit width decreases as the signaling frequency increases. The graph on the right shows that although the nominal bit width at 666 Mb/s is 1.5 ns, the valid-data window delivered by the receiver and deserializer is really about 1.1 ns wide.

This BER eye diagram is useful in characterizing receiver performance. It allows examining the eye diagram for each individual bit. At the highest performance level, these eye diagrams must show limited variation between bits to ensure there is maximum margin for board and cable skew. This characterization helps system designers to achieve reliable

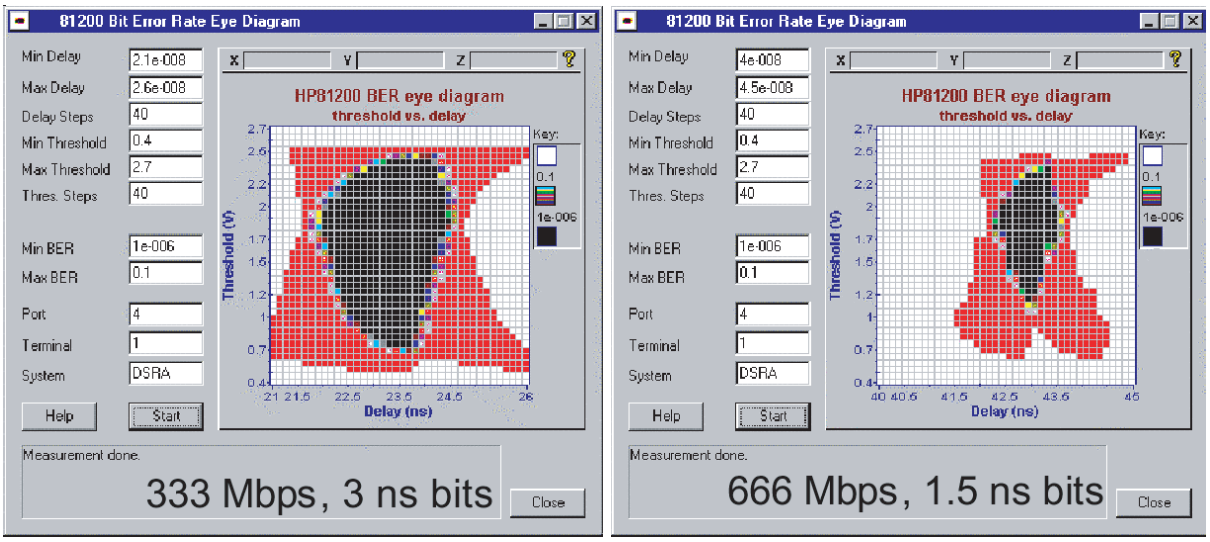

Figure 11. BER eye diagrams for two data rates show how the bit width decreases as the signaling frequency increases.

Recovered Clock Jitter

The deserializer's recovered clock-out jitter can also be examined with the CSC (computer software component). In this case, the data generator/analyzer creates a histogram using the BER measurement. It performs these histogram measurements on a running device to obtain accurate jitter measurements. The CSC uses the deviation of the BER (dBER/dt) to calculate the jitter. It measures the signal transitions by selectively looking at the pass-to-fail and the fail-to-pass BER transitions.

Figure 12 shows the jitter on both the rising edge and the falling edge for the deserializer recovered clock-out signal. Because the sampling point for the analyzer is set at the same point for both the high and low transitions (1.4 V in this case), the jitter is symmetrical on the transitions. Setting the sampling point at different thresholds for the rising transition (2 V) and falling transition (0.8 V) results in different mean transition times for each of the edges.

The CSC also provides calculations for sigma and 6-sigma analysis of the histogram. The Sigma button displays a measurement that corresponds to the RMS jitter, while the 6-Sigma button displays a measurement that corresponds to a peak-to-peak jitter measurement. In figure 12, the CSC reports that rms (root mean square) jitter is about 45.2 ps for both the rising and falling edges of the deserializer clock-out.

Some applications are suitable for more than one of the various LVDS technologies, but there are others in which only one would excel. Plain old standard LVDS excels in applications requiring driving relatively short interconnects, and also where EMI is a critically sensitive issue for the interconnect, such as in display technology.

Bus LVDS excels at driving heavily loaded backplanes such as those used in telecommunications systems. It also works well in distributing signals from a single driver to multiple receivers. BLVDS also finds applications in driving bussed cable interconnects of a few meters in length.

GLVDS could work in very low-power applications such as remote base stations where power may be locally supplied and generated by wind or sun. It could also be useful as a chip-to-chip interconnect for very short distances. The main function for GLVDS might be as the interconnect technology for chips that have power supplies of 1 V or less. Low-Voltage Differential Signaling will continue to evolve toward more and more system applications.

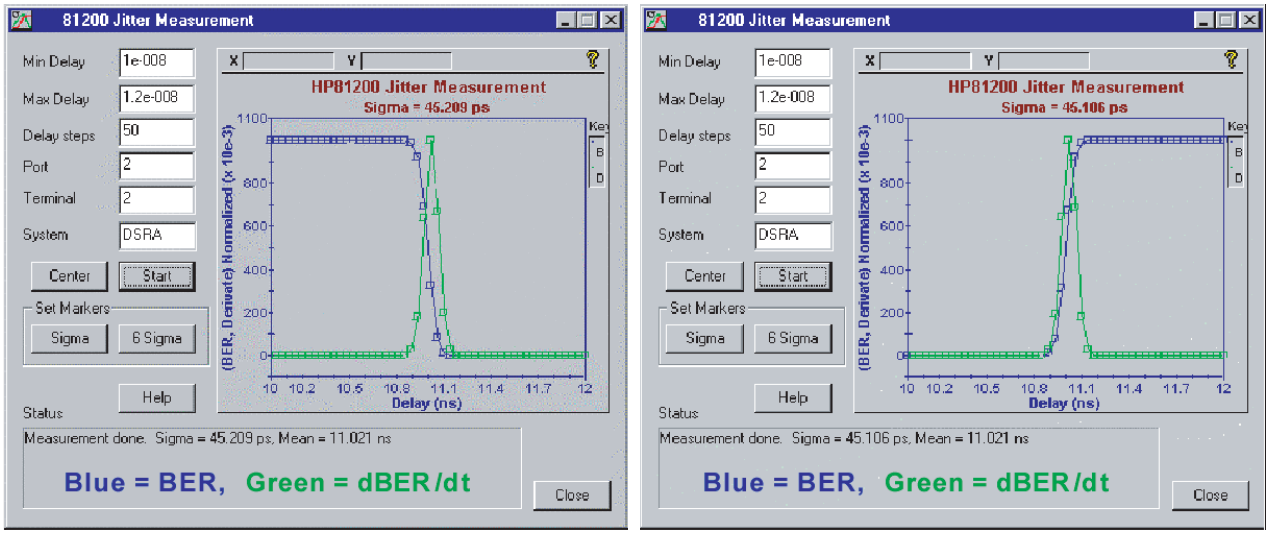

Figure 12. The deserializer's recovered clock-out jitter shows symmetrical jitter when using the same threshold (1.4 V).

ParBERT 81250 Simplifies the Characterization and Testing of LVDS Devices

The advantages of higher speed and better noise performance of LVDS devices must be properly characterized before an LVDS device can be properly designed into a system. The Agilent Technologies ParBERT 81250 provides measurement capabilities that until now were difficult and time consuming to perform. The ParBERT 81250 is a modular instrument that provides parallel bit error rate testing up 2.66 Gb/s for up to 64 channels. It provides chip control signals, divided or multiplied clock signals, 1-Mb/s to 2.6-Gb/s operation with proprietary formats, as well as low voltage differential signaling (LVDS) load generation or analysis. You can test SAN-related multiplexers and demultiplexers, including gigabit Ethernet, flat panel display links, Fibre Channel, and InfiniBand. ParBERT 81250 is especially suitable for multiplexer and demultiplexer (MUX/DeMUX), or SERDES (serializer/deseralizer) testing used in telecommunications and system area network (SAN) ICs, multiple transmitter and receiver testing in manufacturing, and forward error correction (FEC) device testing.

Manufacturing test engineers responsible for testing multiple transmitters and receivers often find that reducing the cost-per-test is critical. The Agilent 81250 ParBERT and SpectralBER help by providing scalable VXI platforms that let designers customize the number of channels needed.

For designers who need to test SAN-related multiplexers or demultiplexers, including Gigabit Ethernet, flat panel display link, Fibre Channel, and InfiniBand, the combination of the 81250 ParBERT, 86130A BitAlyzer and the 86100A Infiniium DCA helps solve physical high-speed design problems.

Figure 13. The Agilent ParBERT 81250 parallel bit error rate tester

81200 Provides the Tools to Test LVDS

Testing and evaluating LVDS-based components and systems is a challenge. Not only are the data rates very high and the signals differential, but the types of tests required are often complex and time consuming to perform. The Agilent 81200 provides an easier way to evaluate a design or perform manufacturing tests. It provides a number of visual presentations that allow you to quickly analyze measured data and evaluate the outcome of tests.

The Agilent 81200 data generator/analyzer platform is a flexible real-time stimulus and response system that now works at up to 2.67 Gbit/s for up to 64 channels. It provides chip control signals, divided or multiplied clock signals, 1-Mb/s to 2.67-Gb/s operation with proprietary formats, as well as LVDS load generation or analysis.

Powerful sequencing capabilities and full control of pulse parameters for each individual channel mean that you can really stress your device under test (DUT). The system generates pseudo random word sequences (PRWS) and pseudo random binary signals (PRBS) up to 2^{15}-1. Analysis is in real time, saving you time because no post-processing is necessary.

If you work on telecommunications multiplexers and demultiplexers (MUX/DeMUX), SERDES (serializer/deserializer), or transmitters and receivers, you can take advantage of the thorough parallel BER measurements of the ParBERT 81250 system. For compliance testing, it generates PRWS and PRBS up to 2^{31}-1, and also has sophisticated synchronization features.

Figure 14. The Agilent 81200 data generator/analyzer

Related Literature

Publication Title	Publication Type	Publication Number
Need to Test BER? Complete Solutions for High Speed Digital Transmission Testing	Color brochure	5968-9250E
Agilent ParBERT 81250 43G Parallel Bit Error Ratio Tester	Product overview	5988-3020EN
Agilent 81200 Data Generator/Analyzer Platform	Color brochure	5980-0488E
Test Tools for InfiniBand	Color brochure	5988-2424EN

Agilent Technologies' Test and Measurement Support, Services, and Assistance
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