

# Debugging a PCI Bus with a Mixed-Signal Oscilloscope

Application Note 1417

## Introduction

In today's high-tech, high-speed world, engineering teams frequently are under pressure to finish design projects quickly. The faster you can complete a design, the sooner the product hits the market and the sooner it starts producing revenue. If you are like most engineers, your response to the pressure is to look for ways to get your job done as quickly and efficiently as possible.

One of the more time-consuming tasks in a project is debugging your design, or identifying, locating and resolving the inevitable problems. Isolating signal-integrity issues on a PCI bus can be particularly time consuming. However, choosing the right test instruments can reduce significantly the time you devote to the task.

There are several test instruments you can use to test a PCI bus, and engineers typically use more than one in order to fully test them. Logic analyzers are excellent tools for looking at all the lines on the bus simultaneously. However,

because logic analyzers are strictly for digital signals, they capture data as 1s and 0s. You cannot view detailed signal characteristics such as ringing, rise times, bounce, etc., with a logic analyzer, and this type of information is critical for effective PCI-bus debugging.

PCI exercisers and analyzers also allow you to connect all the lines of the PCI bus, and they provide more timing checks for PCI-bus events than logic analyzers do. You can find and isolate timing violations more easily with these tools, but they also do not allow you to view and analyze errors in detail.

Many engineers consider digital storage oscilloscopes (DSOs) to be the best tool for viewing and analyzing signal integrity issues. Oscilloscopes are designed specifically to look at signal characteristics in detail. However, since scope channel count is limited (maximum of four channels), it is sometimes difficult to trigger properly on PCI-bus events. To look at signal integrity issues with complex,

multi-line triggering, you need to cross trigger the oscilloscope with either an exerciser/analyzer tool or a logic analyzer.

Agilent Infiniium Series mixed-signal oscilloscopes (MSOs) fill the gap in the above tool set. They feature a normal number of scope channels (2 or 4) and also contain 16 digital timing channels. Using an MSO, you can trigger and view a signal integrity issue on a PCI bus with a single instrument, greatly simplifying your debugging task and eliminating the time and trouble required to set up elaborate cross-triggering schemes.

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## Identifying the Cause of Intermittent Failures

This application note describes how Agilent engineers used an Infiniium MSO to isolate a PCI bus problem. While the specifics of your debugging task will be different from the one described here, you should be able to use a similar process to speed up your debugging tasks.

Agilent engineering teams were nearing completion on a development project for a test-instrument acquisition board. The hardware seemed to be functioning properly and the firmware quality assurance process was on schedule. Then the acquisition boards started to fail sporadically. Boards that were working fine would suddenly crash. A system shut-down and reboot were required for operation to resume.

The failures threatened the product launch schedule. Engineers on the manufacturing line could not get the new systems to run through all the parametric tests consistently and environmental testing could not proceed. Firmware engineers needed to reboot numerous times a day, causing delays in firmware QA.

After examining the problem, project engineers found that the board's PCI bus was locking up intermittently. Since the problem was intermittent, the team's first step was to find a way to reproduce the problem repeatedly. Software and hardware engineers collaborated and discovered a way to cause the problem more frequently, although they did not reach the stage where they could reproduce it purposefully and reliably. The problem occurred more often when the engineers ran a software test cycle that exercised the PCI bus and the devices connected to it. The team's next step was to determine where and why the failures occurred.

The printed circuit board had many custom components and ASICs on it. The area of interest contained a 32-bit, 33 MHz PCI bus with five to seven devices connected to it, depending on the configuration. A large firmware base drove the board.

A 32-bit PCI bus requires 47 to 49 pins, depending on whether it is a target or master device. For this project, all components contained

49 lines, since all devices were required to master at some point. Multiplexed address and data pins occupied 32 of the 49 lines. Two were for error reporting and one was a parity bit for the address/data lines. The rest were control lines that coordinated bus use by multiple devices. Since the team faced a lockup problem, they needed to look at the interaction of the control lines. The team used an Agilent 54832D Infiniium MSO that has 16 digital timing channels as well as the 4 standard analog channels.

The team noticed a problem when it ran basic write and readout tests; the address lines of one of the devices occasionally received the wrong address. That is, the sequence returned was not always the sequence that had been sent. For instance, an ABCDEF address sequence sent to the device would be read sporadically as ABCFEF. This prompted the team to look at the address phase of the PCI bus transaction. The MSO's state trigger handled this task nicely.

# The Debugging Process

To begin, the team hooked up several of the control lines from the bus (FRAME#, IRDY#, TRDY#, DEVSEL#, GNT0) to five of the digital channels on the MSO. Because the engineers suspected the clock line was the source of the problem, they hooked CLK to an analog channel. We set the oscilloscope to trigger in the advanced AND state/pattern mode.

CLK provides the basic timing for the PCI bus. All the other connected lines were sampled on the rising edge of CLK. CLK was therefore used as the clock in the state trigger. FRAME# is asserted when a transaction occurs. It needed to be asserted (lo) in the trigger since the non-transaction phases were not of interest. IRDY# and TRDY# were asserted when both the initiator (or master) and the target were ready for data transfer. Since the data phases of the transaction were not important, the team wanted both IRDY# and TRDY# to be de-asserted (hi). DEVSEL# indicates when the device has decoded its address. Since we were interested in the address phase itself, we set it up to be de-asserted (hi). This prevents triggering in the middle of a data phase where both the master and the target devices are not ready. GNT0 is an arbitration line used to grant devices the right to drive the bus. We toggled it from asserted (lo) to de-asserted (hi) so we could control whether or not we triggered when device 1 was driving the bus. The MSO's dialog boxes for the trigger are shown in figures 1 and 2.

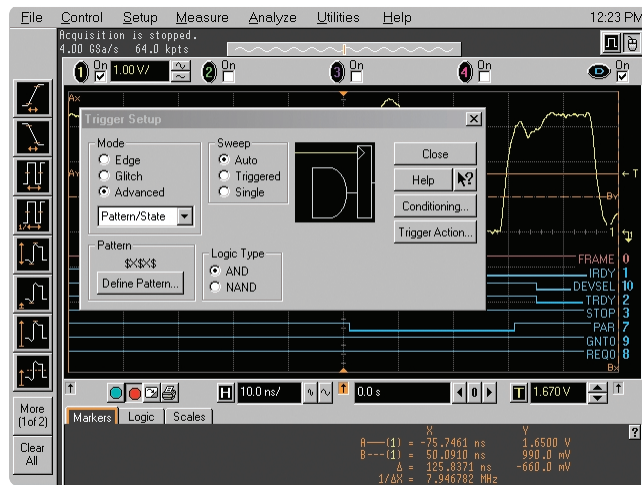


Figure 1. The MSO's Trigger Setup dialog box makes it easy to specify high-level trigger conditions.

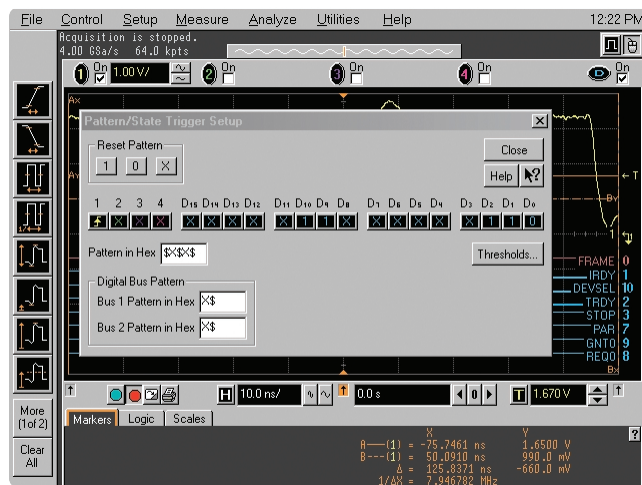


Figure 2. You also need to use the Pattern/State Trigger Setup dialog box to specify the pattern for the trigger.

## The Debugging Process (continued)

The address phase of a PCI bus starts on the CLK edge after FRAME# is asserted (going low). After some investigation, the debugging team noticed that the CLK signal appeared to be having problems with signal integrity. They turned on the “infinite persistence” feature to keep a running record of all the triggers on the scope, so they could see any issues with the CLK signal. Figure 3 shows the address phases of all devices other than device 1. That is, GNT0 was set to de-assert (hi) in the state trigger described above. Basically, the team was examining CLK-signal integrity when device 1 was inactive. The markers were set to the VIN and VOut levels of the CLK. Everything looked fine.

Triggering on the address phase of device 1, however, revealed a problem with the clock pulse that preceded the address phase clock. This is the clock that samples the FRAME# signal when it is first asserted. Figure 4 clearly shows an anomaly dropping below the trigger level and the VOut marker. This is an indication that the CLK occasionally sampled twice, instead of just once. Coupling between the device lines and the CLK line caused the dip in the CLK signal (figure 3). Activity on device 1 caused the coupling to increase. This extra coupling was enough to drive the CLK signal below acceptable limits intermittently.



Figure 3. The CLK signal (yellow trace) shows potential signs of signal integrity issues.



Figure 4. On the CLK signal, an anomaly dropped below the trigger level and the VOut marker.

# The Solution

Now that the engineers had a viable suspect, they added circuitry to enhance the coupling on boards that were not failing to see if they would fail, too. They did.

The address write and readout tests failed occasionally because the anomalous CLK signal was double clocking, causing the address to be read in sooner than expected. The address was clocked when the anomalous dip in the CLK signal went high, instead of clocking on a normal edge.

Changing the circuitry to reduce the coupling between the activity on device 1 with the CLK eliminated the intermittent lockup problems.

## Conclusion

The mixed-signal oscilloscope was an effective tool for exploring signal integrity issues on the PCI bus. If we had used a DSO to examine the same problem, we would have needed to build external circuitry or we would have needed to use a logic analyzer to cross trigger the DSO. Both solutions make it difficult to look at the signals you are triggering on as well as the signal you are checking for integrity problems. Both solutions require significantly more time to set up. Using an MSO helped our project team to reduce debugging time, allowing us to meet our schedule requirements.

## Glossary

**ASIC** Application-specific integrated circuit

**DSO** Digital storage oscilloscope

**MSO** Mixed-signal oscilloscope

**PCI bus** Peripheral Component Interconnect local bus is an industry-standard, high-performance 32-bit or 64-bit local bus architecture intended for use between highly integrated peripheral controller components, peripheral add-in cards, and process/memory systems.

## Related Literature

<b>Publication Title</b>	<b>Publication Type</b>	<b>Publication Number</b>
<i>Agilent E2930 PCI Timing Check using the Agilent E2920 PCI Series Exerciser/Analyzer</i>	Application Note	5968-5816E
<i>Finding Hidden Problems Using Deep-Memory Oscilloscopes</i>	Application Note	5988-5979EN

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