Using the Agilent Infiniium Series Real-time Oscilloscope to Validate the DigRF

Application Note 1598

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The DigRF v3 standard

The DigRF v3 standard presents new digital hardware validation challenges for mobile wireless development as the links between the baseband (BB) ICs and the radio frequency (RF) ICs transition from an analog interface to a digital interface. The DigRF v3 standard was designed to enable interoperability between RF ICs and BB ICs from different suppliers. To ensure your devices interoperate properly, you will need to add compliance measurements to your hardware validation test plan.

With the superior signal integrity, jitter analysis software and probing solutions provided by the Agilent 80000 Series oscilloscopes, you can have confidence in your ability to test and validate your digital interfaces for DigRF compliance and interoperability.

The DigRF v3 specification allows for 1.8-V LVDS, 1.2-V LVDS or SLVDS electrical interfaces between the BB IC and the RF IC. The interface consists of six signals with independent transmit and receive paths.

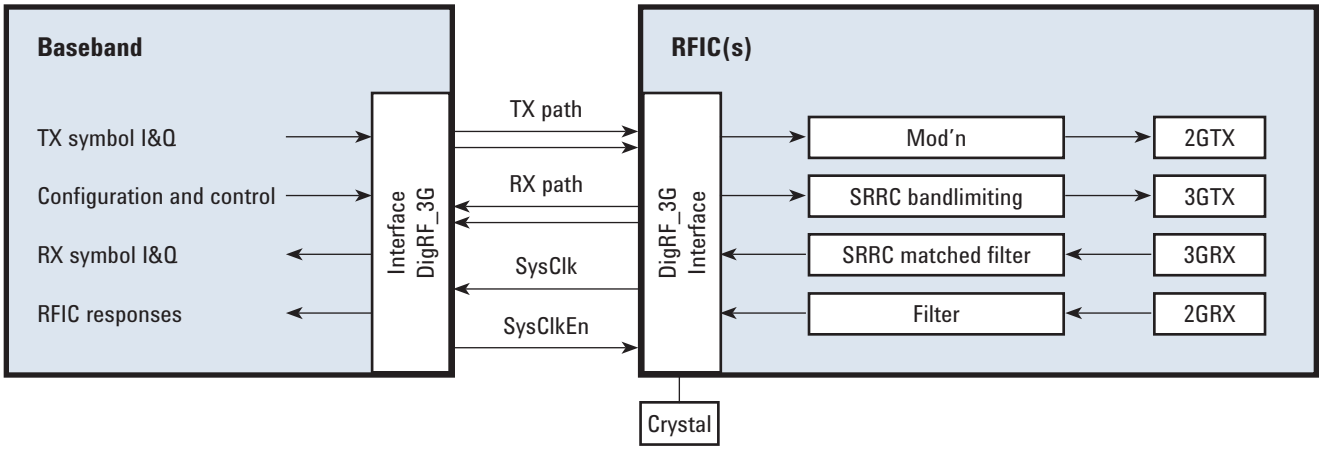

Figure 1. DigRF v3 top-level block diagram

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Oscilloscope bandwidth requirements

Agilent Infiniium oscilloscopes have real-time system bandwidths from 2.5 GHz to 13 GHz. For DigRF v3, the 2.5-GHz DSO90254A provides sufficient system bandwidth with the 1131A 3.5-GHz InfiniiMax differential and single-ended probes.

For future needs, the Infiniium 90000 Series is also bandwidth upgradeable up to13 GHz.

Probing and system setup

Single-ended probing solution
When you probe with single-ended probes, you make the measurement by probing each half of the differential signal for the Tx and Rx buses. For measurements made from the RF IC to the BB IC, the RX signals are probed, and TX is probed from the BB IC to the RF IC. The differential signal is created with waveform math using Ch1–Ch3. The common mode measurements are also available from the common mode waveform (Ch1–Ch3)/2.

With this use model, it is a good idea to solder in the probe using the E2679A solder-in single-ended probe head with the 1131A probe adapter. One probe is soldered with a 91-ohm leader resister (01131-81510) to the pad on the board or directly to the device for RXp and the other probe is connected to RXn. The grounds will be connected through a 0-ohm mini-axial lead resistor (01131-81504) to a pad on the board.

For the most accuracy using this technique channel-to-channel deskew is required.

Figure 2. InfiniiMax solder-in single-ended probe head

SMA probing solution
When probing with SMA, the measurement is similar to the single-ended probes where the differential signal is created with waveform math using Ch1–Ch3. The common mode measurements are also available from the common mode waveform (Ch1–Ch3)/2. Just as with the single-ended probe measurement, each SMA probe will be connected to an SMA connector for the RXp and RXn for measurement from the RF IC to the BB IC.

This probing technique requires breaking the link between the RF IC and the BB IC and terminating into the 50-ohm termination into the oscilloscope.

For the best accuracy, channel-to-channel deskew is also required for this technique because two channels are used.

Differential probing solution
When you probe with a differential probe, the measurement is made by probing both the RXp and RXn signals from the RF IC to the BB IC at the same time you probe with the 1131A InfiniiMax differential probe.

With this use model, it is a good idea to solder in the probe using the E2677A solder-in differential probe head with the 1131A probe adapter as shown in Figure 3. One side of the probe will be connected to the RXp signal and the other will be connected to the RXn signal. Each connection to the circuit is made using a 91-ohm lead resistor (01131-81510).

Channel-to-channel deskew is required using this technique.

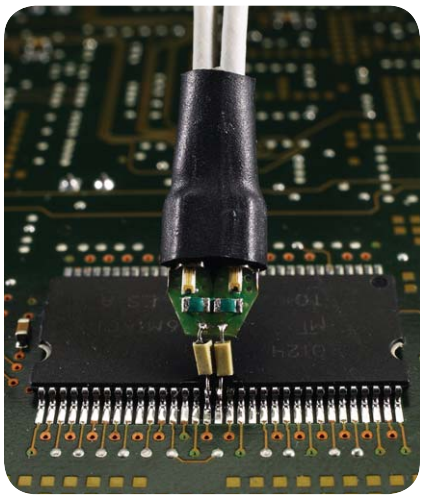

Figure 3. InfiniiMax solder-in differential probe head

SysCLK measurements

For DigRF v3, the SysCLK is the single-ended master reference clock for both the BB IC and RF IC. The specifications for the SysCLK are 45 to 55% duty cycle and a frequency of 19.2 MHz, 26 MHz, or 38.4 MHz.

The high-speed data rate in 3G or dual-system mode on both the TxData and RxData interfaces is 312 Mbps (1248 MHz/4 = 38.4 M x 65/8, 26 M x 12, or 19.2 M x 65/4). The 312 MHz clocks at the two ends of each link need to be in nominal phase lock with each other.

The clock is distributed between the BB IC and RF IC at the system clock frequency to minimize the generation of spurious signals and clock skew problems. The high-frequency clock signals are generated locally within each IC with a limited frequency error to ensure the robustness of the interface. The SysCLK signal is provided to the baseband continuously while SysClkEn is asserted from the BB IC.

Automatic measurements on Infiniium Series scopes enable easy measurements on SysCLK to measure all the basic characteristics including voltage level, rise time, fall time, frequency, slew rate, etc.

Serial trigger for data analysis

The sync field for DigRF v3 is a 16-bit pattern designed to facilitate phase selection in the interface receivers (1010100001001011). This pattern is used for all clock speeds.

The N5414A InfiniiScan identification software allows you to trigger at the beginning of the packet using the 16-bit pattern to further analyze the DigRF data signals.

In Figure 4, the trigger is applied to the positive signal of the differential pair for analysis. You can use the oscilloscope's automatic measurements to validate typical measurements like voltage level, slew rate, rise time, fall time, etc., to ensure compliance with the specifications. Both differential signals are shown in Figure 5. You also can use markers to validate packet length, bit times, and other timing measurements.

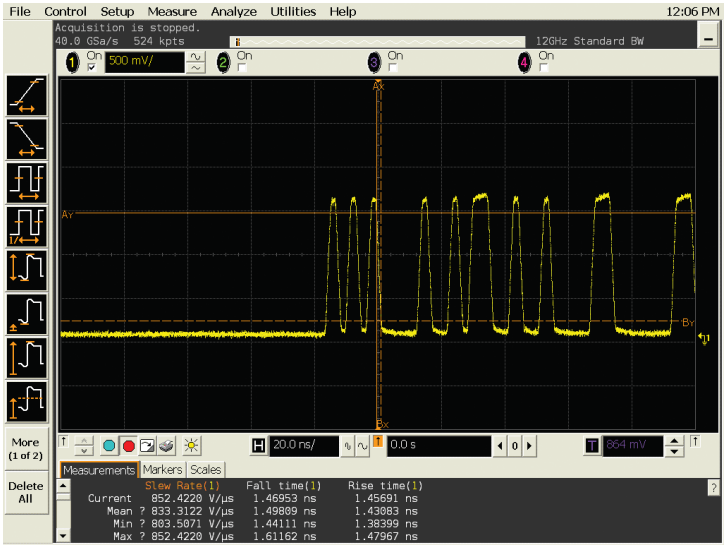

Figure 4. Oscilloscope triggering on DigRF sync

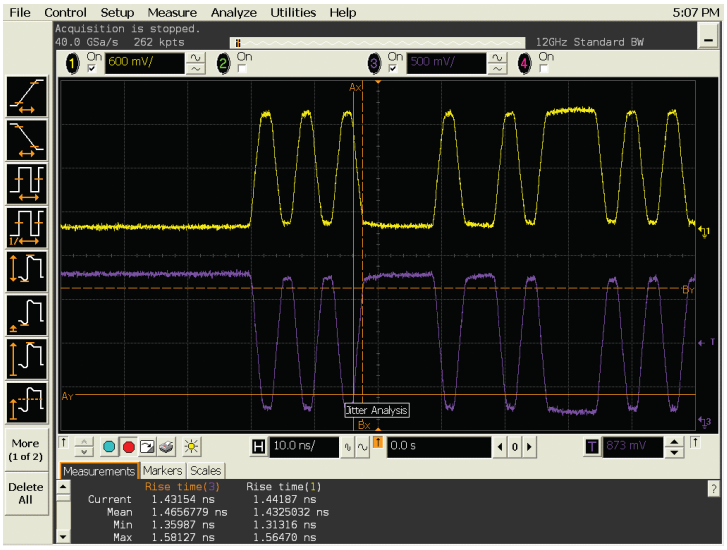

Figure 5. Oscilloscope triggering on DigRF sync with both RXp and RXn signals

Basic jitter analysis

Jitter is fundamentally the deviation of a timing event of a signal from its ideal position or an expected location or absolute time reference. As shown in Figure 6, amplitude and phase noise can combine to cause jitter.

Jitter is complex and is composed of both random jitter (RJ) and deterministic jitter (DJ). Random jitter (RJ) is unbounded and is usually measured in terms of an RMS value, while deterministic jitter (DJ) is bounded, but doesn't follow any predictable distribution. Deterministic jitter is measured in terms of peak-to-peak values. The causes of deterministic jitter, unlike random jitter, are usually predictable and can be broken down into sub-components of duty cycle distortion (DCD), inter-symbol interference (ISI), and periodic jitter (PJ). For more information on the jitter components, refer to the application note, *Measuring Jitter in Digital Systems*, Application Note 1448-1 or *Finding Sources of Jitter with Real-Time Jitter Analysis*, Application Note 1448-2.

The most fundamental way to view total system jitter is by using the eye diagram on an oscilloscope. An eye diagram is a composite view of all the bit periods of a captured waveform superimposed on an ideal timing reference to provide a view of all the data unit intervals over a long continuous acquisition.

The display is also color graded to provide information about the number of hits at a particular voltage or time.

For the DigRF 3.09 version of the specification, the total clock jitter specification is 600 ps peak-peak and 600 ps total jitter for data.

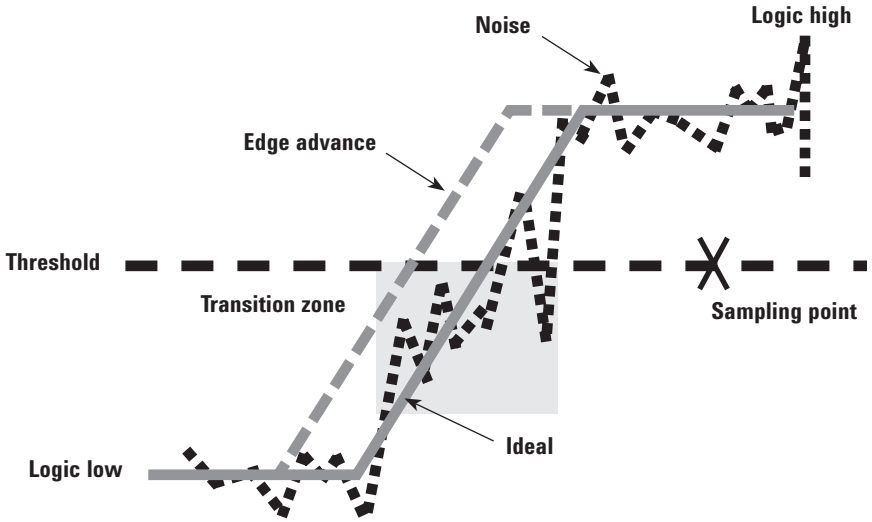

Figure 6. Amplitude and phase noise can combine to cause jitter

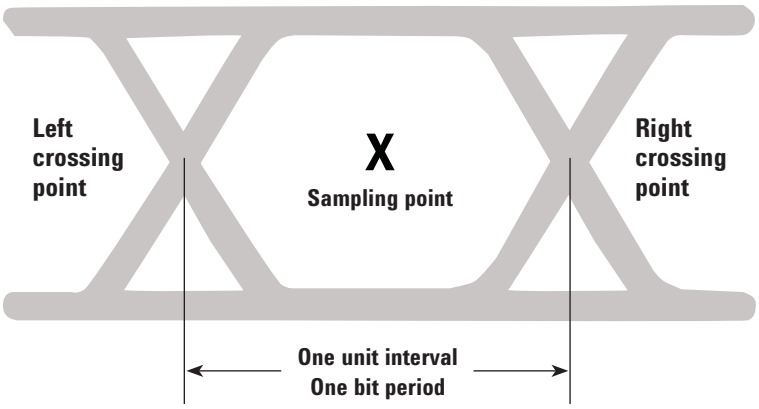

Figure 7. An idealized eye diagram

High-speed serial data analysis

With the DigRF v3 standard, the SysCLK is a forwarded clock running at 19.2 MHz, 26 MHz, or 38.4 MHz while the data rate is 312 Mbits/s for Tx and Rx. The E2688A serial data analysis software allows you to reconstruct the data clock that has been multiplied up in the receiver to create a real-time eye diagram to analyze the total system jitter, perform mask testing, and characterization of the serial data streams.

A histogram measurement is also very useful to analyze the types of jitter present in the system. In Figure 8, the histogram appears to have a normal Gaussian shape.

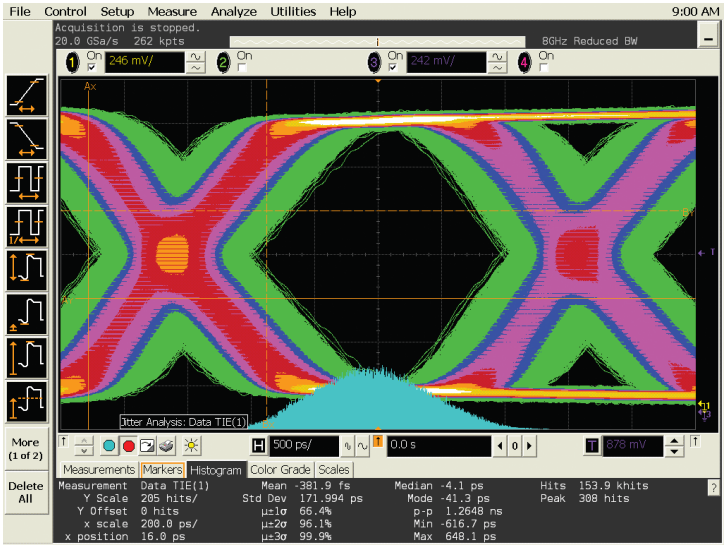

Figure 8. DigRF eye diagram from recovered clock

Jitter analysis with EZJIT Plus software

EZJIT Plus, a jitter analysis software package for the Infiniium oscilloscopes, separates the RJ/DJ jitter components to give you further insight into underlying causes of the system jitter. The software can analyze the jitter on any clock waveform or NRZ serial data waveform, no matter what binary sequence is present in the data. EZJIT Plus software uses two different analysis techniques depending on whether you specify that the data is periodic or non-periodic. For DigRF v3, the periodic method is used to optimize analysis time.

The EZJIT Plus software is easy to set up using a measurement wizard to identify the data channels, vertical channel scaling, clock recovery algorithm, acquisition memory depth, sample rate, and more.

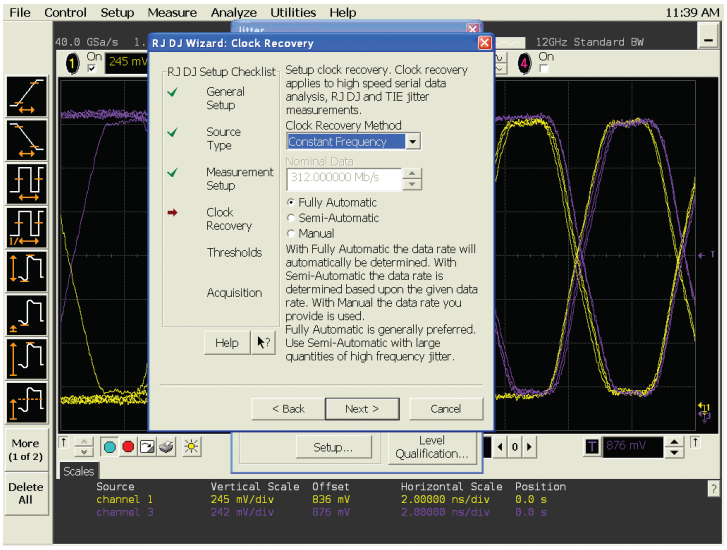

Figure 9. Clock recovery wizard in EZJIT Plus software

With the EZJIT Plus software, you can see the RJ/DJ separation and the eye diagram, as shown in Figure 10. This particular system shown in Figure 10 is not compliant with the jitter specification for DigRF v3 as there is 1.2856 ns of TJ or total jitter versus the 600 ps peak-to-peak specification for data.

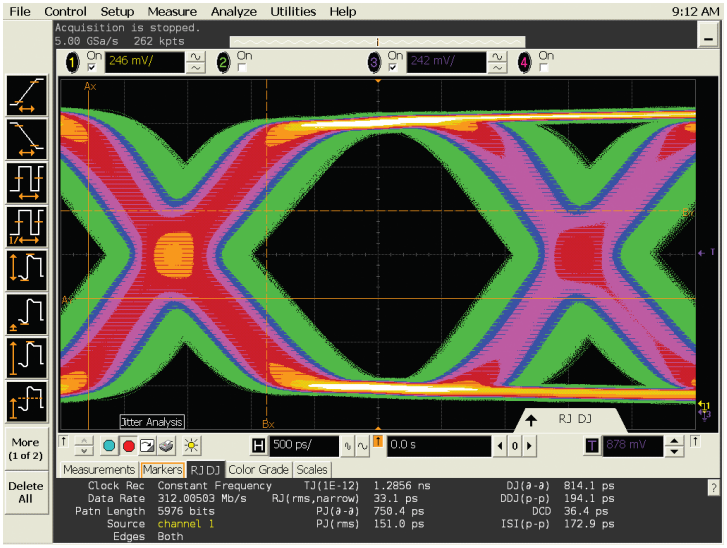

Figure 10. Eye diagram using EZJIT Plus software to show jitter separation of RJ and DJ

The EZJIT Plus software also allows you to view histograms of total jitter combined with the separation of each jitter component. You can also view the jitter contribution by frequency with FFT analysis of the random jitter and periodic jitter to further analyze the potential jitter source. **You can also predict bit error rates with the EZJIT Plus software.**

For more information regarding EZJIT Plus software, refer to the application note *Analyzing Jitter Using Agilent EZJIT Plus software*, Application Note 1563.

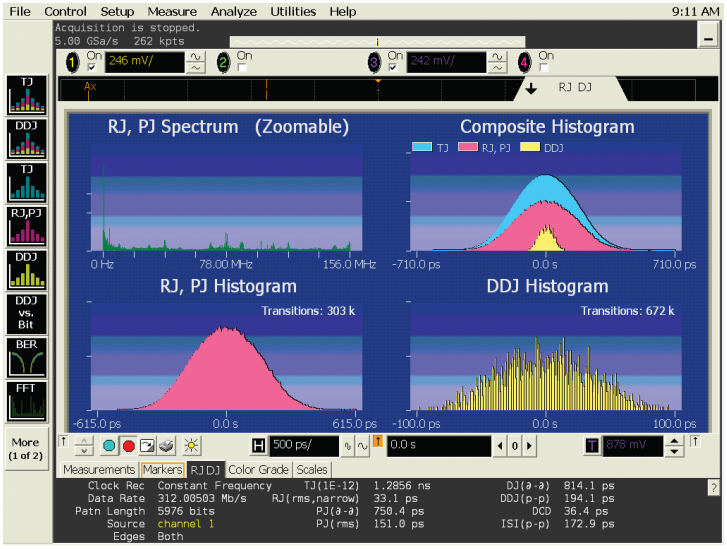

Figure 11. Histogram measurements using EZJIT Plus software

Complete DigRFv3 Test Solution

Measuring and stimulating the BB-IC and RF-IC interface traditionally required you to use a spectrum analyzer and signal generator. However these tools are incapable of making the necessary measurements on the new digital serial bus. Creating a custom test solution requires resources, time and long-term support that you just can't afford.

To address this measurement challenge, Agilent developed the N4850A DigRF v3 acquisition probe and N4860A DigRF v3 stimulus probe. The probes operate in conjunction with 16800 and 16900 Series logic analyzers to provide the digital serial acquisition and stimulus capabilities required for DigRF v3-based IC evaluation and integration. The integration of DigRF v3 logic analysis tools with the Agilent RF portfolio provides the cross-domain solutions that will help you rapidly deploy your DigRF v3-based designs. For the most up-to-date and complete application and product information, please visit our Web site at: www.agilent.com/find/DigRF

Figure 12. Stimulus, analysis and RF tools provide complete DigRF v3 test solution.

Product Web site

For the most up-to-date and complete application and product information, please visit our product Web site at: **www.agilent.com/find/DigRF**

Related literature

Publication title	Publication type	Publication number
Infiniium 90000 Series Oscilloscopes	Data sheet	5989-7819EN
Infiniium DSO80000B Series Oscilloscopes and InfiniiMax Series Probes	Data Sheet	5989-4604EN
EZJIT and EZJIT Plus Jitter Analysis Software for Infiniium Series Oscilloscopes	Data Sheet	5989-0109EN
Agilent Technologies E2688A, N5384A High-Speed Serial Data Analysis and Clock Recovery Software for Infiniium Oscilloscopes	Data Sheet	5989-0108EN
Agilent InfiniiScan Event Identification Software for Infiniium Series Oscilloscopes (N5414A and N5415A)	Data Sheet	5989-4605EN
Measuring Jitter in Digital Systems	Application Note	5988-9109EN
Analyzing Jitter Using Agilent EZJIT Plus Software	Application Note	5989-3776EN
Finding Sources of Jitter with Real-Time Jitter Analysis	Application Note	5988-9740EN
Agilent Solutions for the DigRF v3 Digital Serial Interface Used In Mobile Wireless Devices	Brochure	5989-6224EN
Agilent N4850A DigRF v3 Acquisition Probe	Data Sheet	5989-6058EN

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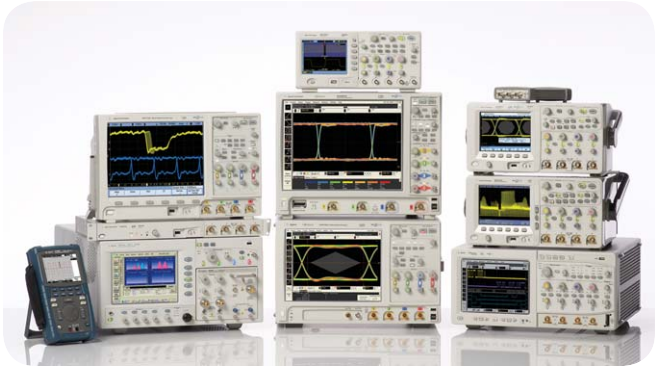

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Revised: October 1, 2008

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Printed in USA, June 18, 2009
5989-7189EN

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