Errata

Document Title: Digital Triggering For Analog Instruments (AN 167-2)

Part Number: 5952-1939

Revision Date: March 1974

HP References in this Application Note

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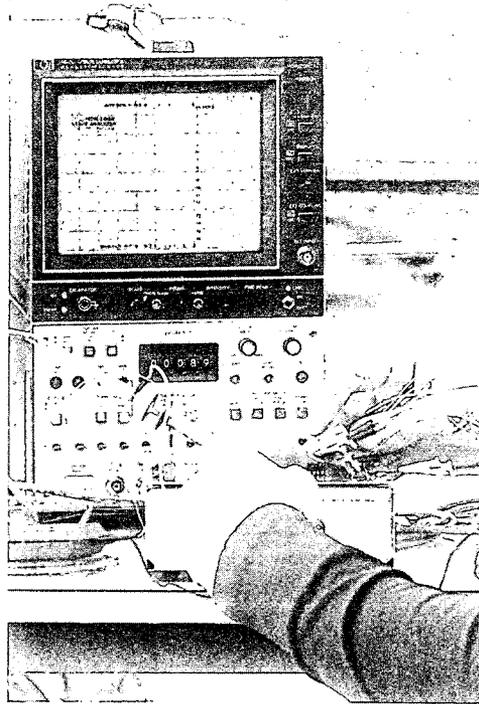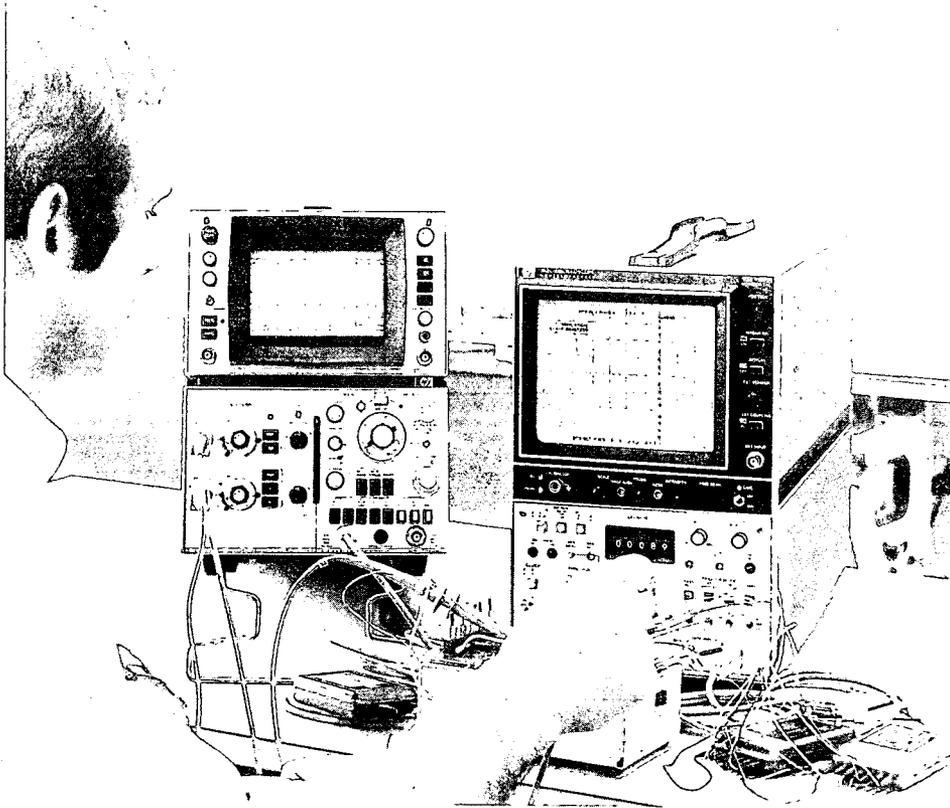
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DIGITAL TRIGGERING FOR ANALOG MEASUREMENTS

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The Model 1601L Logic State Analyzer's ability to trigger on a particular state in sequential state digital machines is made possible with its 12-bit parallel pattern recognition capability. This unique trigger signal, available as a front panel output, is an extremely powerful tool in digital circuit analysis. The trigger signal is an RZ pulse that occurs each time the digital pattern in the circuit under test matches the pattern set on the Analyzer trigger switches. This signal, when applied to other test instruments, positions the measurement in the same "time window" as the event. Two examples of the use of the trigger signal output are covered in this Application Note, one with an oscilloscope and one with a counter.

The first example is using the 1601L Logic State Analyzer for functional checks and an oscilloscope for electrical measurements to determine why a two decade BCD counter is not operating properly. After connecting the Analyzer to the counter, the Analyzer is set to trigger on state 00 BCD, and digital delay is used to functionally check out operation. Scanning the counter sequence shows that it does not count to 99 but resets to 00 at state 89 (figure 1). This check shows that the first decade is operating properly, so the problem must be in the second decade. Since there are no superimposed ones and zeros displayed on the Analyzer in the second decade the problem is not intermittent. Further, since each output has toggled at least once, the master reset is suspected to be the problem source. Analysis with an oscilloscope should pinpoint the problem.
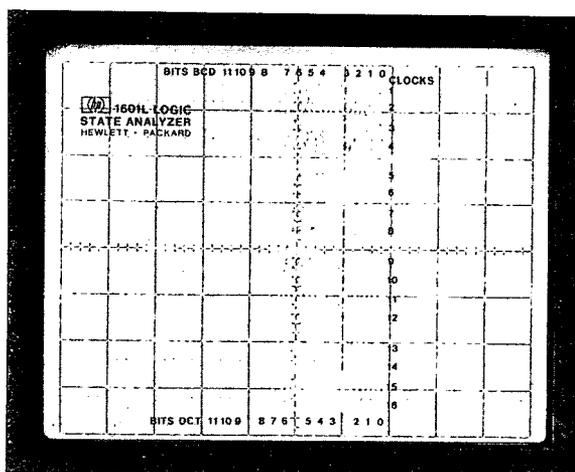

Figure 1. Functional analysis clearly shows a two decade counter resetting to zero at state 89 rather than state 99.
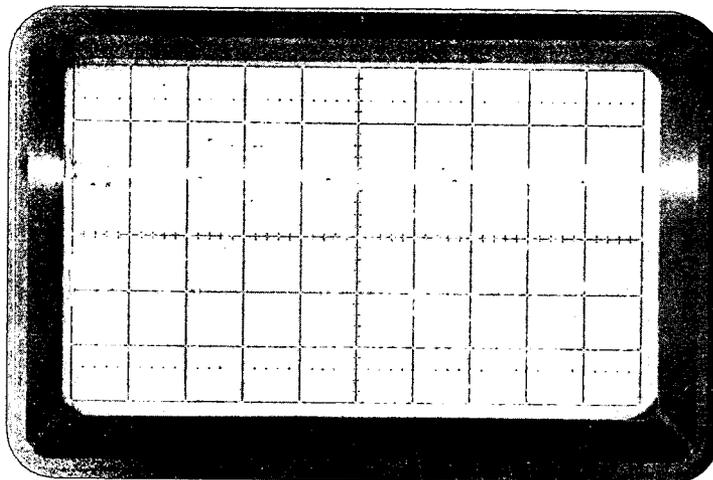

Figure 2. Electrical analysis of the counter reset line shows several pulses that could cause erroneons reset.

Connecting the oscilloscope probe to the master reset line shows several pulses (figure 2) that could cause a problem. Since the oscilloscope is not referenced to a particular digital point in time, the pulse that is causing the problem is not readily apparent. Connecting the Analyzer Trigger Output

signal to the oscilloscope external trigger input and setting the Analyzer trigger switches to the functional problem point references the oscilloscope measurement to the digital time frame. Setting the Analyzer trigger pattern to 89 triggers the oscilloscope in the proper time frame and clearly shows the glitch on the reset bus that is causing the malfunction. Note: if the oscilloscope vertical amplifier does not have a delay line the Analyzer trigger may be reset to 88 or 87 to position the glitch toward the center of the scope display for better viewing (figure 3).
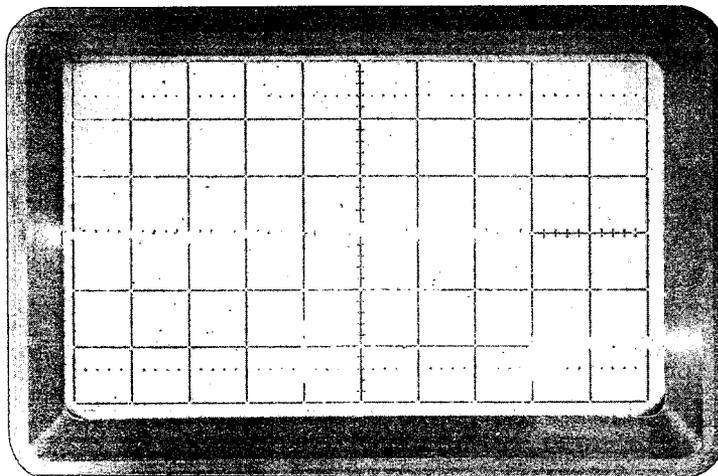
Figure 3. Externally triggering the oscilloscope at the proper digital point in time clearly pinpoints the glitch on the reset bus.

In the second example, a counter is used to check the timing of a pen-lift command in a digital plotter. A wait loop in the plotter is designed to raise the pen off the paper before it moves to prevent smearing. In this case, it is necessary to verify that the pen lift wait loop is long enough for the pen to lift off the paper. By selecting state 33_8 as the trigger word which is the start of the pen lift wait loop, and connecting the trigger output to a counter, the number of times the program cycles through state 33_8 will be recorded. The count is 13, 038 which is the correct number for the pen lift sequence. Time is calculated by multiplying the number of states in the loop by the clock period in seconds to obtain the total time in the pen lift wait loop.

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