Errata

Document Title: Functional Analysis of National Semiconductor SC/MP Microprocessor System (AN 167-18)

Part Number: 5952-2025

Revision Date: January 1975

HP References in this Application Note

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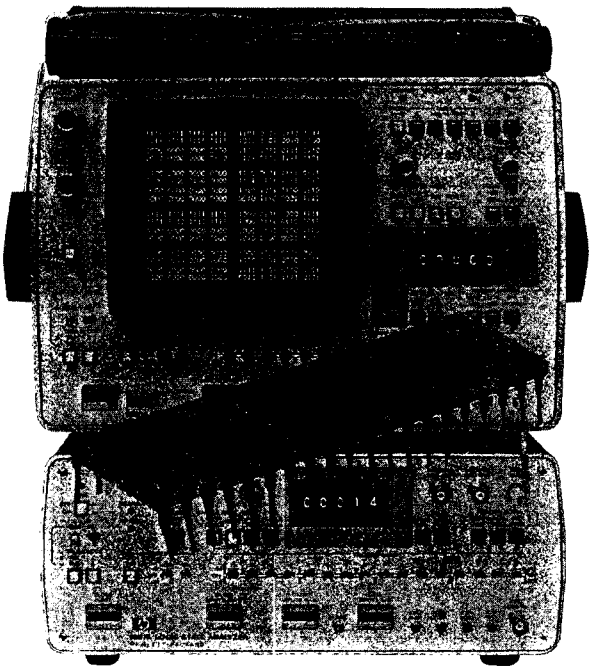
APPLICATION NOTE 167-18
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of National Semiconductor SC/MP microprocessor system.



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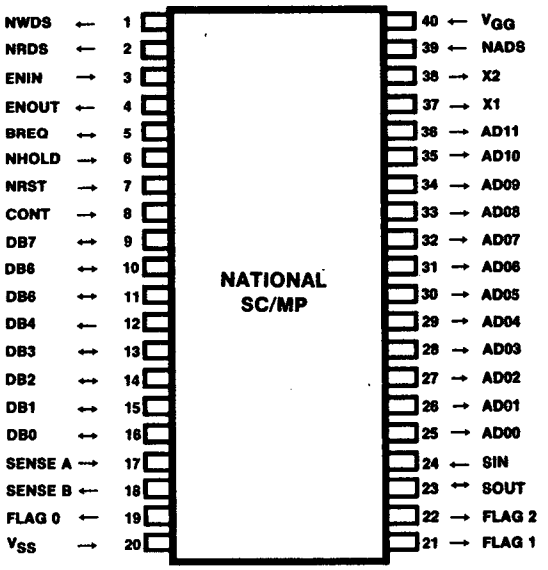
1. INTRODUCTION

This application note is designed to assist the user of the National Semiconductor SC/MP microprocessor in the real time analysis of his system in both design and troubleshooting environments. The note demonstrates real time analysis of actual program sequences, triggering on specific events, use of the map, paging technique, and observation of information flow on the data bus.

The SC/MP is a single-chip microprocessor packaged in a 40-pin DIP package and intended for use in general-purpose applications. The chip has self-contained timing circuits (frequency is set with an external crystal or capacitor), 16-bit addressing capability, and serial and parallel data transfer capability. The Central Processing Unit (CPU) contains an 8-bit data bus and a 12-bit address bus as well as three pointer registers capable of automatic incrementing or decrementing. The architecture makes possible a very low-cost system including internal I/O ports and compatability with most standard TTL/CMOS components.

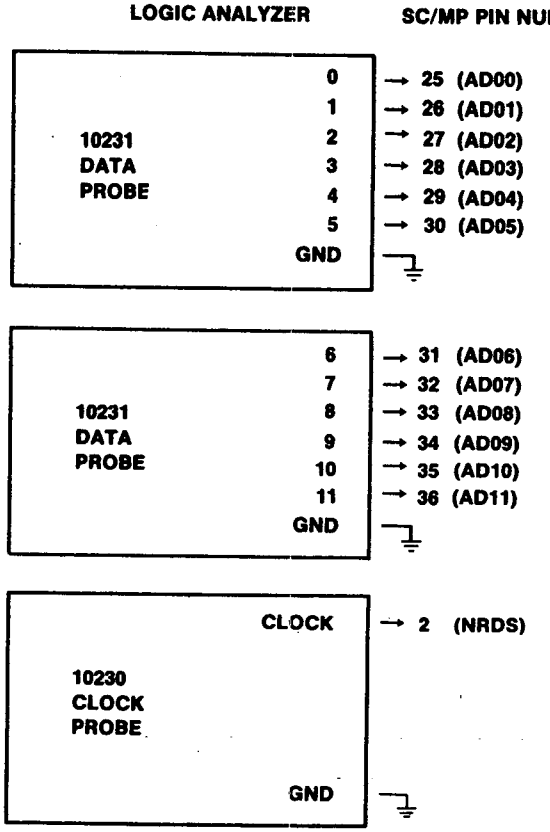
2. PIN ASSIGNMENTS



PIN NAME	FUNCTION
DB0-DB7	Data Bus
AD00-AD11	Address Bus
FLAG 0-FLAG 2	User Assigned, General-purpose Bit
X1, X2	To Ext Timing Xtal/Cap.
NWDS	Write Strobe Output
NRDS	Read Strobe Output
ENIN	Enable Input
ENOUT	Enable Output
BREQ	Bus Request Input/Output
NHOLD	Hold Lengthens Input/Output Cycle
NRST	Reset Input
CONT	Continue Input
SENSE A-SENSE B	General Purpose Status Inputs
NADS	Address Strobe Output
SIN	Serial Input
SOUT	Serial Output
V_{SS}	Positive Supply Voltage
V_{GG}	Negative Supply Voltage

3. PROBE CONNECTIONS

A system that will not "come up" can frequently be debugged by monitoring address flow alone. With the SC/MP, the following Logic State Analyzer Probe connections will display activity on the SC/MP Address Bus.



4. SETTING THE CONTROLS

Turn power on to the Logic State Analyzer and set controls as follows:

Display Mode	Table A
Sample Mode	SGL
Start Display	ON
Trigger Mode	WORD
Threshold	TTL
Clock	⌐¯
All other pushbuttons	Out Position
Display Time	ccw
Column Blanking	Display 12 bits
Qualifiers	OFF
Trigger Word Switches	Set to Address at which you wish to trigger*

*If program is not looping or cycling through the selected address, press RESET and start your system. The first time the system passes through the selected trigger state, the display will be generated and stored.

5. DISPLAY INTERPRETATION

Figure 1 shows the display of information on the address bus (A) and the program from which it was derived (B). This figure will help you understand the Logic State Analyzer display. Your own program will do equally well. Proper system program operation is verified by a comparison of the table display with the program listing.

The entire program can be viewed in 16 word "Pages" by resetting the trigger word switches to correspond to the last (16th) word in each successive display. This paging technique can also be accomplished by using the Digital Delay thumbwheel switches advanced in increments of 16.

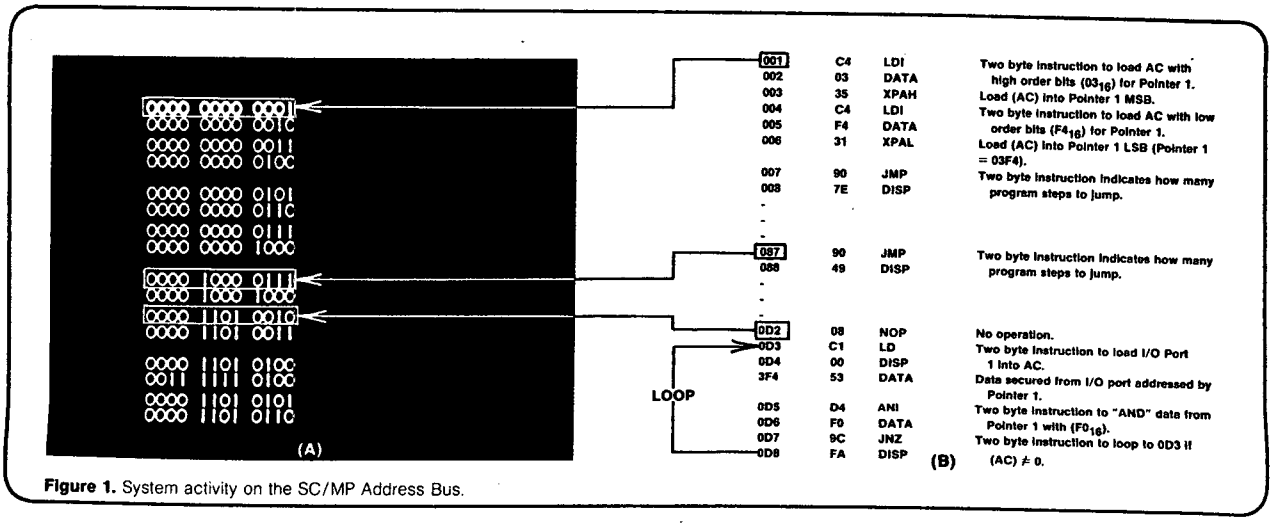


Figure 1. System activity on the SC/MP Address Bus.

6. THE MAP

If a tabular display is not presented in the previous step, it means that the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program, switch to "map" (figure 2). The Logic State Analyzer trigger word switches are now operating in their cursor positioning mode. Use the trigger word switches to position the cursor (circle) over one of the dots on

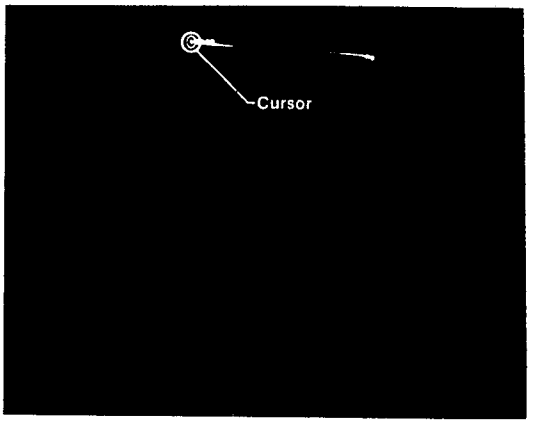


Figure 2. Map Display Shows Entire System Activity.

screen. Switch to MAP EXPAND and make the final positioning. The no trigger light will now go out and pressing Table A pushbutton will display the 16 address words beginning at the point located with the cursor.

7. VIEWING ADDRESS AND DATA LINES

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the Data Bus or in peripheral memory. Additional input channels now become very desirable. By combining the 1600A and the 1607A the display and trigger capability can be expanded to 32 bits wide, allowing the full 16 bits of address, 8 bits of data, and eight other active lines to be viewed simultaneously. Connect the instrument as follows:

1. Connect the data cable between rear-panel connectors.
2. Connect trigger bus cable between instrument front panel bus connectors.
3. Select Trigger mode "WORD" on 1600A.
4. Select "BUS" and "OFF" on the 1607A.
5. Select "Start Display", SAMPLE MODE "Single" on both Analyzers, and TABLE "A&B" on the 1600A.
6. Set Threshold and Logic Polarity on 1607A to be the same as the 1600A.
7. Leave all other pushbuttons "out" on 1607A.
8. Leave the 1600A set up as in Section 3.
9. Connect data and clock inputs for 1607A to the SC/MP as follows:
   a. Data inputs on 1607A 0 through 7 to SC/MP DB0 through DB7 respectively.
   b. Clock input to SC/MP pin 2.
   c. Grounds to appropriate point(s).
10. Press "Reset" on both Logic State Analyzers and restart system.
11. Set Column Blanking on 1607A to display 8 columns.

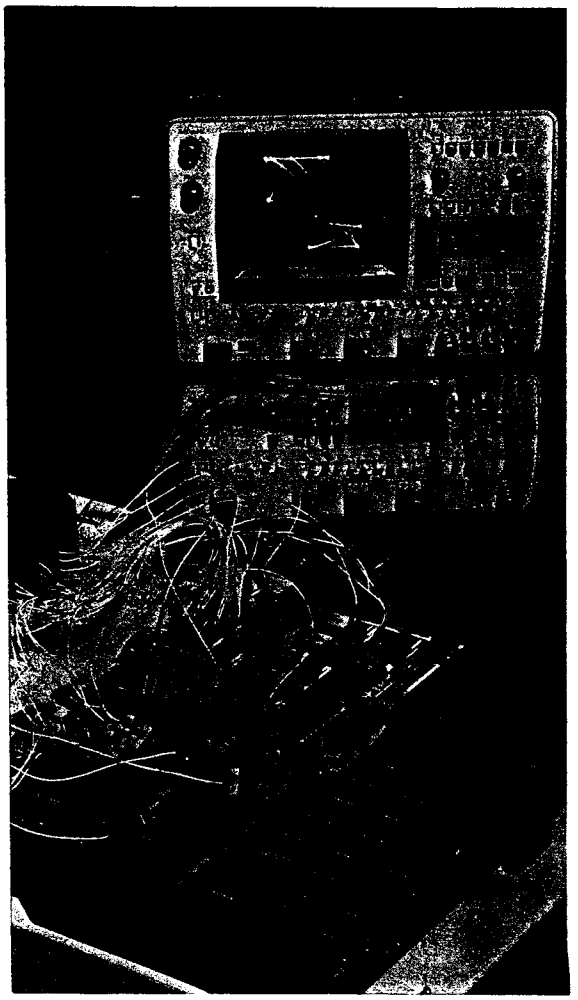


Figure 3. Typical Test Setup of 1600A and 1607A for Displaying up to 32 Bits of Information.

8. DISPLAY INTERPRETATION OF ADDRESS AND DATA BUSES

Operating the Logic State Analyzer system as set up in section seven, the display shows all the activity on the address and data buses during system operation. Even though there is a 16-bit address register in the SC/MP, the output is not latched in our test system and the display shows only what is on the 12-bit address bus.

Figure 4A is the Logic State Analyzer display of address and data activity in the SC/MP while operating from the program listed in figure 4B. The first six program steps load an 8-bit address into Pointer 1 for use later in the program. At program step 008 and 088, the program calls for a jump to address 0D2, and by examining the display you can see these jump instructions being executed. The next portion of the program loads data from I/O Port 1 into the accumulator. Pointer 1 addresses I/O Port 1 and it is here that the address 03F4 from earlier steps is used. The display shows that each of these program steps is completed accurately. Similiar analysis will show the implementation of each instruction in the program.

9. CONCLUSION

From the foregoing examples, it may be concluded that efficient troubleshooting of National Semiconductor SC/MP μP systems is expedited by two factors. First: availability of the program listing, the definitive document of program execution; and Second: the availability of real time Logic State Analysis to display system operation in terms of actual logic bits for rapid error detection and correction.

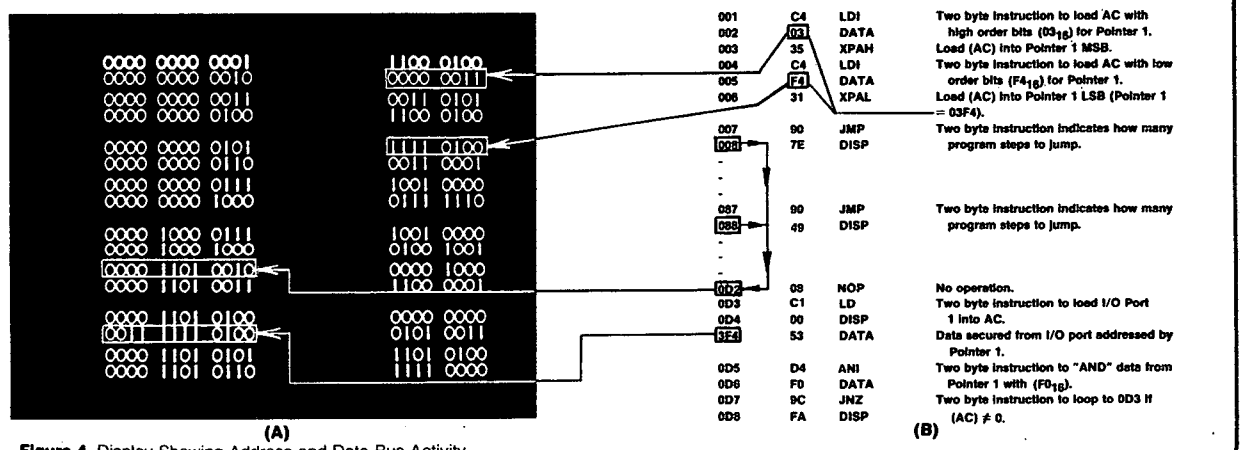


Figure 4. Display Showing Address and Data Bus Activity.

Application Notes in the 167 series with the primary instrument(s) used in parenthesis.

167-1 The Logic Analyzer (5000A).
167-2 Digital Triggering for Analog Measurements (1601L).
167-3 Functional Digital Analysis (1601L).
167-4 Engineering in The Data Domain Calls for a New Kind of Digital Instrument (Describes measurement problems and various solutions with applicable instruments.)
167-5 Troubleshooting in the Data Domain is Simplified by Logic Analyzers (1600A and 1607A).
167-6 Mapping, a Dynamic Display of Digital System Operation (1600A).
167-7 Supplementary Data from Map Displays without Changing Probes (1600A).
167-8 Stable Displays of Disc System Waveforms Synchronized to Record Address (1620A).
167-9 Functional Analysis of Motorola M6800 Microprocessor Systems (1600A and 1607A).
167-10 Using the 1620A for Serial Pattern Recognition (1620A).
167-11 Functional Analysis of Intel 8008 Microprocessor Systems (1600A and 1607A).
167-12 Functional Analysis of Fairchild F8 Microprocessor Systems (1600A and 1607A).
167-13 The Role of Logic State Analyzers in Microprocessor Based Designs (1600A and 1607A).
167-14 Functional Analysis of 8080 Microprocessor Systems (1600A and 1607A).
167-15 Functional Analysis of Intel 4004 Microprocessor Systems (1600A and 1607A).
167-16 Functional Analysis of Intel 4040 Microprocessor Systems (1600A and 1607A).
167-17 Functional Analysis of National IMP Microprocessor Systems (1600A and 1607A).
167-18 Functional Analysis of National Semiconductor SC/MP Microprocessor Systems (1600A and 1607A).
167-19 Systematic "turn-on" of μP Systems using Logic State Analyzers (1600A and 1607A).

VIDEO TAPE SERIES: The four hour series titled "The Data Domain Its Analysis and Measurements" introduces logic state analysis and measurement techniques unique to the data domain. Contact your HP Field Engineer for price and availability of this color tape series.

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