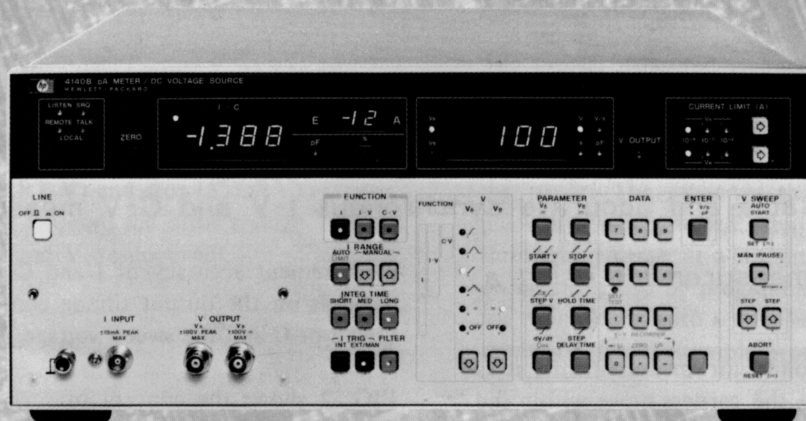
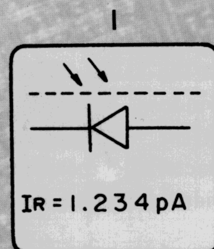
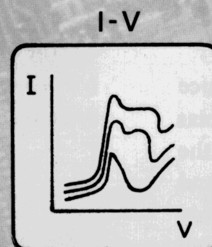
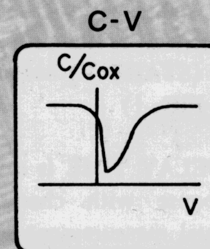
SEMICONDUCTOR MEASUREMENTS WITH THE HP4140B PICOAMMETER/ DC VOLTAGE SOURCE









A COMPLETE SOLUTION---

- Three Basic Semiconductor Measurement Capabilities:
  - I-V: I-V characteristics measurements,
  - C-V: Quasi-Static C-V measurements, and
  - I: Pico-Ampere measurements.
- An extremely stable digital pA meter with 10^{-15}A resolution (even at the probe station) plus two built-in programmable DC Voltage Sources.
- Wide current measurement range: 10^{-2}A down to 10^{-12}A, with automatic ranging capability.
- HP-IB capability for easy systemization into a DC parameter or process test system.

HEWLETT PACKARD

Introduction

This application note describes how to easily make very low current measurements **(down to 10^{-15} A)** and quasi-static capacitance-voltage measurements with the HP 4140B. These measurements can offer **improved production yields** and also aid in the **development of higher performance semiconductor devices.**

Previously, measurements that required test voltages supplied from an external source also required the building of a system. Such systems included a pA meter, voltage sources, test fixtures, and appropriate overall control. These systems were usually large and expensive. Also, noise problems and measurement timing problems made the systems difficult to use. **The 4140B pA Meter/DC Voltage Source** offers a better solution. The 4140B includes a pico ammeter and two built-in dc voltage sources. And all measurements are controlled and properly synchronized by a single internal microprocessor.

I. Low current semiconductor measurements

---How to obtain stable and accurate synchronous I-V and C-V measurements---

● Synchronous I-V measurement using a staircase sweep

In very low current semiconductor measurements, it is important to determine how the carriers move within the semiconductor. The 4140B includes a voltage sweep for automatic current measurement. The 4140B also initially sets the (1)**HOLD TIME** to stabilize the DUT (device or material under test) with respect to its properties. This is done using a bias voltage **(START V)** before the automatic sweep is started. (See FIG. 1)

In addition, the (2)**STEP DELAY TIME** is set to reduce undesireable transient response with changes in bias voltage **(STEP V)**. The actual measurement starts at the end of **STEP DELAY TIME**, after the step changes. And the measured current is displayed or output simultaneously with the actual bias voltage value. To obtain the desired accuracy and stability of measurement, a **SHORT, MED** or **LONG** measurement time can be selected.

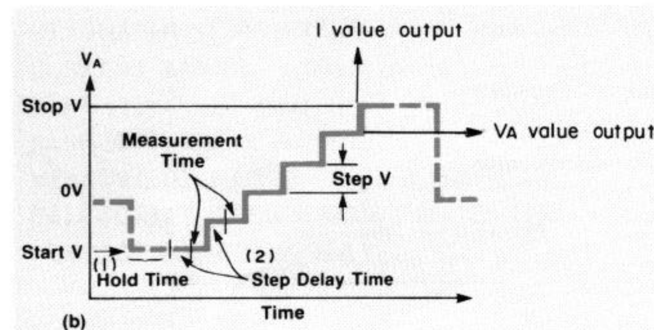


FIG. 1 Synchronous I-V measurement for sweep

● Synchronous I-V and C-V measurement with ramp sweep

I-V and C-V measurements usually employ a sweep voltage with a constant ramp rate dV/dt (0.001 V/s - 1V/s). The measurement accuracy of I and C at a given bias voltage depends on the output timing control between the measured I or C and the sweep voltage.

FIG. 2 shows the concept of such a synchronous I-V or C-V measurement. The **HOLD TIME** can be previously set to provide a waiting time for stabilizing the DUT at an initial bias voltage. In the sweep measurement, the I or C value is averaged in a measuring time window. The displayed V value is the value obtained at the center of the measuring time window. The unique timing control in the 4140B pA Meter/DC Voltage Source offers more exact I-V or C-V characteristic measurements than by merely systemizing individual instruments.

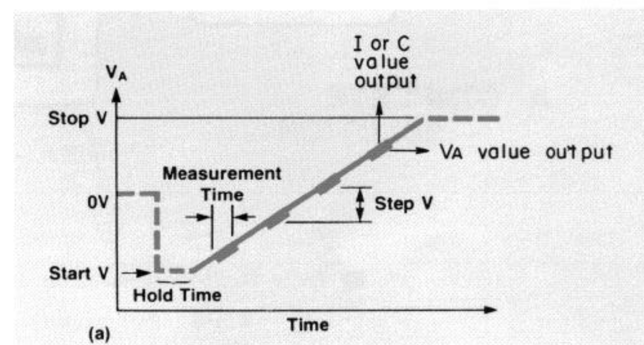


FIG. 2 I-V or C-V measurement with ramp sweep

---Protecting sensitive DUT's (devices under test) from destruction---

For both built-in voltage sources of the 4140B, there are three kinds of DUT protection:

1) **absolute current limiting** by the output current limiter at 100μA, 1mA, and 10mA,
2) **simultaneous output voltage change** in V_A and V_B is provided, and
3) **no overshoot in step voltage changes** because of the nominal slew rate of 1V/ms.

APPLICATION: I_D-V_{GS}, I_D-V_{DS} measurements of MOS FET

One of the DC parameter measurements used in MOS device evaluations is the I_D-V_{GS} characteristics measurement in the subthreshold region. Such subthreshold characteristic measurment requires an ammeter with a very **wide current range**. Also required are **two voltage sources**: one which drives V_{GS} (gate voltage) and another which supplies V_{DS} (drain voltage).

When making the I_D-V_{GS} measurement, the 4140B controls are first preset, and the AUTO START KEY is pressed. The DUT properties are automatically measured by the 4140B between the start (START V) and stop (STOP V) voltages. The measured value for I_{DS} and the drive voltage V_{GS} are displayed on displays-I and V, respectively.

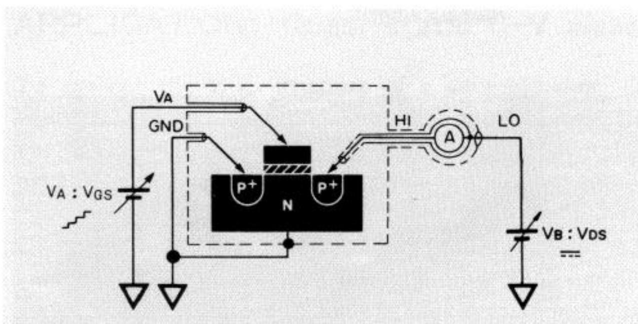


FIG. 3 I_D-V_{GS} measurement

For very low current measurement in subthreshold region, a shielded box for probe station and floating probes are necessary.

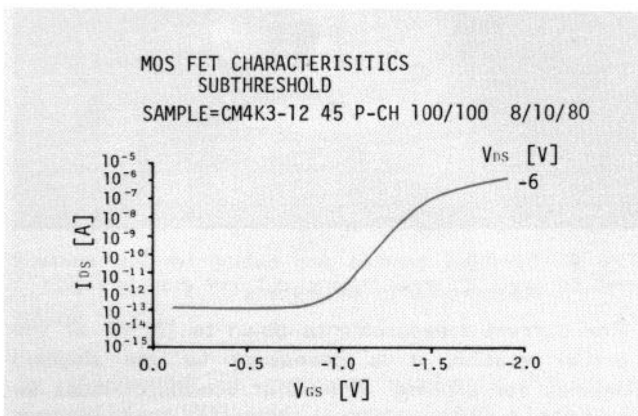


FIG. 4 I_D-V_{GS} characteristics in subthreshold region

In this case, sweep voltage automatically maintains its value until the measured current value becomes stable and displays an optimum value (rejecting any transient ranging pulse change).

Use of the 4140B will simplify test connection, and increase measurement speed and accuracy.

The typical measured characteristics of I_D-V_{GS} are shown in FIG. 4. The 4140B offers flexible measurement with its PAUSE key function. The PAUSE function stops the sweep and enables a step voltage change to be made during the pause. The sequence then restarts automatically (or manually) and proceeds step by step -- to search for the threshold voltage at a nominal current value. These procedures can also be programmed by an HP-IB Controller -- for example, as auto search in a threshold voltage measurement. (Refer to example program on page 7.)

If the DUT is already packaged in T0-5 or dual-in-line packages, the **16055A Electro-static light shielded Test Fixture can be useful.** (See FIG. 5)

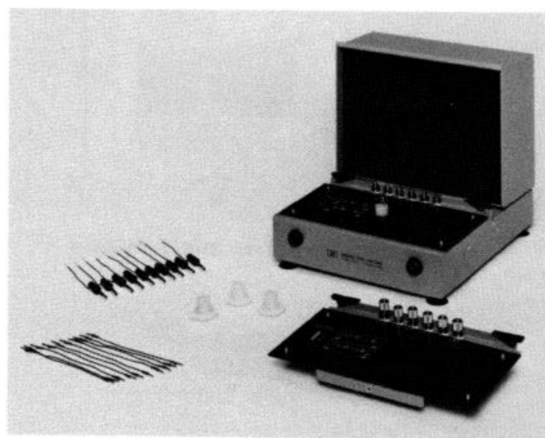


FIG. 5 16055A Electrostatic and light shielding Test Fixture

Accessory test fixture provides electrostatic and light shielding for the device under test. One connection plate is provided for use with the clip leads (included) and a second plate is provided for TO-5 type sockets.

APPLICATION: I_R-V_G measurement of gated diode in wafer test

Most test patterns for process evaluations of the so-called TEG (test element group), include a gated diode pattern for evaluation of carrier generation and recombination properties at the Si-SiO_2 surface. This causes a large reverse current at the PN-junction which, in turn, contributes to the degradation of the device. However this technique can help identify packaged MOS-FET's with high drain leakage current or low breakdown voltage between the drain and source. It also permits selection of reliable devices with long lifetimes at a relatively early production stage. This evaluation method is called a reverse bias PN junction current (I_R) measurement. The gate voltage (V_G) is varied from accumulation through depletion. An inversion layer is created in the substrate under the SiO_2 layer by applying a reverse bias (V_R) at the PN junction. (See FIG. 6)

In this application, the 4140B measures and displays I_R values with a **resolution of 10^{-15}A (1fA).** Two built-in programmable voltage sources (V_A for V_G and V_B for V_R) are automatically controlled during the measurements.

Special guarding and shielding arrangements must be made when measuring current values under 10^{-12}A. A typical arrangement with the 4140B is shown in FIG's 8 and 9.

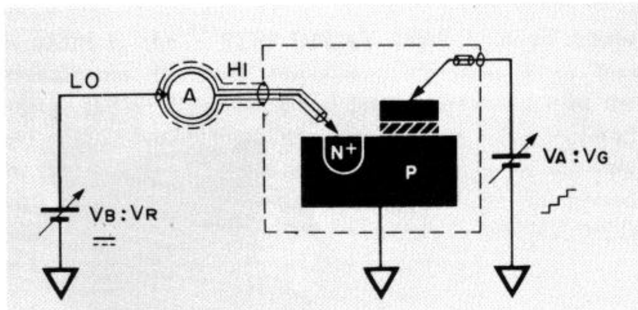


FIG. 6 Gated diode measurement

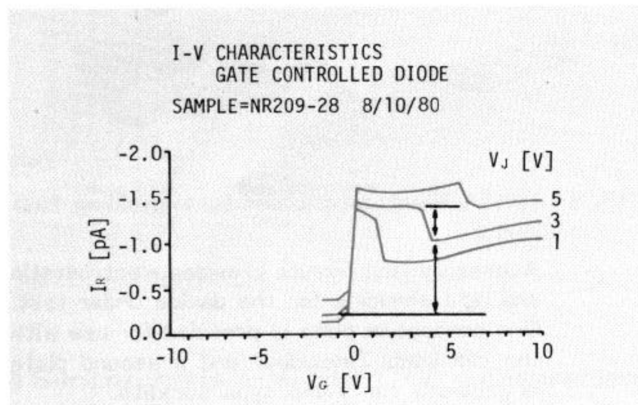


FIG. 7 Gated diode characteristics

High resolution pA Meter is necessary for this measurement.

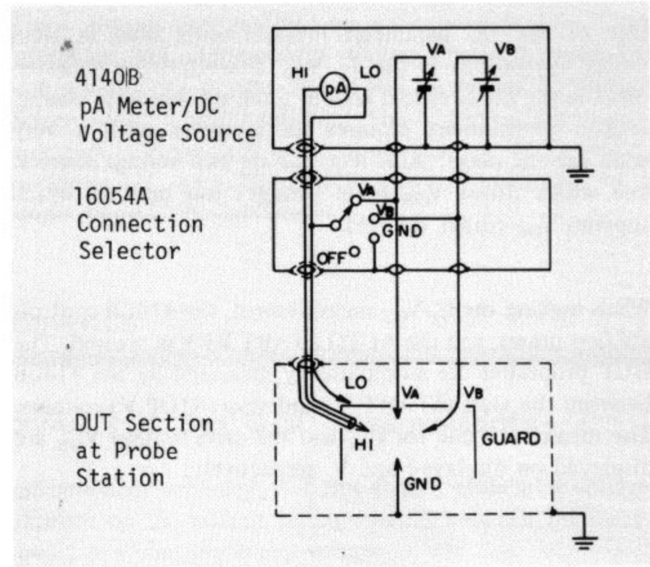


FIG. 8 Typical arrangement for low current measurement

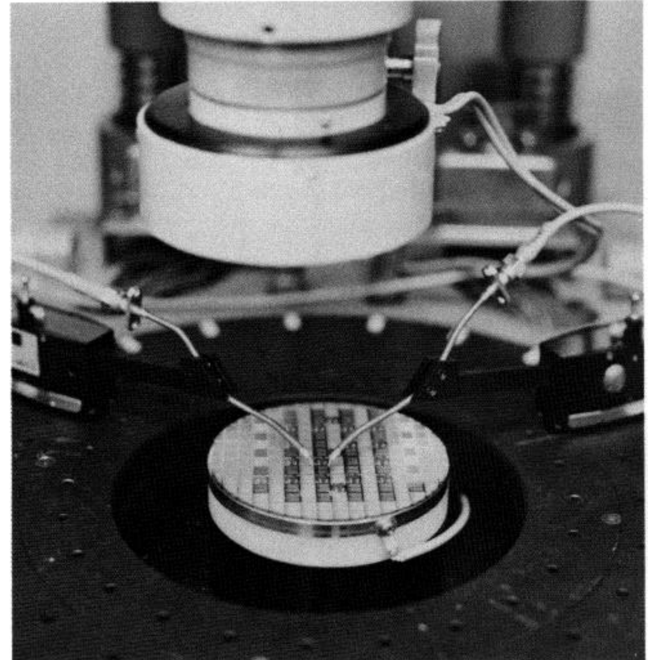
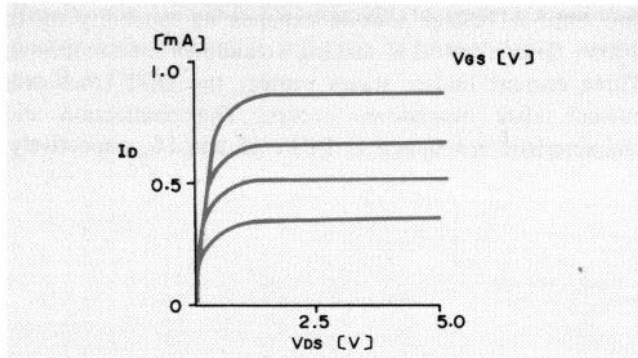


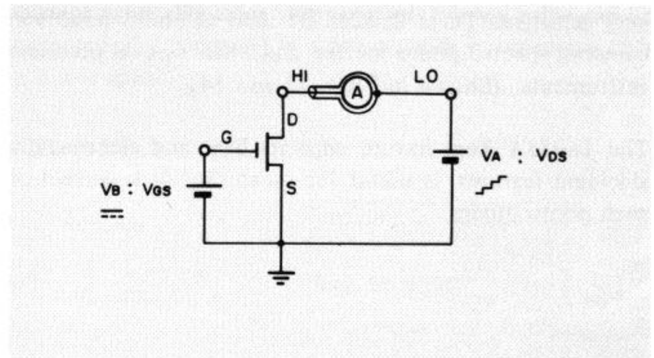
FIG. 9 Shielded needles and cables for low current measurements of wafers

For current measurements down to 10^{-15}A at the prober station, it is necessary to use shielded needles for probing. The outer conductor must be connected to the LO input terminal of the pA Meter (see FIG. 9). The entire probe station should be enclosed in a grounded metal box. This arrangement will reduce leakage current between the HI input terminal and ground, and reject noise from surrounding equipment.

By using the LOW lead connection switch on the 16054A Connection Selector or 16055A Test Fixture low lead connection changes to the pA Meter can easily be made. For example, the I_D-V_{DS} characteristics shown in FIG. 10 (a) can be easily obtained by simply reversing the V_A and V_B connections in FIG. 3. The resulting connection is shown in FIG. 10 (b).



(a) I_D-V_{DS} characteristics



(b) Connection for I_D-V_{DS} characteristics measurement

FIG. 10

APPLICATION: Quasi-static C-V measurement of an MOS structure

To analyze the MOS structure of a semiconductor, the 4140B provides a quasi-static C-V measurement method in one instrument. This method is useful for determining the properties of the minority carriers generated at the surface of the oxide layer. Quasi-static results also determine the C-V characteristics at high frequency (1 MHz). These measurements provide significant information such as impurity profile (doping profile) of surface state density which are useful when evaluating device quality.

The quasi-static C-V method requires a sweep bias voltage with a very **slow and stable ramp rate (down to 1mV/sec).** This is necessary to create an equilibrium state for various weighted carriers -- and is why this method is called "quasi-static." A waiting time corresponding to the lifetime of the carriers in the DUT is necessary before the sweep starts.

In this application, the quasi-static C is calculated from the measured current I divided by the constant voltage change or ramp rate dV/dt.

$$C = \frac{I}{dV/dt} \text{ farads}$$

C values at very low frequencies (near DC) can be determined.

An arrangement for measuring quasi-static C-V characteristics of an MOS diode is shown in FIG. 11. Once the 4140B is preset in accordance with the properties of the DUT -- the operator then only needs to press AUTO START. This enables generation of the C-V characteristic curve (as shown in FIG. 12) between the START V and STOP V.

The C-V measurement is synchronously done as described on page 2, so that measured capacitance values without voltage shift can be reliably used for calculation of surface state density (See Appendix A) or for comparison with an ideal C-V curve.

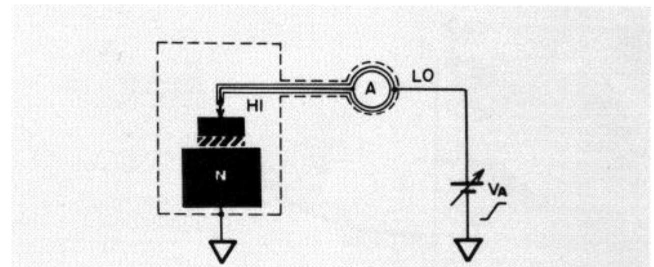


FIG. 11 Quasi-static C-V measurement on MOS diode

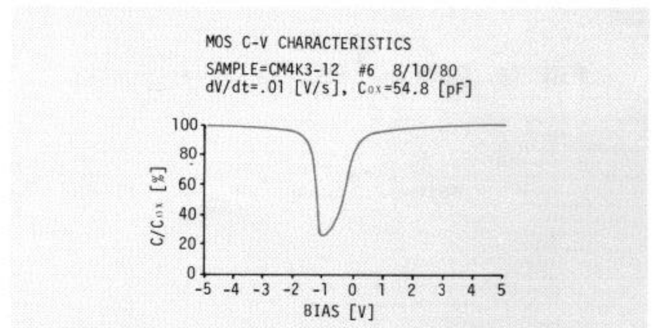


FIG. 12 Quasi-static C-V characteristics curve

Cox value can be entered, so that the displayed value can be selected as C (pF) or C/Cox (%) normalized by oxide layer capacitance Cox.

APPLICATION: Dark current vs bias measurement

The development of photo diodes in which the dark current is 10^{-12}A or less has led to photo detectors which are very sensitive. These devices are used as photo sensors in cameras, spectro photo meters, and other optical precision instruments. (Shown in FIG's 13 and 14)

The 16055A Test fixture with its light and electrostatic shielding features, is useful for measuring dark current of such photo diodes.

The breakdown voltage of diodes is distributed over a wide range. To adapt to this need, the cascade use of the 4140B's two built-in voltage sources expands its capability up to 200V. This is useful in making breakdown measurements. Three current limiter stages protect the DUT from over current after breakdown occurs. The connection and characteristic are shown in FIG's 15 and 16, respectively.

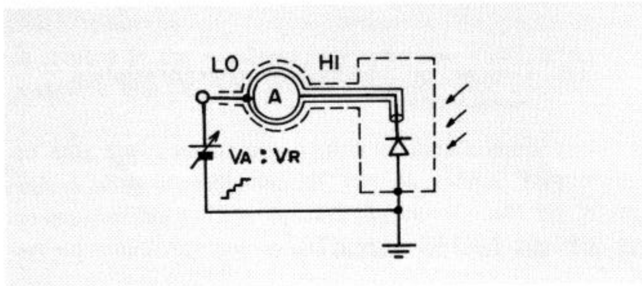


FIG. 13 Dark current measurement circuit

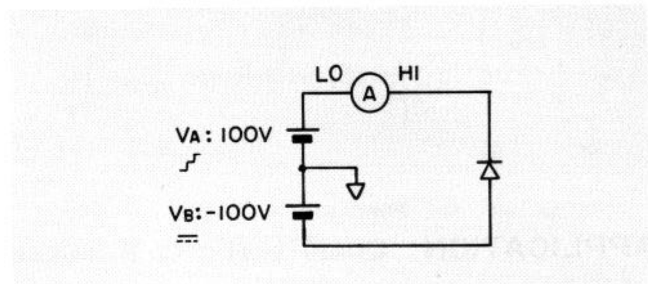


FIG. 15 Cascade use of two built-in voltage sources expands bias voltage range to 200V.

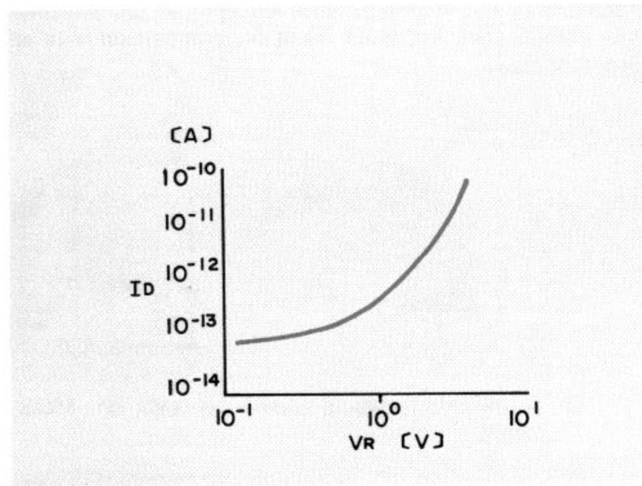


FIG. 14 Dark current-bias characteristics

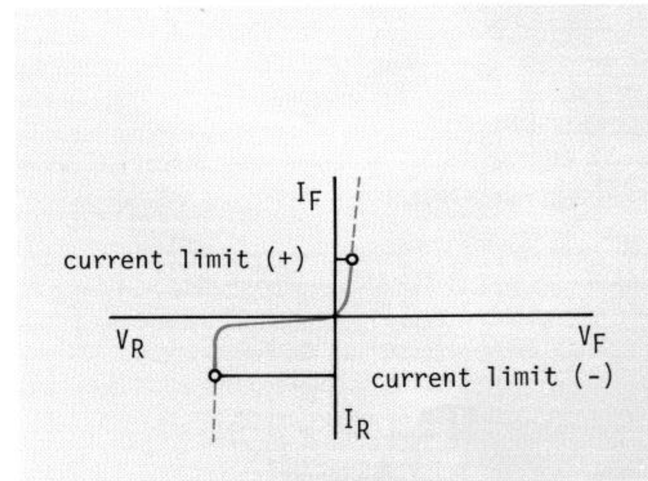


FIG. 16 Diode I-V characteristic

"All keys on the 4140B front panel can be controlled from the HP-IB by one of the many available HP-IB controllers. An HP-IB system can obtain accurate measurement data very quickly and analyze the data within the controller. Results can be used, for example, to control a semiconductor wafer process in real time or to save design time in the R & D lab."

HP-IB capability expands the 4140B functions to automatic measurements, data analysis and characteristic graphic plotting. The sample program given in Table 1 shows automatic searching for threshold voltage (V_{th}) at a nominal current value. By using this program, the V_{th} value can be automatically measured in a few seconds by sweeping over a 2 volt span.

```
10    ! Threshold Voltage Measurement (VthA/N)                                  Aug.09,1980
20    ! HP4140B+9835A      used for 4140B A/N
30    PRINT PAGE
40    PRINT "THRESHOLD VOLTAGE MEASUREMENT"
50    Flag=0
60    Inst=717
70    INPUT "4140B ADDRESS CODE ?  (717)",Inst
80 Meas:CALL Meas_para_entry(Flag,Sample$,Channel$,Vd,Ith,Vth_upper,Vth_lower)
90     CALL Vth_measurement(Flag,Inst,Channel$,Vd,Ith,Vth_upper,Vth_lower,Vth)
100    BEEP
110    PRINT USING "18A,A,M3D.2D,K";Sample$,":",Vth,"V"
120    Flag=1
130   GOTO Meas
140   END
150   !
160   SUB Vth_measurement(Flag,Inst,Channel$,Vd,Ith,Vth_upper,Vth_lower,Vth)
170     DISP "THRESHOLD VOLTAGE MEASUREMENT"
180 Image:     IMAGE 2A,M3DZ.2D,","
190     Vth=0
200     C=(UPC$(Channel$)="P")
210     IF C=1 THEN 250
220     Stop=PROUND(MIN(Vth_lower,Vth_upper),-2)
230     Start=PROUND(MAX(Vth_lower,Vth_upper),-2)
240     GOTO 270
250     Start=PROUND(MIN(Vth_lower,Vth_upper),-2)
260     Stop=PROUND(MAX(Vth_lower,Vth_upper),-2)
270     Step=ABS(PROUND(Start-Stop,-2))
280     IF Flag=1 THEN 330
290     OUTPUT Inst;"F2RA1I1"
300     OUTPUT Inst;"C0A3B1L3M3S0J1H09"
310     OUTPUT Inst USING Image;"PB",Vd
320     OUTPUT Inst USING Image;"PS",Start,"PT",Stop,"PE",Step,"PH",0,"PD",.01
330     OUTPUT Inst;"W2"
340     IF C=1 THEN 380
350     J=1
360 Step: Step=MAX(PROUND(Step*.5,-2),.01)
370 Set: OUTPUT Inst USING Image;"PE",Step
380     IF (I>Ith) AND (C=0) OR (I<Ith) AND (C=1) THEN GOSUB Down
390     IF (I<Ith) AND (C=0) OR (I>Ith) AND (C=1) THEN GOSUB Up
400     ENTER Inst;I,V
410     I=ABS(I)
420     IF ABS(I)=Ith THEN Meas_end
430     IF SGN(I-Ith)*SGN(J-Ith)=1 THEN GOTO 450
440     IF (ABS(I-Ith)=MIN(ABS(I-Ith),ABS(J-Ith))) AND (Step=.01) THEN Meas_end
450     J=I
460     IF Step=.01 THEN GOTO Set
470  GOTO Step
480 Down: OUTPUT Inst;"W5"
490  RETURN
500 Up: OUTPUT Inst;"W6"
510  RETURN
520 Meas_end: Vth=V
530     OUTPUT Inst USING "K";"W7"
540  SUBEXIT
550  SUB Meas_para_entry(Flag,Sample$,Channel$,Vd,Ith,Vth_upper,Vth_lower)
560   EDIT "CONNECT/CHANGE DUT and EDIT SAMPLE NUMBER?  (max 18 chara)",Sample$
570   IF Flag=1 THEN 640
580   INPUT "Channel?  (P or N)",Channel$
590   INPUT "Vd (V)?",Vd
600   INPUT "Ith (uA)?",Ith
610   Ith=Ith/1E6
620   INPUT "Vth upper limit (V)?",Vth_upper
630   INPUT "Vth lower limit (V)?",Vth_lower
640  SUBEND
```

Table 1. Vth measurement program

Appendix A: Quasi-static C-V measurement for evaluation of an MOS device in the manufacturing process

The quasi-static technique determines the low frequency thermal equilibrium MOS cpacitance-voltage characteristics. With this technique, surface potential and surface state density can be obtained relatively simply over a large part of the energy gap on a single sample. Such measurement also provides a direct test for the presence of gross non-uniformities in MOS structures. By knowing the surface state density, the present production process can be evaluated and feedback treatment can be applied. This can reduce non-uniformity for obtaining a higher quality and more reliable MOS device.

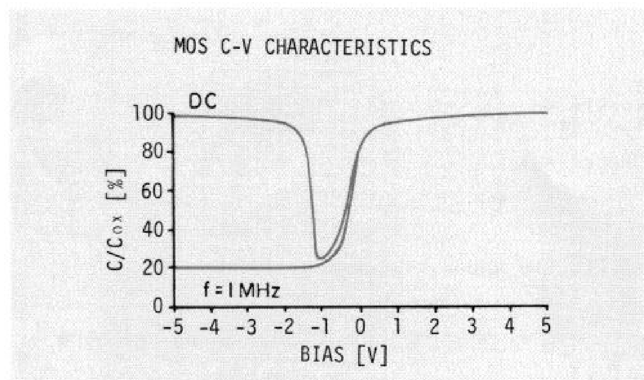


FIG. 17 MOS C-V characteristics

By measuring both C-V characteristics, the surface state density can be calculated below from the following equation.

If this low frequency technique is used alone, it would be difficult to calculate surface potential and surface state density. But by doing both a C-V measurement at high frequency and a quasi-static measurement, the complicated equation can be simplified to the following for surface state density, N_{SS}:

$$N_{SS} = \frac{C_{SS}}{q} = \left[\frac{C_{LF}C_{OX}}{C_{OX} - C_{LF}} - \frac{C_{HF}C_{OX}}{C_{OX} - C_{HF}}\right] \cdot \frac{1}{q}$$

where C_{SS} : **surface capacitance,**
$q = 1.602 \times 10^{-19}$ **coulomb**
C_{LF} : **quasi-static capacitance**
C_{HF} : **high frequency capacitance**
C_{OX} : **oxide layer capacitance**

Reference

1) Kuhn, M. 1970. *Solid-State Electronics,* vol. 13, p. 873.
2) Noguchi, H. 1979. *Hewlett-Packard Journal,* vol. 30, no. 12, pp. 10-19.

4140B SPECIFICATIONS

MEASUREMENT FUNCTIONS: I, I-V and C-V
CURRENT RANGE: 0.001×10^{-12}A – 1.999×10^{-2}A
DISPLAYS: 3-1/2 digits
BASIC ACCURACY: 0.5%
MEASUREMENT TIME: Approx. 4ms – 2.56s
CALCULATED CAPACITANCE RANGE: 0.1pF – 1999pF
VOLTAGE SOURCE (V_A and V_B): 0.00 to ±100.0V

Function	V_A	V_B
I		
I-V		
C-V		

RAMP RATE: 0.001V/s – 1.000V/s
SWEEP MODE: Auto/Manual (Pause)

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