Practical Design and Evaluation of High Frequency Circuits

Using the HP4193A Vector Impedance Meter



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Figure 1-1. 4193A Vector Impedance Meter

1. INTRODUCTION

1.1 Preface

Have you ever designed an electronic circuit only to find that once it was built, it didn't work the way you intended it to. You have probably run into this sort of problem when working with electronic circuits that will operate somewhere between the HF and VHF bands. Such differences can usually be accounted for by three factors which affect circuit performance in the high frequency band, but not in the low frequency band. These factors include the following:

- Circuit components do not always work across an actual operational frequency range the way they theoretically should.
- At high frequency bands, printed circuit board patterns exhibit high impedance that cannot be ignored.
- The way components are packaged or laid out on the board will affect circuit operation.

This Application Note explains how to use the 4193A Vector Impedance Meter (Fig. 1-1) to solve these problems, and to achieve reliable and efficient design of video electronic circuits, and circuits which operate in the VHF band. In explaining the circuit design application of the 4193A, many actual examples are used. These include measuring component impedance at the desired operating frequency, measuring the input/output impedance of an assembled circuit, and measuring the output impedance of a power supply. The information included in this Application Note should prove useful in designing and packaging circuits for VTR, TV and other communications equipment.

1.2 4193A Outline

The 4193A is a grounded probe-type vector impedance meter. Its measurement frequency is continuously vari-

Test Signal	Frequency: 400 kHz to 110.0 MHz. 4 digit resolution Sweep: Manual or Automatic, Full Sweep or Partial Sweep
Measurement Range Resolution and Accuracy	$\begin{aligned} & Z : 0.01\Omega \text{ to } 120.0 \text{ k}\Omega \\ &\text{Maximum resolution: } 10 \text{m}\Omega \text{ on } \\ &10.00\Omega \text{ range} \\ &\text{Best accuracy: } 3.0\% \\ &\theta: -180.0^{\bullet} \sim +180.0^{\circ} \\ &\text{Resolution: } 0.1^{\circ} \\ &\text{Best accuracy: } 3.2^{\circ} \end{aligned}$
Displays	 4 digit frequency display. 3½ digit impedance magnitude and phase displays.
Data Output/ Remote Control	HP-IB and recorder output of $ Z $ θ and frequency

Table 1-1. Key Specifications of 4193A

able from 0.4 to 110 MHz with 4-digit resolution. The instrument measures and digitally displays impedance magnitude |Z| from 10 milliohms to 100 kilohms with 3.5 digit resolution, and phase from 0° to ±180° with 0.1° resolution. In addition, the automatic sweep feature provides many convenient functions for measuring frequency characteristics and operability. The 4193A can accurately measure impedance characteristics of not only individual circuit components, but also of entire assembled circuits, and can be effectively used at every stage of electronic circuit design. Main specifications are listed in Table 1-1.

1.3 RF Circuit Design

When designing an electronic circuit, the main components must first be selected. Careful selection is important because the characteristics of components at rated frequencies may be quite different from those at actual operating frequencies. Parts which greatly affect circuit performance must be carefully evaluated before circuit assembly to ensure they will perform as desired. The impedance of lead wires and stray capacitance between components also affect circuit performance, requiring components to be evaluated at the actual operating frequency or frequency band, and with the lead wire cut to the lengths that will actually be used. After evaluating the individual components, the pattern in which the selected parts will be mounted on the printed circuit board must be evaluated. This becomes especially important for circuits operating at frequencies above 10 MHz, because the impedance in the pattern and capacitance between patterns greatly affect circuit characteristics. Correct evaluation can effectively prevent unexpected phase shifts, signal attenuation, and oscillations. After assembling the components in the determined pattern, the circuit must be connected to a DC power source and tested for overall performance. Various problems may be encountered at this stage: the amplifier doesn't provide sufficient gain, the gain is not flat enough, or, for a filter, the cut-off frequencies do not match. One of the most common causes of these problems is that stray admittances generated between the packaged parts of patterns result in actual impedance values quite different from the expected ones. To solve this problem, input and output impedances and other characteristics must be measured with the circuit assembled, and without changing bias conditions. Thus, when designing an electronic circuit for operation in the RF band, the three most important factors to be evaluated are the characteristics of components at the actual operating frequency, the impedance of lead wires and printed circuit board patterns, and the stray capacitance between mounted circuit components. The 4193A Vector Impedance Meter measures component characteristics, pattern impedance, and stray capacitance easily and efficiently, and contributes greatly to reliable design of video circuits and circuits operating in the VHF band.

2. MEASUREMENT OF DISCRETE COMPONENTS FOR HIGH FREQUENCY CIRCUITS

2. 1 General

The most frequently encountered problems in high frequency circuit design are insufficient gain (amplifiers) and incorrect cutoff frequency (filters), both of which are usually caused by differences between the impedances and admittances of the design-stage circuit and those of the assembled circuit. At the component level, there are two main causes:

- Impedance frequency characteristics of the components themselves.
- Impedance of and capacitance between lead wires of individual circuit components.

In terms of the assembled circuit, there are also two main causes:

- Impedance of the printed pattern.
- Stray admittances between components and between patterns.

Components used in high-frequency electronic circuits should be evaluated for individual characteristics before assembly, and for impedance after assembly. The following explains how to make this evaluation.

2. 2 Component Frequency Characteristics Measurement

A great deal of useful information can be obtained by measuring the impedance characteristics of circuit components at the frequency which they are to operate. Fig. 2.1 shows an example of using the 4193A to measure the impedance frequency characteristics of a ceramic capacitor. If the capacitor were ideal, the curve would go down at the right. Instead, it shows a V-shaped characteristic. This happens because the capacitor itself includes inductive and resistive components. If equivalent circuit elements do not greatly depend on frequency characteristics, the R, C, and L values given in Fig. 2.2 can easily be estimated from the measurement results shown in Fig. 2.1.



(b) Simplified Equivalent Circuit

The L and C reactances can be ignored in the area indicating resistance near the resonant frequency f_0 (approx. 5.8 MHz), where the phase is zero in Fig. 2.1. Since $1/G \gg R$, the capacitor can be regarded as a simple equivalent resistive circuit, whose equivalent series resistance (ESR) is 0.57 ohm,

$$R = 0.57 \text{ ohm}$$
 (2.1)

In the low-frequency capacitive area of Fig. 2.1, the L component can be ignored. Since parallel conductance Gis also negligibly small compared to ωC , the capacitor can be regarded as an equivalent RC series circuit. Therefore, the value of C can be calculated from the following equation.

$$C \simeq \frac{1}{\omega\sqrt{|Z|^2 - R^2}}$$
(2.2)

- ω : Angular frequency = $2\pi f$
- : Measurement frequency (Hz) = 0.4 MHz f
- |Z|: Impedance magnitude (ohm) displayed on the 4193A
- : Equivalent series resistance (ohm) R



Figure 2.1. **Frequency Characteristics of Ceramic** Capacitor



(c) Example of Equivalent Circuit with Actual Values

Equival ent Circuits of Ceramic Capacitor Figure 2.2.

The following equation can be used in the frequency range where $|Z| \gg R$.

$$C \simeq \frac{1}{\omega |Z|} = \frac{1}{2\pi \times 0.4 \times 10^6 \times 17.00} = 23.4 \text{ nF}$$
(2.3)

In the area of high-frequency inductance, the capacitive reactance can be ignored and an equivalent RL series circuit can be assumed. The value of L, then, is determined by the following equation.

$$L \simeq \frac{\sqrt{|Z|^2 - R^2}}{\omega}.$$
 (2.4)

The following equation can be used in the frequency range where $|Z| \gg R$, and f = 110 MHz.

$$L \simeq \frac{|Z|}{\omega} = \frac{17.85}{2 \times \pi \times 110 \times 10^6} = 25.8 \text{ nH}$$
 (2.5)

From the above explanation, the equivalent circuit given in Fig. 2.2 can be expressed as b) or c) if the results of equations 2.1 to 2.5 are used.

The measurement results given in Fig. 2.1 indicate that the capacitor works well at frequencies of about 5 MHz or below. The limitation of capacitor performance can be checked by calculating the equivalent circuit constants as described above, and then used as a basic value for selecting parts or design data.

This method of capacitor evaluation is also applicable to resistors and coils. Fig. 2.3 shows how to calculate each equivalent circuit constant.



Figure 2.3. Frequency Characteristics and Equivalent Circuit for Circuit Components

2. 3 4193A Test Fixture for Discrete Component Measurement

For reliable measurement of a circuit component in the video or VHF band, it is important to put the component in as close to actually assembled status as possible, and to use a suitable test fixture. The 4193A provides a variety of fixtures (Fig. 2.4) for measuring chip, radial lead, and axial lead components, and components of other shapes.



Figure 2.4. Test Fixtures for the 4193A

Fig. 2.4 (a) shows the 4193A attached to the 16099A Test Fixture Adapter, upon which is mounted a discrete component test fixture. Three types of component test fixtures are available, as shown in (b), (c) and (d) of Fig. 2.4. The numbers given in the figure indicate the distance between terminals, or the maximum measurable component dimensions. Because its measurement terminals are movable, the 16092A Test Fixture, shown in (b) of Fig. 2.4, can be used to measure components with lead wires as long as those to be actually used. Fig. 2.5 shows the results of two measurements made on the same ceramic capacitor. Lead wire length differs by about 1 cm for purposes of measurement. Since there are big differences in resonance frequencies and impedance values, the lead wires must be as long as will actually be used.

Fig. 2.6 shows a component mounting adapter which connects directly to the probe. Components are connected between the center terminal and either of the two outer terminals. Spacing between the center terminal and each outer terminal is 13.5 mm and 20 mm, respectively.

Fig. 2.7 shows a probe socket designed for board mounting and for user-fabricated test fixtures. Almost any type of fixture can be connected for measurement.



 $|Z_L|, \theta_L$: Long lead $|Z_s|, \theta_s$: Short lead









Figure 2.7. Probe Socket

2. 4 Compensation for Test Fixture Residuals

In some cases, the residual impedance in a test fixture causes error when measuring the impedance of a circuit component. If this effect can be compensated, a more accurate measurement can be obtained. Fig. 2.8 compares values of impedance characteristics with and without residual impedance compensation. Compensation for residual impedance raises the resonant frequency by about 8 MHz, and lowers the resonant impedance by about 0.5 ohm. Eliminating the error caused by the test fixture results in the correct value. The impedance range in which correct values can be obtained if residual impedance is compensated is shown in Fig. 2.9. (A sample program for automatic residual impedance compensation via the HP-IB is given in the Appendix (p. 19).



Figure 2.8. Residual Imposdance Compensation for Frequency Characteristics of Ceremic Capacitor



- □ : Range where the residual error is less than 10%
- Range where the residual error is 10% or more (must be compensated)

Whenever the residual error caused by the fixture is to be minimized, compensation is necessary.

Figure 2.9. Additional Error due to Residual Impedance when the 16092A is attached to the 16099A

• How to compensate for residual impedance

Measured impedance values displayed on the 4193A include the impedance of the DUT plus the residual impedance of the test fixture. See Fig. 2.10. To obtain the true impedance of the DUT, the following method can be used.

1. Short circuit terminals A and B, and note the values displayed on the 4193A as $|Z_s|$ and θ_s (R_0 and X_0 measurements). Shorting rings are furnished with the 16092A and 16093A/B for this purpose.

$$Z_s \simeq R_0 + jX_0 \quad (\text{Impedance of shorting} \\ \text{ring} \ll |R_0 + jX_0|) \quad (2.6)$$

2. Perform measurement with terminals A and B open, and note the values displayed on the 4193A as $|Z_0|$ and θ_0 (G₀ and B₀ measurements).

$$Z_0 \simeq \frac{1}{G_0 + jB_0} \quad (|G_0 + jB_0| \ll \frac{1}{|R_0 + jX_0|}) \quad (2.7)$$

- 3. Connect the component to be measured to terminals A and B, and note the values displayed on the 4193A as $|Z_m|$ and θ_m .
- 4. The actual impedance of the component is Z_X/θ_X , and is calculated as follows:

$$|Z_x| = \sqrt{R^2 + X^2}$$
 (2.8)

$$\theta_x = \tan^{-1} \frac{X}{R} \tag{2.9}$$

where

$$R = \frac{(|Z_0| \cos \theta_m - |Z_m| \cos \theta_0) \cdot |Z_m| \cdot |Z_0|}{(|Z_0| \cos \theta_m - |Z_m| \cos \theta_0)^2 + (|Z_0| \sin \theta_m)} - |Z_m| \sin \theta_0)^2 - |Z_s| \cos \theta_s$$
(2.10)

$$X = \frac{(|Z_0| \sin \theta_m - |Z_m| \sin \theta_0) \cdot |Z_m| \cdot |Z_0|}{(|Z_0| \cos \theta_m - |Z_m| \cos \theta_0)^2 + (|Z_0| \sin \theta_m)} - |Z_m| \sin \theta_0)^2 - |Z_s| \sin \theta_s$$
(2.11)



Figure 2.10. Equivalent Circuit of Test Fixture

3. IN-CIRCUIT IMPEDANCE MEASUREMENT

In addition to measuring discrete components, as explained in Section 2, it is also important to measure the impedance of the assembled circuit if it is to operate at high frequencies. The following explains how to use the 4193A for this kind of evaluation.

3. 1 Input/Output Impedance Measurement

A high-frequency circuit often exhibits characteristics that differ significantly from theoretical ones because of board pattern impedances, and because of stray capacitances between mounted components. This results in, for example, insufficient amplifier output or incorrect filter cutoff frequency. One of the causes is that the actual input and output impedance values are different from the theoretical ones. By measuring the input and output impedances, the following factors can be correctly evaluated:

- Amplifier or mixer impedance matching.
- Tuning amplifier frequency characteristics.

Two examples of how to solve the above problems are given below.

(1) Impedance Matching

Fig. 3.1 shows a hypothetical video amplifier circuit. Point (A) is designed to match at 50 ohms. The filter used in amplifier 2 eliminates noise in the 300 MHz region, and is designed so that the characteristic impedance becomes 50 ohms. With the 4193A, impedance matching was checked at 50 ohms in the frequency range of 1 to 100 MHz. The results shown in Fig. 3.2 were obtained.



Figure 3.2. Impedance Matching between Amplifiers 1 and 2



The two circuits were found to match at frequencies up to 10 MHz. However, the output and input impedances were 53 and 40 ohms at 20 MHz, and 61 and 18 ohms at 50 MHz, respectively. That is, they were found not to match at high frequencies. This disparity results because the distributed capacitance of inductor L1 becomes larger as the frequency increases, and because the characteristic impedance value changes. In this circuit, the frequency range is from 1 to 100 MHz, and the input impedance of amplifier 2 must be between 25 and 75 ohms to obtain the initial output level of amplifier 2. To satisfy this condition, the value of the input filter capacitor of amplifier 2 must be changed, while measuring the input impedance with the 4193A, until the optimum value is obtained. The value of 20 pF was found to be best for the 47 pF capacitor (Fig. 3.3). Since the filter cutoff frequency is 205 MHz at that value, noise in the 300 MHz area from amplifier 1 can be sufficiently suppressed.

In a circuit which requires matching between stages, the 4193A can be used to measure the impedance, evaluate the results, and if mismatching occurs, to get rid of the cause.



Figure 3.4. Output Impedance-Frequency Characteristics of a Tuned Amplifier



Figure 3.5. Tuned Amplifier Circuit

(2) Tuned Amplifier

In a tuned amplifier, because output impedance is generally proportional to gain, by measuring output impedance, characteristics such as resonant frequency and bandpass can be evaluated. Fig. 3.4 shows the results of using the 4193A to measure output impedance in order to find frequency characteristics of the tuned amplifier shown in Fig. 3.5. This amplifier should theoretically resonate at 5.2 MHz, but actually resonates at 6.08 MHz. The measured resonant frequency differs from the expected one because of pattern inductance and stray capacitance between patterns and components. From the measurement results shown in Fig. 3.4, the pass band and resonant frequency can be calculated as follows.

- Pass Band Frequency range between the -3 dB points on the curve: 5.99 MHz to 6.18 MHz
- Resonant frequency . Frequency at which output voltage and current are in phase: 6.08 MHz

When the tank circuit is mounted, the circuit Q can be calculated from bandwidth ΔF and resonant frequency f_0 using the following equation.

$$Q = \frac{f_0}{\Delta F} = \frac{6.08}{6.18 - 5.99} = 32.0 \tag{3.1}$$

When $L = 4.7 \mu H$ and C = 200 pF, the characteristics are as shown in Fig. 3.4. To change the resonant frequency to the desired value of 5.2 MHz, the following measures can be taken.

By setting the 4193A measurement frequency to 5.2 MHzand continually changing the value of the tuning capacitor, the phase display can be checked. When the phase is 0 degrees, 254 pF is the capacitor value to be used. Fig. 3.6 shows the output impedance characteristics at that time.



Figure 3.6. Output Impedance – Frequency Characteristics of the Improved Tuned Amplifier

3.2 Oscillator Circuit Design and Evaluation

Oscillator circuits, such as crystal oscillators, often do not work as designed. One of the causes is that the negative impedance of the circuit could not be measured accurately after circuit assembly. The 4193A can be used to calculate stable oscillation conditions from the negative impedance measurement and to determine the optimum value of the load impedance. As an example, the following describes how to do so for the 100 MHz crystal oscillator shown in Fig. 3.7.

The 100 MHz crystal oscillator circuit in the figure can be represented by the equivalent circuit shown in Fig. 3.8.

Condition for oscillation:

$$-\frac{1}{r} + \frac{1}{R_L} \le 0 \ (r \le R_L) \tag{3.2}$$

Condition for no oscillation:

$$-\frac{1}{r} + \frac{1}{R_L} > 0 \ (r > R_L) \tag{3.3}$$

When the condition given in equation 3.2 is satisfied, oscillation starts. When the condition given in equation 3.3 is satisfied, oscillation does not occur.



Figure 3.8. Equivalent Circuit and Oscillation Condition of Negative Resistance Oscillator

By disconnecting point A in Fig. 3.8 and measuring the negative impedance and the load impedance with the 4193A, it can be checked whether the oscillation condition and design margin are satisfied. If the oscillation condition is not satisfied, constants -r or R_L can be changed to stabilize oscillation.

Refer again to the circuit diagram given in Fig. 3.7. Circuits R1 and U1 on the load side can be removed to check the oscillation condition and to measure the negative output impedance at point. The result is shown in Fig. 3.9. Oscillations may occur at points $\mathfrak{B}(100 \text{ MHz})$ and $\mathfrak{O}(100.04 \text{ MHz})$ where the phase is -180° . Since the negative resistance $(-r_1)$ at point \mathfrak{B} is 320 ohms and $(-r_2)$ at point \mathfrak{B} is 820 ohms, the following two conditions must be satisfied to cause oscillation at 100 MHzat point \mathfrak{B} , and not at 100.04 MHz at point \mathfrak{C} . From the oscillation condition of equation 3.2,

$$320 \text{ ohms} \leq R_L \ (r_1 \leq R_L) \tag{3.4}$$

and from equation 3.3,

$$820 \text{ ohms} > R_L \ (r_2 > R_L) \tag{3.5}$$



Figure 3.9. Negative Impedance Characteristics of Crystal Oscillator

Thus, a load impedance, R_L , which satisfies both conditions, must be used. The optimum value is about 600 ohms, which is between 320 and 820 ohms, taking into account design margins such as the diverse impedances of the crystal resonator and circuit components, and ambient temperature.

Value R1 can then be determined from value R_L (600 ohms). The impedance on the load side from point A is about 16 times R1 (connected by transfonner T1; turns ratio 4:1) because the U1 input resistance can be ignored. Therefore, R1 is 37.5 ohms (= 600 ohms/16). If R1 is a discrete resistor with a standard value, 38.3 ohms, R_L is 612.8 ohms (38.3 ohms × 16) and fully satisfies the stability conditions at point A (equations 3.4 and 3.5).

Finally, R1 and U1, whose values are now known, can be installed, the negative impedance can be removed, and the impedance on the load side can be measured using the 4193A. The result is converted to the resistance shown in Fig. 3.10. The figure indicates that value R_L is around 600 ohms, and that stable oscillation can be obtained.

The 4193A can easily measure the usually hard-to-determine impedance characteristics of an assembled oscillator circuit such as this, or at least to determine circuit constants for securing stable oscillation, for preventing abnormal oscillations, and for designing highly reliable oscillator circuits. Figures 3.9 and 3.10 show measurements made with an external synthesizer connected and the frequency resolution raised. For details, refer to the apppendix (p. 18).



3.3 Power Source and Ground Pattern Impedance

In a hybrid circuit with both analog and digital sections, noise in the digital section may have adverse effects on the analog section when transmitted through the power source or ground line. In this case, the impedances of the power source and ground patterns can be used to prevent noise from getting through. To eliminate interference between circuits, power source line evaluation using the 4193A is especially important. In actual applications, the AC impedance should be large enough to attenuate noise on a line if the line lets noise pass easily, or absorbs noise because of the decoupling capacitor. The 4193A is useful for designing a pattern which does not transmit noise. This is done by measuring pattern impedances of the power source and ground systems over a frequency range of 0.4 to 110 MHz by simple probing.



(1) Printed pattern connection between points (8) and (2)

- Zt : Impedance of frequency divider at the power supply point
- Z_2 : Output impedance of 5V supply
- Z₃: Printed pattern impedance between 5V supply and frequency divider



(2) Filter circuit inserted between points (A) and (C)

Z₄: Printed pattern impedance between 5V supply and power supply point of amplifier

Z₅: Impedance of amplifier at the power supply input

Figure 3.11. DC Power Supply Configuration for Mixed Analog and Digital Circuit

Fig. 3.11 shows frequency divider (digital) and amplifier (analog) circuits mounted on a printed circuit board. They are both powered from the same +5V power source. Z_1 contains decoupling capacitor C6, and Z_5 contains decoupling capacitor C7. The impedance value is large at high frequencies, and switching noise generated at Z_1 goes to point (B) through the +5V power source pattern, and appears in the amplifier output as spurious noise. To check how much noise gets through, the switching frequency of the divider circuit, pattern impedances Z_3 and Z_4 between points (A) and (C), and between points (B) and ©, respectively, at the second harmonic, and ground impedances Z_1 , Z_2 , and Z_3 at points (A), (B), and (C), respectively, were measured with the 4193A. The results are listed in Table 3.1 (1). Using equation 3.6 to determine the noise transfer ratio, gave results of 16% to 70%.

$$B(t) = \frac{Z_2 \cdot Z_5 \cdot A(t)}{Z_3 (Z_2 + Z_4 + Z_5) + Z_2 (Z_4 + Z_5)} \quad (3.6)$$

$$A(t) : \text{ Noise generated at } Z_3$$

A (t) : Noise generated at Z_1 B (t) : Noise transferred to Z_5

If the AC impedance of Z_3 is increased, noise can be attenuated. By inserting an inductor in series with the Z_3 pattern, and a bypass capacitor between the grounds (see Fig. 3.11), the resultant values become as listed in Table 3-1 (2). The noise transfer ratio improves to about 1% or less, spurious noise at the amplifier output decreases at the same ratio, and high-quality signals are thereby obtained.

Since the 4193A measures pattern impedances and quantitatively evaluates noise, it is a valuable tool for achieving more logical and efficient circuit design.

Noise level at Point (B) Frequency Z2:0 23:04 2,0 Zsin Noise level at point (A) (1) 50 1.5 2 9 - 3.08dB 7.5MHz (2) 450 2 9 - 35.9dB 50 (1) 2.5 1.5 - 13.1 dB 65 2.6 10MH2 (2) 600 2.6 1.5 - 52.6dB 65 3.7 1.5 (1) 120 4 - 15.9dB 15MH2 3.7 1.5 - 56.6dB (2)120 970 $(\mathbf{1})$ 235 5.6 4.8 2.5 - 14.3dB 20MHz - 55.4dB (2) 235 1420 2,5 4.8

Table 3-1. Impedance Evaluation of DC Power Supplys

3.4 Pattern Inductor Design and Evaluation

Circuits often do not operate as designed at high frequencies because of pattern impedances. However, this need not always be a problem. Pattern impedances can sometimes be utilized for more effective circuit design because of three factors:

- They have high resonant frequencies, are stable as inductive elements, and are not frequency dependent.
- Not all desired inductor values can be created by coils.
- They are cheap and do not take up much board space.

The following explains how the 4193A is used to measure the pattern inductance of an LC filter.

In the low-pass filter for input to the video amplifier shown in Fig. 3.12, pattern type series inductor L1 (Fig. 3.13) was chosen in order to match the previous stage at 50-ohm impedance. This match is necessary because the filter's cut-off frequency is over 100MHz and cannot be increased any further. The designed value is 60nH, but lead inductance, distributed capacitance, pattern inductance, and other factors make it difficult to obtain the exact value when initially assembling the circuit. Here, the 4193A can be used to solve the problem. By making a trial pattern inductor value larger than the designed value, the initial impedance value can be found by shifting the 4193A probe tip (Fig. 3.14).



Figure 3.12. Low-pass Filter Circuit Used in Video Amplifier



Figure 3.13. Printed Pattern Inductor

Figure 3.14. Pattern Impedance Measurement Using Test Probe of the 4193A

Conversely, by making the pattern area gradually smaller, the impedance can be measured step by step. In the 4193A, parameter conversion can be easily done by a controller via the HP-1B. The optimum value can be obtained by monitoring the inductance value directly. When designing a pattern with high inductance ($\geq 1\mu H$), the stray capacitance of the probe may affect measurement. The correct value can be obtained by compensating for the residual impedance (see paragraph 3.5 and appendix A (p. 15)). Fig. 3.15 shows the measured values of the trial pattern inductor created by using the parameter conversion program given in the appendix (p. 19) and gradually changing the measurement point. The point at which the measured value is almost the same as the designed value, 60nH, is found in the frequency range of 1 to 100 MHz. The 4193A proves very useful for measuring pattern inductance of a high-frequency electronic circuit like this or any other hybrid IC because of its high resolution (10 milliohms), wide measurement range, and easy-to-use probe.



Figure 3.15. Helical Pattern Inductence Evaluation at Different Points on Pattern

3.5 Measuring Assembled Circuit Impedance

There are several points to note when measuring assembled circuit impedance, especially active circuits which must have high reliability. The four most important points for making measurements with the 4193A are as follows:

(1) Circuit Measurement Fixture and Residual Impedance Compensation

In addition to the component measurement test fixtures explained in Section 2.3, there are also circuit measurement test fixtures for the 4193A. Fig. 3.16 (a) shows a ground adapter which measures by directly probing circuit, and Fig. 3.16 (b) shows a ground lead used when there is no ground point near the measurement point. When the circuit measurement terminal is a BNC connector, the BNC adapter shown in Fig. 3.17 is used. The BNC adapter ground can be used as an N-type ground if removed. Residual impedances can be compensated for these fixtures in the same way as for discrete component test fixtures described in Section 2.4.



Figure 3.16. Ground Adapter (a) and Ground Lead (b)



Figure 3,17. BNC Adapter

(2) Probe Withstand Voltege

When the probe is used to measure impedances in an active circuit the bias voltage of the circuit may have an adverse affect. The 4193A probe can handle up to 50V DC, and can measure almost any circuit without being damaged. However, this limit may be exceeded when measuring a circuit driven by high voltage or a high output electronic amplifier. In this case, correct measurement can be obtained without damaging the probe by using a blocking capacitor (refer to the appendix for the measurement method). Note that the AC withstand voltage of the probe is 5 Vnns.

(3) Measurement Signal Level

The 4193A measurement signal level changes according to the impedance measurement range, as listed in Table 3-2. If the range is fixed, the current level does not change regardless of the impedance measured. Therefore, a voltage equal to the product of displayed impedance value and measurement current is applied to the component being measured, and reaches its peak when the impedance value is highest.

Impedance range	10Ω	100 N	1kΩ	10kΩ	100 k Ω
Measurement current	100 <i>⊭</i> A	1 00 " A	100 <i>⊭</i> A	50 <i>⊭</i> A	10#A
Maximum signal level	2mV	20mV	200mV	1۷	1.2V

Table 3-2. Relation between Measurement Signal Level and Impedance Range

If measured impedance value overrange (Or) is displayed, the voltage applied to the component exceeds the value in the table. This may reach 100 to 230mVrms on 10Ω to $1k\Omega$ ranges, and 1 to 1.2Vrms on other ranges. Therefore, care must be taken when measuring voltage sensitive components. When measuring an assembled circuit, the measurement signal level must be carefully considered, especially for circuits that contain an amplifier. If the circuit saturates, or if the active point of an active element is changed drastically, the impedance may be measured under circuit conditions different from actual operating conditions. To guard against this, use an oscilloscope, and check the measurement points of the circuit before actual measurement to make sure that there is no distortion in the waveforms.

(4) Effects of Operation Signals on Circuit Measurement When measuring circuit impedance with the 4193A, ideally, the circuit should be free from operating signals or noise. However, this is impossible for some circuits. For circuits with AC signals (e.g., active circuits such as synthesizers or signal generators), the measured value may become unstable. To obtain stable results with the 4193A despite the AC signals or noise, the following two points should be considered.

- 1. Difference between frequency of operating signal in the circuit and the 4193A measurement frequency.
- 2. Level of operating signal going through the circuit.

1. Frequency condition

If the operating frequency of the circuit to be measured is too close to the 4193A measurement frequency, measured values fluctuate and the correct value cannot be obtained. Therefore, it is necessary to set a difference between them. This difference, called ΔF , changes according to the signal level of the circuit to be measured. Fig. 3.18 gives reference data indicating the relationships between signal level and ΔF . Note how much difference must be set between their frequencies when the signal level does not change. This is near the fundamental wave of the 4193A measurement signal, but also applies to harmonics. Therefore, the following harmonics and signal frequency of the circuit to be measured must have at least the ΔF shown in Fig. 3.18.

$$F = n \times K$$
 (n = 1, 2, ...) (3.7)
 $F:$ 4193A harmonics
 $K:$ See Fig. 3.19



(ΔF : Frequency difference between test frequency of the 4193A and operating signal frequency of circuit under test)

Figure 3.18. Relation between Minimum Frequency Difference (△F) and Operating Signal Level of Circuit under Test



2. Level of operating signal passing through circuit

The second point necessary for stable measurement is the level of the signal passing through the circuit. The maximum allowable signal level in the circuit loosely depends on the impedance of the component to be measured, as shown in Fig. 3.20. For example, if the impedance is 10 ohm, the level of the signal passing through the circuit must be lower than -10 dBm. If higher, measurement values may fluctuate.

Check whether the following example satisfies the above condition (indicated by dashed lines in Fig. 3.18 to 3.20).

Measurement conditions:

Operating frequency	 10MHz (assume there
	are no harmonics)
Operation signal level	 -30 dBm
Impedance	 10 ohms

If the measurement is made at a frequency as close to the operating frequency as possible, ΔF is 30 to 35 kHz as calculated from Fig. 3.18. Then, suppose that the 4193A measurement frequency is set to 10.04MHz. Here, 8.3748 and 10.0498 MHz are found to be the 4193A harmonics closest to 10MHz from equation 3.7 and Fig. 3.19. These values satisfy the ΔF condition because they are more than 35 kHz away from the operating frequency, 10 MHz, of the component to be measured. Also, since the 10-ohm impedance is in the stable area of Fig. 3.20 when the operation signal is -30 dBm, stable measurement is possible at 10.04 MHz. Note that measurement is always stable if the level of a signal passing through a circuit is -80 dB or lower than the 4193A measurement signal.



Figure 3.20. Relation between Operating Signal Level and Impedance Value of Circuit under Test

APPENDIXES

A. HP-IB System Applications

By connecting the 4193A to a controller via the HP-IB, measurement and data processing can be done automatically. The following describes a measurement example in which the residual impedance of a test fixture is compensated by a simple system structure as shown in Fig. A-1. Parameter conversion is also done. Residual impedance compensation was already explained in Section 2.4. Parameter conversion can be calculated from the 4193A measurement data (|Z| and θ) given in Table A-1. Fig. A-2 (p. 16) is a flowchart for compensation and conversion using the 9845B desk-top computer, and shows six cases of representative automatic parameter conversion. The results are given in Fig. A-3. This program is very efficient because parameter conversion can be done without having to compensate for residual impedance. For a device or test fixture which does not require such compensation, parameter conversion can be done immediately.

Parameters	Circuits	Symbols	Conversion equations
Series resistance		Rs	Z · cos∅
Series reactance	*• i•	X	Z · sinθ
Conductance		G	cos0/ Z
Susceptance		В	-sin0/121
Series inductance		Ls	Z ·sinθ/(2πf)
Series capacitance	0	C _S	—1/(2πf+ Z +sinθ)
Parallel inductance	<u>مر "ب</u> ه	Ĺp	Z /(2#f·sin0)
Parallel capacitance		Ср	—sinθ/(2πf· Z)
Quality factor	×,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	Q	tan <i>θ</i>
Dissipation factor		D	tanð− /tanθ
Admittance		Y , Ø _Y	$ Y =1/ Z , \ \theta_{Y}=-\theta$

Table A-1. Table of Parameter Conversion



Figure A-3. Effect of Residual Compensation

f : Test frequency

|Z|: Impedance magnitude readings

 θ : Phase readings





OPT. 311(98411A) GRAPHICS ROM OPT. 312(98412A) I/O ROM

Line number



Figure A-2. Flow Chart for Residual Impedance Compensation and Parameter Conversion Program

B. Measuring Impedance of Components Biased at Over 50V DC

The 4193A probe can safely handle up to 50V DC or 5Vrms AC. Use the following methods for values over 50V DC to prevent damage to the probe.

(1) Circuit Measurement

If a circuit has a bias voltage of over 50V, insert a blocking capacitor (C_B) between the probe and circuit before measurement (Fig. B-1). The impedance $[1/(2\pi f C_B)]$ of capacitor C_B must be negligible at the measurement frequency in order to compare it with that of the circuit to be measured. Note that a 4193A measurement value includes C_B if the value is not small enough. When this occurs, apply the same voltage to be applied to the circuit to C_B , and check that it does not fail. Then measure with the 4193A to obtain the value of vector impedance Z_{CB} . After that, measure circuit impedance Z_m through capacitor C_B and compute $Z_m - Z_{CB}$ to obtain the value of component impedance Z_C .

(2) Component Measurement

When measuring a component with a voltage over 50V, use the bias circuit shown in Fig. B-2. Here, the impedance of capacitor C_B must be negligible as described in (1). If the C_B impedance is too large, compensate in the same way as described in (1). Conversely, the impedance, $\sqrt{R^2 + \omega^2 L^2}$, of the bias circuit must be sufficiently large in comparison with that of the component, because the two are in parallel.



when the impedance of blocking capacitor is negligible compared to that of circuit under test:

 $(|Z_{CB}| \ll |Z_C|)$

 $Z_C \simeq Z_m$

when the impedance of blocking capacitor is not negligible:

$$Z_C = Z_m - Z_{CB}$$

Figure B-1. Measurement of Active Circuits Biased at Over 50V DC



Condition that the measured value is equal to the impedance value of DUT is as follows:

$$|Z_{CB}| \ll |Z_x|$$
$$\sqrt{R^2 + (2\pi fL)^2} \gg |Z_x|$$

Figure B-2. Measurement of Components Biased at Dver 50 V D C

C. How to Increase Test Frequency Resolution (External Synthesizer Application)

The 4193A frequency resolution is 4 digits, but must be improved when measuring high Q devices, such as crystals. The frequency resolution can be improved by connecting an external synthesizer to the 4193A as shown in Fig. C-1. The external synthesizer affects only the frequency resolution. The measurement signal level and other characteristics are all determined by the 4193A. It is best to make the synthesizer frequency as close to that of the 4193A as possible, but, for the absolute impedance value |Z|, a difference of 10 MHz or less is small enough for accurate measurement. The phase should be compensated using the following equation.

- $\theta_r = \theta_m + 0.72 \ (f_0 f_1)$
 - f_0 : 4193A set frequency in MHz
 - f_1 : External synthesizer set frequency in MHz
 - θ_m : 4193A display value
 - θ_r : Compensated real phase value

The limit of frequency resolution provided by an external synthesizer depends on the residual FM in the 4193A internal synthesizer (Fig. C-2).

Notes

If a synthesizer capable of generating a frequency of 110 MHz or over is connected, the 4193A may be able to measure up to 140 MHz. Also, if a synthesizer with higher frequency resolution than residual FM in the 4193A internal synthesizer us used, measurement is possible with lower frequency resolution than residual FM. In this case, however, accuracy of the measured value cannot be guaranteed.







1310 BEEP 1320 INPUT "Topon PARAMETER CONDINATION NUMBER.", \$ 1330 GCLEAR 1340 FINED 3 1350 IF BAL THEN FRENT "STEP No.", "FPEQUENCY "MHZ"", "RESISTANCE COND.". "REACTAN CE KOHMUM 1360 IF B#2 THEN PRINT "STEP NG.". "FPEQUENCY HIND/STEPDUCTANCE (MS)". "SUSCEPT ANCE LASS! 1370 IF B=@ THEN PRINT "STEP NO.", "FREQUENCY (11HZ)", "INDUCTANCE (UH)", "PUALITY FR. TOR" 1380 IF B=4 THEN PRINT "STEP No.", "FREQUENCY (MHz.", "CAPACITANCE (pF)", "DISS. PA TION" 1390 IF B=5 THEN PRINT "STEP No.", "FPEQUENCY (MHZ)", "INDUCTANCE (VH)", "RESISTAN CECOND. 1400 IF BEG THEN PRINT "STEP Ho.". "FPEQUENCY (MHZ)". "CAPACITANCE (OF)". "CONBUCT ANCE CHS?" 1410 IF \$=7" THEN PPINT "STEP HA. "."FREQUENCY (MMESH", "MAGNITUDE (UMH)", "PHASE (D EGREE / " 1420 FOR 1=1 TO N 1430 IF B=1 THEN AKI/=CF1 (#COSCDKT/) 1448 IF B=2 THEN A(L/=COS(D(L))/C+L/+1000 1450 IF BES THEN ALDECCIDESING DILODY2/PL F(I)+1E6 1460 | IF B=4 THEN ACI)=-1E12/2/F1/C(I)/\$14(D(I))/F(1) 1470 IF B=5 THEN A(1)=((1)+SIN(D(1))/2/PE/F(1++E6) 1480 IF B=6 THEN A(1)=-LEL2/2/P1/C(1)/SEN(D(1))/F(1) 1490 IF B=7 THEN AKID=CUD 1500 IF B=L THEN B(L+=C(D+SLH(D(L++ 1510 IF B=2 THEME B(1)=-SIN(D(1))/0(1)*1000 1520 [F (B=3) AND (COS(D(1))=0) THEN B(L)=ABS(S[H(D(1)))/[E-3) 1530 LF (\$=3) AND (COS(D(1))=0) THEN 1590 1540 IF B=3 THEN B(I)=ABS(SIN(D(I)))/ABS(COS(D(1))) 1550 IF B=4 THEN B(I)=TAH(ABS(40-ABS(D(I)))) 1560 IF B=5 THEN B(1)=((1)+COS(D(1)) 1570 IF B=6 THEN B(L)=COS(D(1+)) C(L)*1000 1500 IF B=7 THEN B(1)=D(1) 1590 LE TIMAKIS THEN TIRACIS 1600 [F T2>A(L> THEN T2=A(L) 1610 IF SEXELD THEN STUB. [] 1620 1F \$2)B(E) THEN \$2=B(E) 1630 PPINT L, F(I)-1EEGANID, B(1) 1640 NEXT E 1650 PRINT "------" 1660 FRINT "MAXIMUN=",, "A=";T1, "B=";SL 1670 PRINT "HINEMUM="...TA+";T2,"#=":\$2 1680 BEEP THEVE "Input MARINUM and MINIMUM value of A for graphic scaling", (1, k2 1690 [:00 HIPUT "Input MARINUM and MINIMUM walke of B for graphic scaling", L1,L2 1710 STANDARD 1720 RETURN 1738 Polar: 1 ************** POLAR ************** 1740 SCALE K2-+K1-K2++.2.K1+(K[-K2)+.2.L2-/L1-L2++.2.L1+(L1-L2)*.2 1750 CLIF #2,81,12,11 1260 FRAME 1770 IF (11(0) AND (11(0) THEN 1870 1790 LE HELLON AND HELLON OR HELLON THEN GERON 1790 IF (110) AND (1114 OR 11=0/ AND (12:0) THEN 2530 1860 1F - (K2:0) OR (12=0) AND (L1-0) THEN 3040 1810 IF -- K2'0 OR (12=0)) AND (112:00 DR -12=0++ THEN 3370) 1220 IF .(Y2:0) OR (Y2=0)) AND ((LI:0) OF (LI=0)) AND (L2:0) THEN 3700 1830 IF ((11 0) OR (11=0)) AND (1210) AND (1210) OP (12=0) TISEN 4100 1840 IF 2011 02 00 (KL=0)) AND (K2-0) AND (L1(0) THEN 4490 1950 [F ())[30) OP (K1=0) AND (K230) AND ((L110) #R (L1=0)) AND (L230) THEN 43 4. 1870 AXES (#1-#2/10, LI-L2)/10,K2,L2 1880 100VE (*1+K2)/2, L2-(L1-L2)*.2 1890 CSI2E 4..5 1900 DEG 1910 LOFG 4 1920 GOSUE Name

1930 FOP 1=0 TO 10 STEP 2 1940 HOVE 12+1+(11-K2)/10.L2-(L1-L2++.0) 1950 CSIZE 4,.5 1960 LORG 6 1970 IF \$2(-499 THEN 2000 1980 LABEL #2+1+(k1-12)/10 1998 GOTO 2018 2000 LABEL (K2+1*+K1+K2+/10*/1000 2010 NEXT E 2020 MOVE K2-(11-K2)+.2. 11+12 1/2 2030 CSIZE 4..5 2040 LDIR 90 2050 DEG 2060 LORG 6 2070 GOSUB Haming 2080 LD1P . 2090 FOR 1=0 TO 10 STEP 2 2100 MOVE K2-(+ E-K2)*.01,L2+E*(L1-L2)/10 2110 CSLZE 4..5 2120 LORG 8 2130 IF L24-499 THEN 2160 2140 LABEL L2+I+(L1-L2). 10 2150 6010 2170 2160 LABEL (L2+[+(L1-L2) 10)-1000 2170 HEXT L 2180 6010 5350 2200 AXES (1(1-k2)/10.(L1-L2)/10.k2,L2 2210 MOVE (K1+F2+2,L2-+L1-L2++.2 2220 CSIZE 4..5 2230 DEG 2240 LORG 4 2250 GOSUB Name 2266 FOR 1=0 TO 10 STEP 2 2276 NOVE K2+1+(k1-K2), 10, L2-+L1-L2+-.01 2280 CSIZE 4...5 20961 2065 6 2300 IF K24-499 THEN 2330 2310 LABEL 12+1+(11-12).10 2320 COTO 2340 2330 LABEL (k2+3**F1-k2**[0/+1000 2340 NEXT 1 2050 MOVE K2-(+1-K2)+.2.(L1+L2) 2 2960 CSICE 4...5 2370 LDIR 90 2330 DEG 2398 LORG 6 2400 GOSUB Naming 2410 LDIR: 0 2420 FOR L=0 TO 10 STEP 2 2430 MOVE 12-(k1-k2)+.01,L2+1+(L1-L2) 60 2440 (SIZE 4...5 2450 LORG 8 2460 IF L2 499 THEN 141 2470 LABEL L2+1+(L1-L2)/14 2480 GOTE 2500 2496 LABEL (L2+[*(L1-L2)/10//1000 2544 NEXT L 2510 GOTO 5350 2530 AXES (#1-K2)/10, (L1-L2)/10, #1.0 2540 MOVE #2+++(1-#2)*.01,(L2-L1)/20 2550 CSI2E 4..5 2560 BEG 2570 LORG 3 2588 GOSUB Hame 2590 FOR 1=0 TO 10 SITEP 2 2600 HOVE \$2+1+(K1-h2,-10, L2-L1 +. 01 2610 CSIZE 4..5

2620 LORG 6

2630 IF K24-499 THEN 2660

1300 FRENT "12 -PHASE"." 2"

G030B Name G030B Name Move k2+1++k1-k2>+10,L2+(L2++,0) €512E 4..5 L046 00505 Nawe Now 140 No 10 STEP 2 Now 140 No 10 STEP 2 Nove 140 No 10 STEP 2 CSIZE 4.5 CSIZE 4.5 F K1 450 THEN 3840 I F K1 450 THEN 3840 LABEL K241+K1-K2.10 LABEL K241+K1-K2.1000 HEXT 1 NOVE K2.41-K2)+L2.1000 HEXT 1 NOVE K2.41-K2)+L2.2 C11+L2.2 C51ZE 4.5 C51ZE IF (L2(-499) 0F (L] 499 THEN 4000 LABEL I → LI-L2' 10 LABEL 1**11-L2* 10 1000 NEXT 1 NEXT 1 FOP L=0 TO L2*10 (L1-L2* 5TEF -2 MOVE k2-*K1-K2**.01.[**L1-L2*10 NOVE k2-*499 THEN 4070 LABEL 1**L1-L2*10 T. 1. 1499 THEN 3510 LABEL 12213+14/K1+22+10 G0T0 3520 LABEL (V2+14/K1+22+10) HEXT 1 HEXT 1 MOVE K2-1YI-K21+,2,1L1+L27 2 CSITE 4,5 LDIP 90 LABEL (12)+1>+L1-L2+ 10)+1000 LABEL (12)+1>+L1-L2+ 10)+1000 MEXT 1 Gold 5350 HF L11499 THEN 3670 ABEL L2+1+1L1-L2>10 Q U I ME H NENT | Coto 5350 GOTO 4018 6010 3630 4 9 101 6 D.10-LORC 8 LORG 4 LOFICE DEC

IF (kl.490 0K df2 - 493) THEH 4230
IF (kl.490 0K df2 - 493) THEH 4230
Coto 4240
Coto 4200
Coto 449
Coto 4300
Coto 449
Coto 4400
Coto 440 TE (Y2-499, M (K1 499) THEN 4638 LABEL 1*M 10 LABEL 1*M 10 LABEL 1*Y 10-1000 LABEL 1*Y 10-1000 MEXT 1 MEXT GOSUB NAME GOSUB NAME FOP 1=0 TO K1+10 (11-K2) STEF 2 MOVE 1+(1-K2) 10,L2-(L1-L2)+.05 K51E 4..5 L0FG 4 GBT0 4710 LABEL 1+K2*10000 NEXT 1 MOVE - 85+16+1-123,L2+6LL-L2+0,1 CSLEE 4,5 LDIR 90 G09418 Name G09418 Name F00 1=0 T0 K1+40×+1-K2> STEP 2 MOVE 1+411-K2>+10,L2-441-L2>+.01 C5125 4.55 L0RG € MOVE - 12-17---02,1241-41-424-19 0512E -44.5 LOFS \$ [F L] 429 TMEN 4460 [F L] 429 TMEN 4460 [F L] 429 TMEN 4460 [F L] 479 [F L] 419 [F L] 410 [F L] 1 [F L] 410 [F L] 1 G010 4020 Label 1+<L1-L2+ 10000 Next 1 GOSUB Haminq LDIF 0 FOF I+0 T(110 STEP 2 6010 5350 LORG 4 LOF6 7 4 LORG J LOPG ر. ليو DEC

------ e---- 1013 LDIR 0 FOR 1=0 TO 10 STEP 2 MOVE .03*(K2-k1',L2*1*.L1-L2')10 CSI2E 4,.5 LORG 8 Ŷ LOPG 7 COSUB Name COSUB Name FOR 1=0 TO K1+10.4K1-42° STEF 2 NOVE 1+4K1-42+10,4L1-422+03 CSI2E 4.5 LOPG 4 4 FOR 1=0 TO K2*10, K1-K2) STEF -2 MOVE 1=4 TO K2*10, K1-K2) STEF -2 MOVE 1*K1-K2>10, K1-L2)*.03 F *2(-499 THEN 5.00 LABEL 1*K1-K2>10 COTO ST10 LABEL 1*K1-F2> 10000 NEXT I Move .05+(K1-K2).L1-(L1-L2)+.01 C512E 4..5 LD18 90 4 FOR I=0 TO LI*10/(LI-L2/ STEP MOVE .03/(K2-K1),I*(LI-L2)/10 CSIZE 4,.5 LABEL (L2+1*(L1-L2)×10)) 1000 NEXT 1 5010 5350]F L2(-499 THEH 4860 LABEL L2+!*(L1-L2)/10 GOTO 4870 LABEL I*(L1-L2+/10000 HEXT I IF K12499 THEN 5030 Label Ifkk1-k2240 MOVE R(1, B(1) For I=1 TO N Urmu R(1, S(I) Hext I GOSUB Naming LDIP 0 GOSUB Naming LORG 7 LORG 8 RE TURN Name: -47764788

BLEF HHUT "LOG PLOT OR LINEAP FLOT FOR FFEDUENCY, (LMS=0,LINEAP=1)",A SCALE --2,1,2,K2-(K1-K2++,2,k)+(K1-K2++,2 CLIP 0-1,K2,1 CLIP 0-1,K2,1 CLIP 0-1,K2,1 CLIP 1-1,K1 FF 0-1, 0, 0, CL200, THEN 5678 ARE 0.4(1-K2) (10,0,0 ARE 0.4(1-K2) (10,0,0 ARE 0.4(1-K2) (10,0,1) ARE 0.4(1-K2) (10,0,1) CLIP 0-1,K2 FFAME c von if 10 10 >
1 F 1=0 THEN X=4
1 F 1=0 THEN X=4
1 F 1=1 THEN X=4
1 F 1=2 THEN X=2
1 F 1=3 THEN X=10
0 F 1=5 THEN CSIZE 4..5 IF (B=2) OR (B=5, THEN LABEL "INDU[TANCE -4H)" IF (B=4) OR (B=6) THEN LABEL "CAFACITANCE +5'' IF (B=7 THEN LABEL "IMPEDANCE (OHN)" SCALE -.2.1.2,L2-(L1-L2)*.2,L1+(L1-L2)*.2 FOR]=0 TO K2-10'(K!-K2' STEP -2 MOVE -.01,1*(K!-K2)/10 LABEL]*(K!-K2)/10 JF (K2)(3) OR (K1×0) THEN €130 FOR T=0 TO K1×10/(K1+K2) STEP 2 MOVE -.01,1+(K1-K2)/10 LABEL 1+(K1-K2)/10 FOR 1=8 TO 18 STEF 2 MOVE -.01.82+KI-K2>/10+1 MEMEL r2+(t1-K2)/10+1 MEXT 1 GOTO 6030 "FREQUENCY (MHZ)" NEXT I NEXT I MOVE .5, K2-(K1-K2)*.2 CSIZE 4,.5 HOVE -.61,K2 LABEL K2 MOVE -.2,K1+K2>/2 HOVE -.01, K1 LABEL K1 FOR 1=0 TO 5 LBIR 0 6010 6470 \$ LORG 8 4 4EXT] NEXT I ų, LABEL LABEL LORG

MOVE 0,4(1) LINE TYPE 1 LINE TYPE 1 D FOR 141 TG M 44 CL3P 0,1,L2,L1 IF D=? THEN ANES 0,/L1+L2)/18,1,/L1+L2) LURE 90 CSIZE 4,.5 CSIZE 4,.5 LOPC 1.2,.L1+L2.2 F #=3 THEN LAREL "OUNLITY FACTOF" F #=3 THEN LAREL "OUNLITY FACTOF" F #=4 THEN LAREL "ESISTANCE (MH." F #=5 THEN LAREL "CONDUCTANCE (MS." F #=6 THEN LAREL "FHASE (DECREE)" F #=7 THEN LAREL "FHASE (DECREE)" LJIR 0 COTO 6560 IF KI4K2>#0 THEN MOVE "5,K2-(KI-K2)#L2 IF KI4K2<0 THEN NOVE "5,K2-KI)*.1 0010 6888 0110 6888 FOR 1=0 TO 10 STEP 2 MOVE 1/10,K2-(K1-K2)+,81 MOVE 1/10,K2-(K1-K2)+,81 NEXT 1 NEXT 1 RETURN FOR 1=0 TO 10 STEP 2 Move 1.01,12+1+(L1+£2)/10 Labet 12+1+(L1+L2)/10 CSIZE 4.5 CSIZE 4.5 IF MEL "FREULENC" NHA2)" IF KLK22=0 THEN 5330 LORG 4 COR 10 0 THEN 5330 MAVE 1/10, KL+C22=101/01 FOR]+0 T⊕ € 404E 1.01,L2+1+4L1+L2\+6 6010 6230 AMES 0, 11-L2 / 10,1.L2 LABEČ ČZ+(+/L1+L2) 6 Nejt i (\$126 4.,5 16 8≈7 then 6310 INE TYPE 1 NEXT 1 6010 6350 FLKED L HEXT | .0P.C 4

6900 Pesidual: BEEP 6910 DEC 6920 DISP "Short the test fistore terminals. Then Press CONT ." 6930 PAUSE 6940 BEEF 6950 | INFIVE "Select SWEEP MODE. - PARTIAL-L.FULL=2-",W 6960 IF Me2 THEN 7100 6970 BEEP 5980 INFUT "INFOR STRETASTOR FREDATION MHZ. "VELLE2 5990 IF FL F2 THEN 7040 7000 BEEP TOUG DISP "START FREDUXS HUGHER THAN STOP FRECK PREED WONT ." 7028 PRUSE 7030 GOT+ 6980 7040 FEEF 1050 INFUT TANKS NUMBER OF STEPS : 100 OF 100CL ", F.S. 2000 IF F3=1000 THER 7090 2070 OUTFUT C:"TF",F1,"EN", "FF",F2,"EN","F1" 7880 GUT\$ 7100 7090 ONTRUT 2;"TE", FI, "EN", "PF", F2, "EN", "F2;" 7100 IF M=2 THEN F=,4 7110 IF H=2 THEN F2=110 7120 IF H=2 THEN F3=42 7130 EXUT GRAPHICS 7140 IF N=2 THEN 7170 7150 OUTPUT 2: "WL" 7160 6010 7180 TITO OUTPUT 2: W2' 7180 DISP "Measuring" 7190 FOF: 1=1 TO F3+1 7200 TRIGGER 2 7210 ENTER 238.0.1(1), J(1).A.A.F(1) 7220 | FRUAT 1,1-1), J(1-,FKD) 7230 IF J/I++-90 THEN J+1+=-89.9 7240 N=H+1 7250 IF FUT = F2+1E6 THEH 7280 7250 NEXT 1 7276 I FEERALESEE OPEN NERSHIPEMENT FEERELESEE 280 BEEP P290 BISE Permised nothing to the rest fiduate terminals. Then press (CONT)," 2300 PRUSE 7310 BISP "Measuring" 7320 IF N=2 THEN 7370 7330 IF F3=1000 THEH 7360 7340 OUTPUT CONTEN, FL. "EN", "PE", F2. "EN", "PL" 7350 GUT+ 7370 7360 OUTFUL 2;"TF", FL, "EN", "PF", F2, "EN", "P2" 1370 IF H=2 THEN FI=.4 7380 IF H=2 THEN F2=110 7390 IF H=2 THEH F3=42 7400 [F N=2 THEN 7430 7410 OUTPUT 2;"HL* 7420 6010 7440 7430 OUTPUT 2; "N2" 2440 14=61 7450 FUR I=1 TO F3+1 7460 TRIGGER Z 7470 ENTER 2:4,4,0 1., P. 1.,4.4,F.1. 7480 Hatl+1 7490 IF FUL = F2+1E6 THEN 7501 7500 NEXT | 7501 Resdaua=1 7510 RETURN 7520 Compensation: / Freeserses Dult MEASUPENENT estatements 7530 BEEF 7531 IF Pesidara O THEN 7540 7532 DISP (CRUTTON : NO PESIDUAL DATA, Press CONT " 2533 FRUSE 7534 Residera=Peedata+1 7535 GOSHB Residual

#890 ! ----- PESIDUAL CONFENSATION ------- +

2540 OUTPUT 2:"H1" 7550 DISP "Connect DUT to the rest for dre terminal, Then press Could ." 7555 PRUSE 7566 LINPUT "Logist DUT wanie (UP) TP 30 (INSPACITERS (NAT 7570 IF W=2 THEN 7420 7580 IF F3=1000 THEN 7610 75(40 OUTPUT CONTEN, E1, HEDH, HEFH, E2, HEHR, HE1H 76130 00100 .7620 7610 OUTPUT ZUNTFNIEL, MENNIMPENIEZ, MENNIMPEN 7620 IF H=2 THEH F1=,4 7630 IF H=2 THEN F2=110 7640 IF H=2 THEI F3=4: 7650 IF N=2 THEN 7630 7660 OUTPUT 2; "W1" 7570 15610 7690 7440 OUTPUT 2:"N2" 7490 N=0 7700 FOR 1=1 TO F2+1 7710 TRIGGER 2 7720 ENTER 218,8,6-1, H-1-, A, 8, F-1-1730 BISP Hitessurning 2240 N=N+1 7750 IF EVIN=F2+1E6 THEH 7770 7760 HECT I 7770 F ----- FERIDUAL CORPENSATION -----7780 FIDED 3 7790 PPINT OSTER NAVO, "FREQUENCIA MH2 (", "MAGNETULE", (ANN), (, PRASE) LEGREE. 7880 FOR I=1 TO F3+1 7216 H(P-1-----2) 7#20 - L/IN=(0/I)+COS(H(1/N=0)[-+COS(P(1/((+1)))]+1(1)+(0))/((-)) 7890 N. I are Q. I SASING HULL CONFIDENCE I SAN POLICIAN INFORMATION (1997) 7840 C/I == 100R(M/1+ 2+L-1+ 2+ 7850 IF LIFT O THEN LAINE.01 7251 IF KSGN/L+I>>=1+ HND +SGN+M+1 →=_1+ THEN TREA 7852 7253 7854 COTO 7:870 786.0 DO 1, #ATH(N) 12 L(1++ PRINT LEVIS LEG. (11) DOLD 79.70 7338 IF T'C(L) THEN T=C(1) 7440 IF SCARSED IN THEN SEARSED IN 1.1 7900 HEST I 7910 STANDARD

7920 PETURN



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