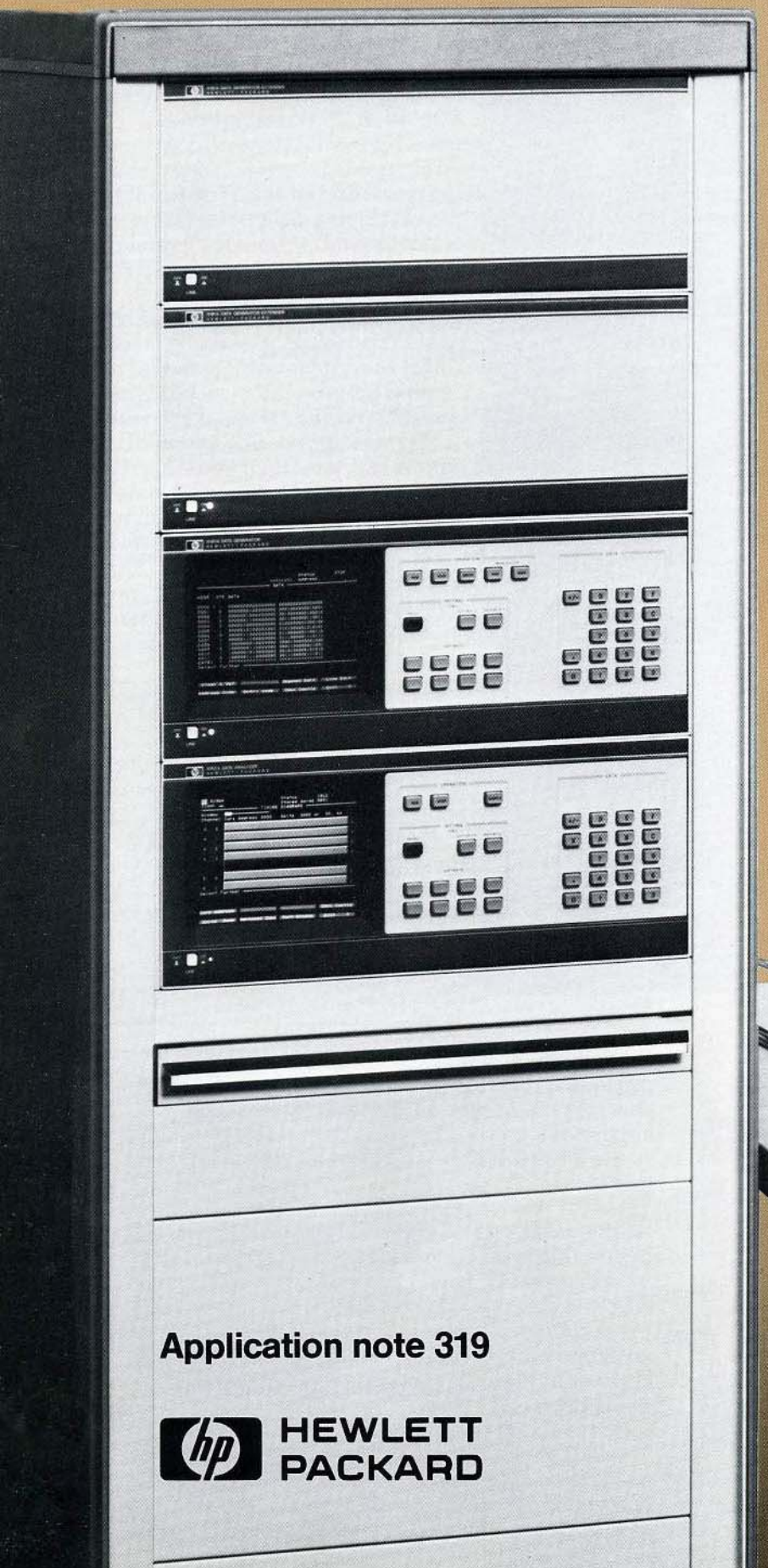
Parametric characterization of digital circuits up to 50 MHz with the 8180 A / 8182 A stimulus/response system



Application note 319

HEWLETT PACKARD

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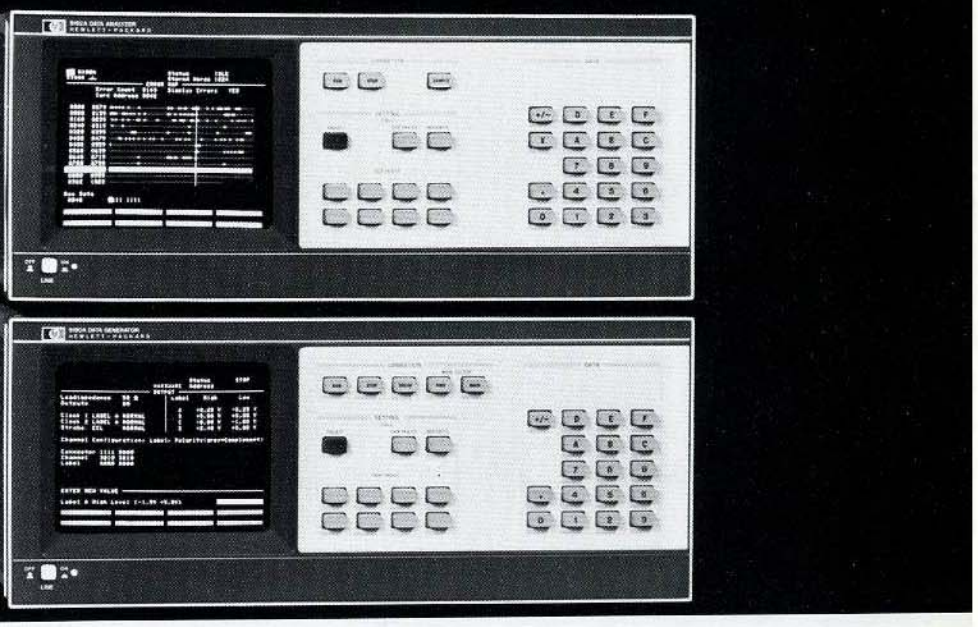


IC - Test protocol

	R inputs	OR inputs
Setup time :	11,5 nsec	12,9 nsec
Hold time :	5,1 nsec	0,7 nsec
Propagation delay:	20,7 nsec	25,8 nsec
Lower Threshold :	0,77 Volt	0,81 Volt
Upper Threshold :	2,44 Volt	2,89 Volt

Test parameters for digital circuit characterization

Introduction

Digital circuit complexity ranges from simple logic gates to PC-board systems of large computers. Irrespective of the application and complexity, all digital circuit blocks can be characterized by their logic function and their input and output parameters.

The 8180A, 8182A system design enables engineers to characterize individual circuits by analyzing the response to specific stimulation.

In addition to testing the logic function, which is specific to a digital circuit type, it also measures the physical parameters which apply to all circuits.

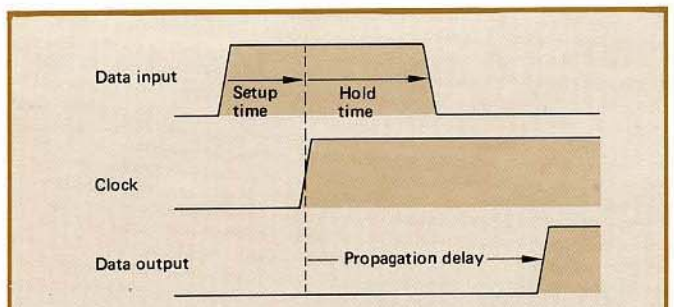
The representative timing parameters

For error-free operation, synchronous devices, e.g. RAM's or latches, require the applied data to be stable a 'setup' time before and a 'hold' time after the active clock transition. Asynchronous devices, such as gates, also require a specific response time in which the input data must be stable.

The propagation delay is the time between input stimulation and output reaction. The value depends on the complexity of the circuit (e.g. for IC's: MSI, LSI, VLSI) and on the technology (e.g. MOS, TTL, ECL).

Propagation delay, as well as setup and hold times, are the timing parameters limiting a circuit's maximum data rate.

To measure the setup and hold times, the stimulating instrument must deliver the functional pattern with the appropriate timing parameters, represented by delay and width. At the same time the receiving instrument must recognize errors which occur due to these parameters being less than the required values.



The timing parameters limiting a circuit's maximum data rate.

To measure the propagation delay, the analyzing instrument must sample the circuit output data at a delay after the system clock.

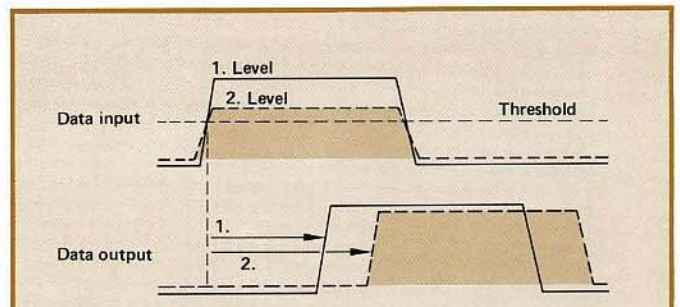
The values of these timing parameters vary from under 1 nsec for ECL gates, to over 100 nsec for MOS gates. It is obvious that the timing resolution of the measurement instrument must be higher. So an instrument with 10 or 20 ns resolution is absolutely inadequate.

Therefore the 100 ps resolution of the 8180A, 8182A system for its key timing parameters is excellent. These parameters are:

the data generator's period; individual delay and width for timing and clock channels; the data analyzer's sampling point placement and the real time compare window.

The level parameters

The dynamic input characteristic influences the timing parameters. For example the reaction time of a comparator depends on the input overdrive. That's why the timing parameters should be tested with different input amplitudes.



Different propagation delays depending on input threshold overdrive.

To do such 'at-speed' level testing, independently programmable high and low levels for individual channels are needed so that even mixed logic circuits can be stimulated. A high resolution, such as the 8180A's 10 mV, assures reliable measurements.

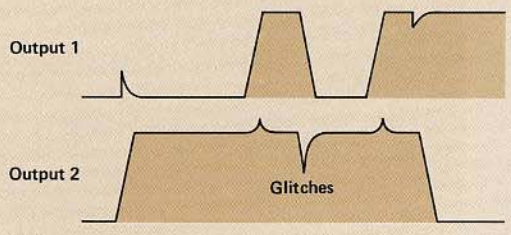
At the output of the device under test, the variation of amplitude over the frequency, that means the 'at-speed swing', is of great interest. A driver may have the ability to deliver the DC current under the specified fan-out conditions, but cannot deliver adequate peak-current to drive the parasitic capacitances at high clock rates, and so the output swing decreases.

The 8182A therefore has two independently programmable thresholds (DUAL LEVEL) per channel, with a high 10 mV resolution, to test the circuit's output data as high, low or intermediate.

The output stability

Another problem in digital circuits is high frequency crosstalk, where fast transitions on one line introduce instabilities on another. Furthermore, glitches can be caused by internal propagation delay mismatching.

These data instabilities or hazards can be sensed by a "glitch detector" feature of the data analyzer. But distinguishing automatically between troublesome glitches during 'data valid', and unimportant ones during 'data change', is only possible with the "real time window compare" feature offered by the 8182A (See page 11).



Crosstalking causes output instability.

Requirements of the measurement instruments

The trend of today's digital circuits is to rapidly increasing complexity. In order to prevent similarly increasing test time and costs, the measurement instruments need to be more sophisticated. That means the instruments must combine several features.

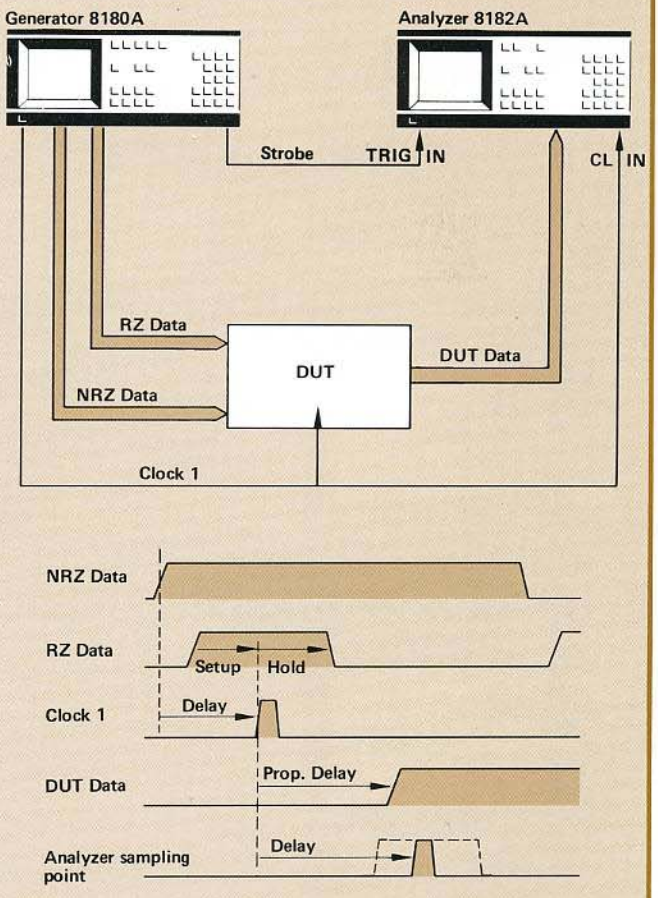
A combination of flexibility and easy operation provides adaptability for changing problems, and enables users to have quick access to all test capabilities.

To combine input measurements and stimulation, the stimulus must combine the timing and level capabilities of pulse generators with the multichannel functional stimulation of word generators with a deep memory.

The analyzing instrument must combine normal logic-analyzer features with additional capabilities, such as fine timing and threshold resolution, for parametric hardware analysis.

The 8180A, 8182A system combines all these features and is therefore the ideal setup for present and future digital circuit characterization.

The graphic shows how the 8180A, 8182A system can be used to stimulate and analyze a circuit under test. Timing and level parameters, separately programmed for different channels, plus functional data pattern are used to perform the characterization.



The 8180A allows the user to vary skew, setup, hold time and input levels; the 8182A allows precise edge location and output level measurement.

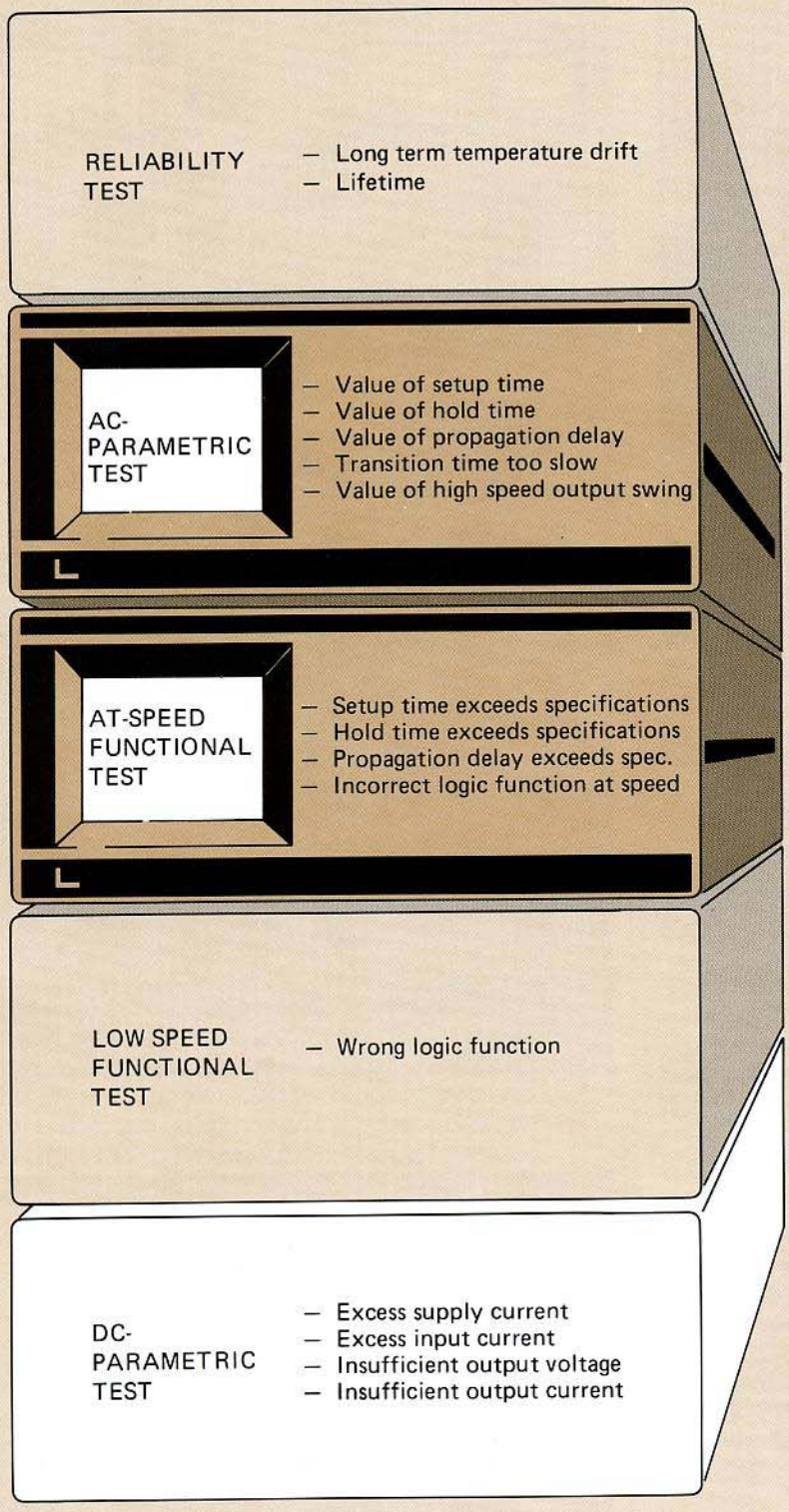
SUMMARY

For parametric digital circuit testing, the parameters of interest are:
- Setup and hold time
- Propagation delay
- Output swing at speed
- Crosstalk .

The 8180A, 8182A system is able to measure these parameters with a very high resolution.

IC investigations and tests

IC test types and criteria



The reliability tests of devices versus time and environmental parameters is performed in quality assurance and vendor evaluation. With these time-intensive tests, statistics can be created for specific devices and production technologies.

IC and board designers need to measure parameters in order to specify the performance and optimize the yield of IC's, or to get a high 'turn on rate' for boards.

At-speed functional tests are indispensable for high volume production, especially for large scale integrated circuits. With this pass/fail test, about 90 % of the faulty IC's are detected.

Low speed functional test, as often performed at incoming inspection, yields 55 % to 70 % of the faults, depending on the IC's complexity.

Bonding or process failures are detected by measuring the DC-parameters in IC production or incoming inspection.

Parametric IC tests in various applications

The 8180A, 8182A system is optimized to do 'at speed functional' and 'ac-parametric' tests.

The 'at-speed functional' tests verify correct operation of IC's in the framework of the specified characteristics. All limit values of setup and hold times, input and output levels, are programmed for a test. The result is a 'passed' or 'failed'.

In the 'ac-parametric' test, the most interesting values of the IC's parameters are measured.

The two major groups doing these IC tests, IC manufactures and IC users (equipment manufacturers), have different reasons for performing them.

The IC manufacturers

Whether manufacturing commercially or captively, newly-developed IC's must be characterized so that the process can be optimized, or the sales specifications established.

Up to now, the designer has had the choice of building his own test setup with pulse generators, oscilloscopes and counters, or to use a production IC-tester (if available).

But neither really matches all needs. The self-built test setup does not offer comfortable solutions such as: high channel count, pattern edit, programability or overall specified system accuracy. So the self-built setup is not very effective.

The production IC-tester is more complete, but therefore expensive. It offers no great flexibility for changing parameters and is often not readily available for engineering tasks. The specialist for IC design is possibly not the specialist for the IC-tester, and multiple compilation runs for setting up a test program prolong the non-availability of the machine for the production tasks. Furthermore a 10 or 20 MHz maximum data rate may not be sufficient to examine the IC's at their operational speed.

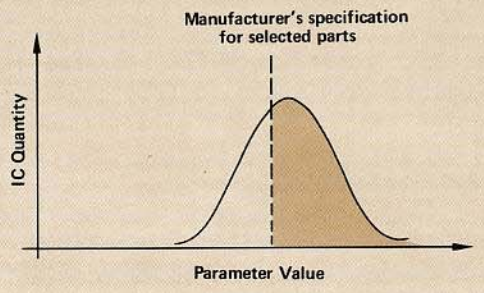
The effective way to characterize IC's during development is to use an 8180A, 8182A system, which offers the comfortable test capabilities on the laboratory bench.

The equipment manufacturers

For the manufacturer of high-quality equipment who wants to reduce PC-board test and warranty cost, IC test has to start during the product development. A characterization gives him information of the actual IC-parameters (propagation delay, maximum clock frequency, setup and hold time, at-speed output swing or dynamic input hysteresis).

This knowledge of the differences between the actual parameters and the specifications gives valuable information in materials engineering for component approval and incoming control.

For example, on a decision to take a single source device or not, a statistical analysis of the measured parameters tells whether the IC manufacturer must select his devices, and whether he has problems to deliver to specification.



Example of a statistical parameter analysis, showing a possible relation between real and specified value.

Or, if a device causes repetitive trouble in production, a characterization clarifies, whether the problem is due to a deterioration in IC quality, or whether the development board was made with 'well in specification' IC's, while the accumulation of propagation delays of some 'marginally in specification' IC's, causes the error.

The characterization of IC's becomes increasingly necessary to improve product quality and reliability, and to reduce production test time and cost, thus maintaining market share of a product. The 8180A, 8182A system offers the capabilities to make characterizations efficient.

SUMMARY

The different test types for IC's and their efficiency was described, focusing on the 'ac-parametric' and 'at-speed functional' tests for IC manufacturers and IC users. The 8180A, 8182A system is a very user-friendly tool, optimized for these applications in the engineering area.

Example of a parametric IC-test

This example shows how the 8180A, 8182A system is used to test an AM 2909 sequencer. This complex TTL IC sets high requirements with its short timing parameters. These are conveniently and accurately tested with the 8180A, 8182A system in manual or automated operation. The operating concept and the permanent access to any instrument parameter support the user. Time is saved and engineering efficiency enhanced: not weeks of software generation, but quick test results.

Performing a characterization starts with a look at the blocks and functions of the device. The pattern for the test is then generated according to that structure. Having a functional pattern, the timing and level parameters can then be set up on the stimulus/response system. Variation of the parameters leads to the IC's operating limits when errors are indicated on the 8182A's display. The test results are simply read from CRT or via HP-IB.

Setting up the test pattern

The way in which a test pattern is assembled will depend on the IC, test objectives, personal knowledge and equipment features.

Stimulus patterns can be generated with simulation programs, but these place heavy demands on computing time. Often the engineer creates effective patterns word-by-word, and he needs good editing features on the stimulus to do this efficiently. The corresponding analyzer pattern can be recorded using a known good device, or can be calculated using a simulation program.

Editing the pattern is facilitated with the 8180A, 8182A system. The comfortable edit features allow rapid setup and convenient modification of testvectors in many ways. It is very important that a pattern for a functional IC test can also be used for a parametric test. This is because the timing parameters and their adjustment may be programmed independently for different measurements always using the same functional pattern.

The description of the IC test starts with the way of how to get such a functional pattern correlated to the hardware conditions.

First the basic distinction between input, output and bi-directional pins is made. Then the 8180A stimulus channels and 8182A receiving channels are assigned to these pins, applying tri-state pods to I/O pins.

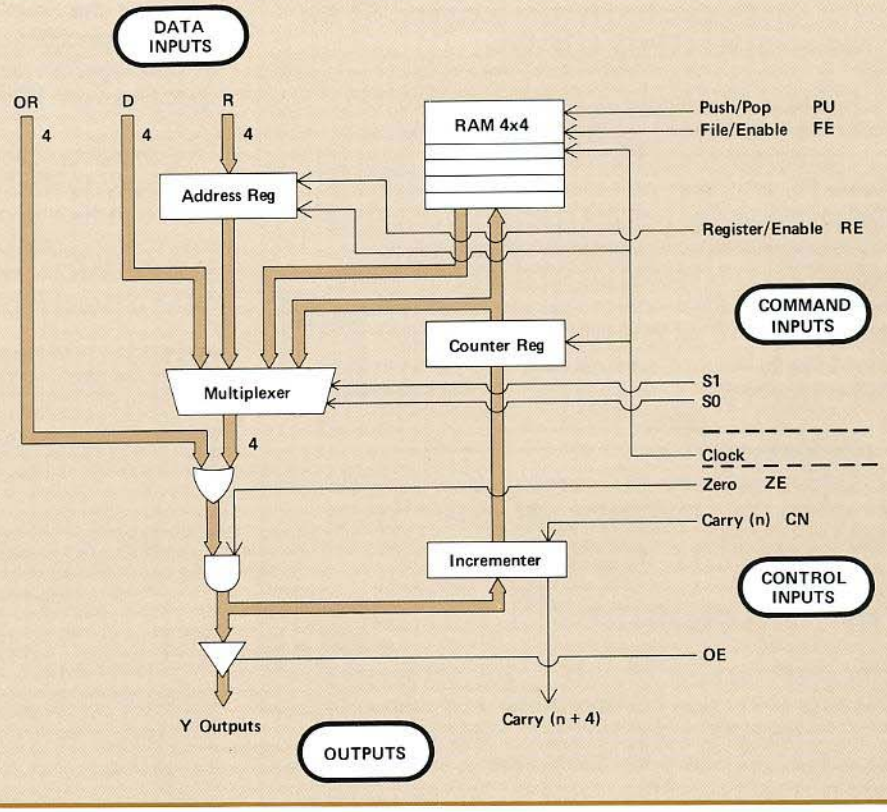
Now groups of homogeneous input and output pins are built. For our example, these groups could be: (see diagram below).

- Data inputs
- Command inputs
- Control inputs
- Outputs

Description of the tested IC: sequencer AM 2909
In a computer a sequencer is typically used in the micro program control of a bit-sliced CPU. The device manages the sequence of microprogram steps by outputting start-address, follow-address and branch-address to the microprogram memory. For this task, the sequencer contains:

1. *A multiplexer for selecting the output address.*
2. *A 4x4 bit memory to hold subroutine addresses.*
3. *Logic gates to generate addresses coherent with external lines.*
4. *Registers to latch addresses.*

The block structure contains an asynchronous and a synchronous part. The ranges for propagation delay, setup and hold time are from 0 to 50 ns.



With these groups, the generator pattern can be swiftly set up because they allow full use of the 8180A's comfortable editing features such as: arbitrary channel grouping and coding, standard patterns, macro word entry, line and channel editing, copy functions and memory segmenting.

Pattern editing strategy for different pin-groups

For the sequencer example, the use of these edit features allows the following approach.

A) Data inputs: they do not influence the IC's function, so the data for these channels can be set up with standard functions (e.g. random data or up-count function). That's quickly done with a few keystrokes.

B) Command inputs: they control the function and logic state of the IC under test. Setting up these patterns require most work. In many cases not all binary combinations of these inputs are meaningful. In our example, there are 5 command lines, but only 12 combinations (instead of $2^5 = 32$) are valid commands. For quick, effective pattern editing, these commands should be coded (e.g. hexadecimal) or defined with a "macro-function", where one long vector can be labeled for repetitive insertion.

C) Control inputs: key set the device under test to a specific state. Generally, they change state infrequently and are therefore easily set up using 'set' or 'clear', and then modified using the channel edit feature when their function is tested.

Performing a manual "ac-parametric" test

To measure the timing parameters of the above IC only those functions concerned with the parameter to be measured need to be stimulated.

Three parameters are measured:

- the setup time of the R-inputs –
- the hold time of the R-inputs – both with the aid of the generator timing channels
- the propagation time (from the R-inputs, via the multiplexer to the Y-outputs) with the aid of the data analyzer.

– The stimulus pattern is set 16 test-vectors long; (destinated by the possible bit combination of the 4 data inputs), and simply programmed with the up-count function.

– The OR-inputs are set to "0", so they do not influence the test.

– The D-inputs need not be stimulated for the test.

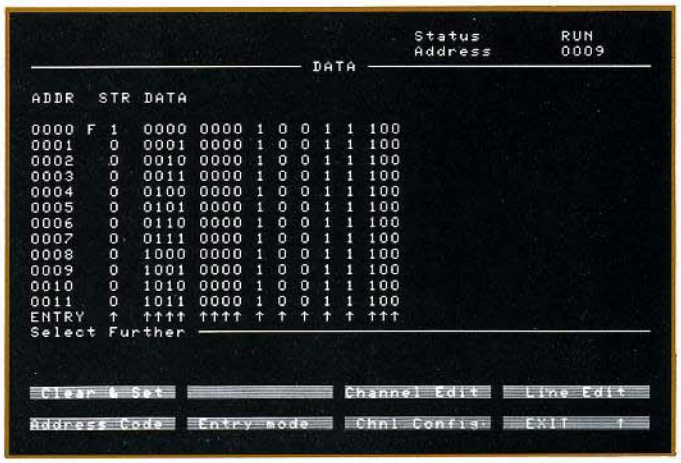
– The command inputs are always stimulated with the same command: "use address register for address" (10011) to activate the desired data path in the IC.

– The control inputs are set so as not to influence the measurement (100).

	DATA INPUT		COMMAND INPUTS					CONTROL INPUTS		
VEC. NR.	R 3210	OR 3210	S1	S0	RE	PU	FE	ZE	0E	CN
0	0000	0000	1	0	0	1	1	1	0	0
1	0001	0000	1	0	0	1	1	1	0	0
.	....	....	.	.	.	.	.	.	.	.
15	1111	0000	1	0	0	1	1	1	0	0

Stimulus pattern segment for the manually performed sequencer measurement.

The analyzer's expected data pattern is the same as the stimulus 'R'-pattern (up-count) but is delayed by the IC's address register for 1 clock period. Therefore the 8182A data analyzer is simply triggered by the 8180A data generator's 'Strobe' channel one clock period after the start address. The 8180A 'clock 1' channel is used as the IC's clock and as the external clock of the analyzer. The recording depth (stop delay) of the analyzer is set to 16 clock cycles, to match the generator's data cycle.



The 'data page' of the 8180A with the comfortable edit facilities via softkeys.

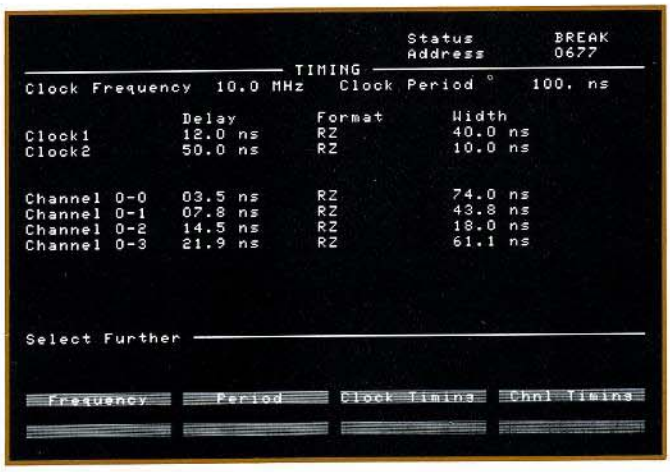
The timing parameters are then set up to safe operating values. That means:

- The stimulus data width is 50 ns (greater than the sum of setup and hold time).
- The stimulus clock delay is set to 35 ns (greater than the setup time).
- The analyzer's sampling point is set to 60 ns after the clock transition (greater than the propagation delay).

Example of a parametric IC-test – continued

Having thus set up stimulus and analyzer with the correct data and 'safe' timing, the live keyboards of the 8180A, 8182A system show their full time-saving advantage.

With the instruments running continuously, a parameter is measured simply by decrementing its value until the analyzer's display shows an error. The parameter has now reached the IC's limit, and the value can be read directly from the display.



The 'timing page' of the 8180A, for changing delay and width parameters.

– To measure the setup time of the AM 2909's R-inputs the delay of the clock channel is decremented.

– To measure the hold time, the width of a stimulus data channel is decremented.

– To measure the propagation delay, the sampling point delay of the analyzer is decremented.

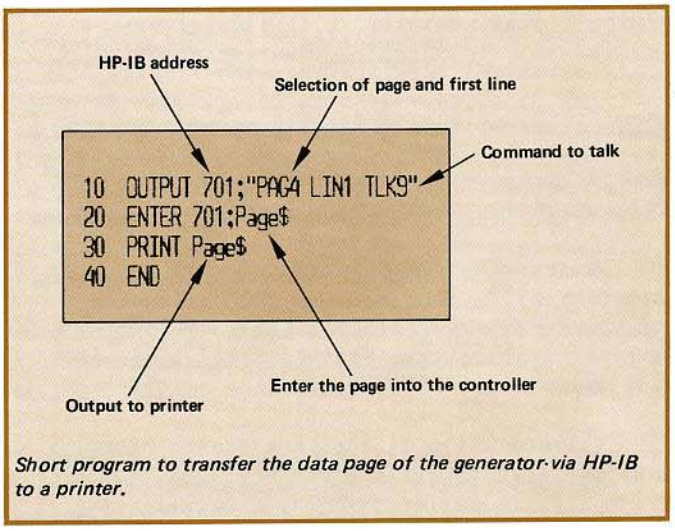
(See timing diagram on page 3).

Performing an automatic "ac-parametric" test

To test all functions of the IC, it is useful to serialize multiple short functional test patterns as described above. The expansion of the setup with a controller offers comfortable handling of such long patterns. It adds mass storage (disk, tape) and documentation possibilities (printer, plotter) and above all, runs the complete IC-test automatically.

The instruments are easy to control from a computer, via HP-IB, because there is direct access to all parameters without moving cursors or rolling pages.

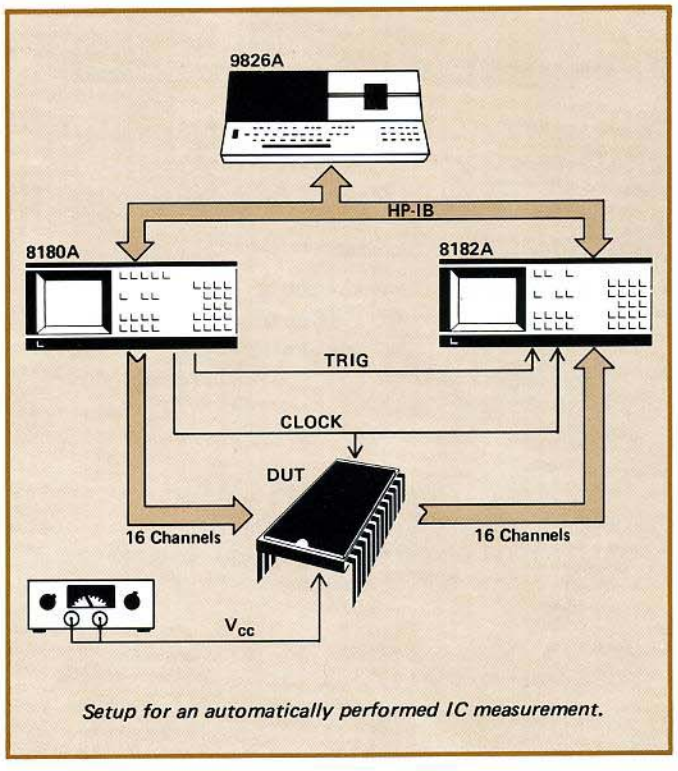
The following example illustrates the clear syntax and also the comprehensive data access for thorough documentation.



Short program to transfer the data page of the generator via HP-IB to a printer.

With a high I/O-rate controller, for example HP's 9826A, it takes only 0.1 s to download 16 channels of data 1024 bit deep to the generator in the fast data mode. Long data sequences in excess of 1 kbit can therefore be simulated by reloading the memory in a short time.

The following figure shows a typical automatic test setup. The 9826A desktop computer is used to control the instruments via HP-IB and to make the decisions for the test flow.



Setup for an automatically performed IC measurement.

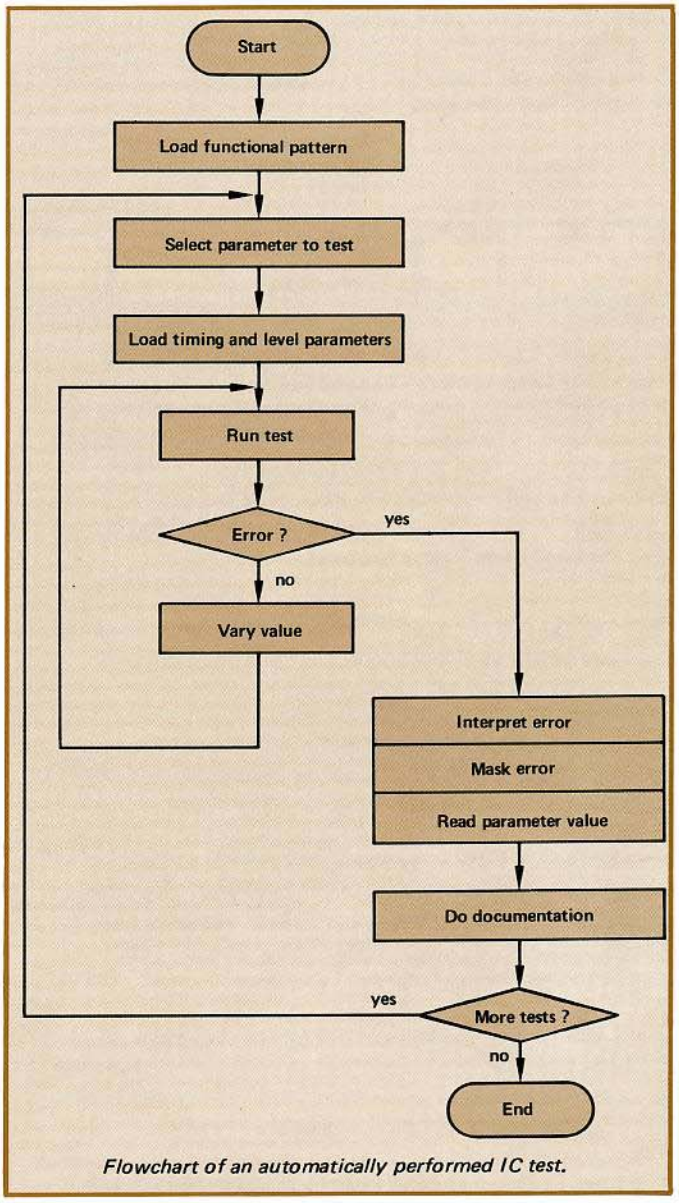
The test pattern for such a setup includes functional groups of test vectors. For the sequencer example these groups are:

- R-input test
- OR-input test
- continue test
- control input test
- D-input test
- up-count test
- store/readout test

This pattern is used repetitively to stimulate the device, changing parameters with each cycle. The data analyzer records and compares the output pattern of the IC. At the same time the controller interprets the errors and handles documentation, statistics and initialization of the next cycle. The entire test can be repeated for multiple devices and for different environmental conditions. For the sequencer test no reloading of patterns for generator or analyzer is necessary because the test parameters can be programmed independent of the logic function.

For example, to measure the different propagation delays of the IC, the measurement can be performed as follows. The sampling point delay is decreased from the safe area of over 60 ns, to under 10 ns, decrementing the value before each test cycle. The controller interrogates the data analyzer at each cycle to determine if a wrong data vector is recognized.

In case an error is reported, the controller talk-addresses the analyzer, which then outputs the error line and error bit. The controller interprets what test at which channel has failed. The numerical value of the programmed delay is the result and is related to the parameter in a test protocol. For the next test, the already received 'wrong' testvectors, are masked with 'don't care' in the data analyzer, so no further comparison is done with them.



Flowchart of an automatically performed IC test.

SUMMARY

Pattern editing is facilitated with the 8180A, 8182A system, because it offers the capabilities for comfortable, structured pattern creation. The systematic approach to establish a test pattern for a characterization is shown in an example.

Some manual measurements, the setup, and the test flow of an automatic IC characterization are described, illustrating the rapidity and convenience of obtaining results with the 8180A, 8182A system.

PC-board investigations and tests

Board characterization has much in common with IC characterization. Consequently, the following paragraphs concentrate on aspects unique to boards and breadboards.

Board test in R & D

To create a 'well designed' digital circuit, a profound knowledge of the IC's employed is needed. These facts can be gathered by IC-characterization, enabling the engineer to calculate the propagation delay paths on a board. Further, the matching of the various propagation delays and logic functions should be verified on a prototype board. This checks the safe operating area of the parameters under different circumstances, ensuring 'high turn on rates' in board production.

Parametric circuit test at board level has the same requirements and objectives as at IC level, but differs in complexity and error sources. For example: The influence of crosstalk on a bus with parallel lines, or data stability in a time window around the system's synchronous clock, are of interest for proper handshake operations.

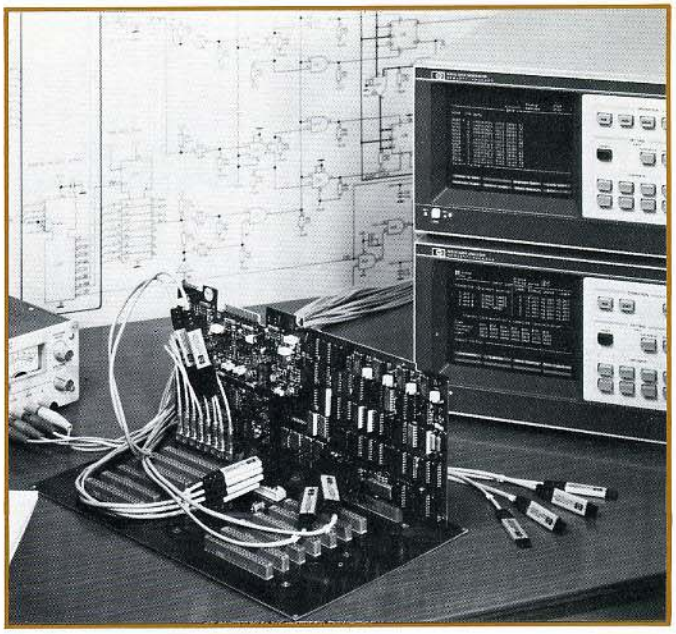
The 8180A, 8182A system can perform such a board test, for it offers the high speed, the pin-count and the concept to simulate various peripheral circuits, and to do the analysis of the respective response on the board.

The high performance of the system allows all critical functions and parameters on a digital board to be tested adequately as under real-life conditions (timing, levels, glitches, data stability).

A closer look at the generator proves the above statement. For example, for mixed logic stimulation, different high level / low level pairs can be assigned to individual channels. Also its 50 ohm output driving technique guarantees low reflections and the ability to stimulate even 50 ohm terminated busses, or simply to have a high 'fan-out'.

Board test in production

In many cases, high volume board test can be reduced to detecting solder and loading errors, assuming good design and tested IC's. But for high-reliability applications such as in aerospace equipment, 100 % parametric test is essential. In this environment the 8180A, 8182A system is a compact high speed solution which can be used manually or for upgrading existing ATS to at-speed performance.



Simple in-circuit probing is possible with a comprehensive set of accessories.

Example of a parametric board test

For a measurement instrument, a so-called 'address control board' has to be tested. It contains: microprocessor accessible TTL control circuits, and ECL circuits for high speed strobe signals and timing edge placement.

The 8180A data generator must stimulate the board with many channels at TTL levels, delivering the signals in a single initialization cycle for the data bus, address bus and the control bus. In a subsequent repetitive data readout cycle, the ECL part of the board is exercised with several data channels and appropriate timing, levels and two-phase clocks.

The 8182A data analyzer is used to verify the logic functions on the board. The propagation delays are measured to confirm the calculated critical data paths, and glitches are captured. Logic function and propagation time measurements do not differ essentially from those in IC characterization. ECL signals are particularly sensitive to glitches, so the influence of 'strip line termination splitting' and crosstalk must be considered.

Because of the data character, the extreme duty cycles of these signals, and the number of channels, an oscilloscope cannot be used to do these measurements satisfactorily.

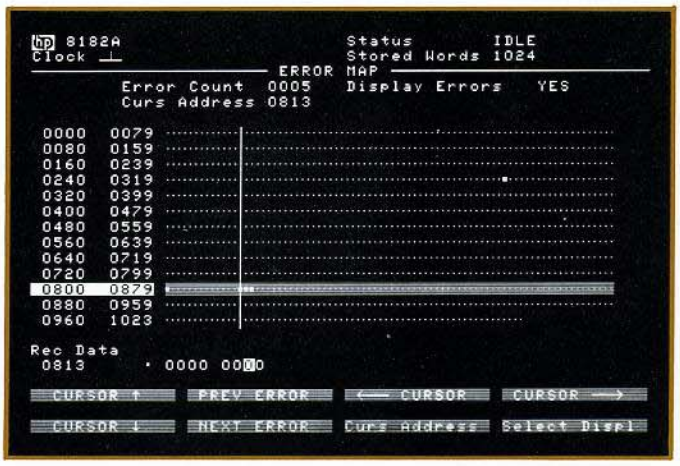
Locating errors

Obtaining detailed information on what really happens on a board is done in steps.

First the data analyzer is used in a logic analyzer mode, checking the logic functions and looking for glitches or hazards. Many channels are probed on the board to pick up parallel data on different sequential gate levels. This allows error nodes to be located and propagation delay measurements.

The second step concerns the identification of critical glitches. In asynchronous logic no glitches are tolerable. In synchronous logic, data has to be stable and valid only during a time around the respective clock transition. Distinguishing between troublesome and unimportant data instabilities with a normal logic analyzer is time consuming. Even if a logic analyzer with extremely high asynchronous sampling capability is available to locate a glitch within a system period, the user can't be sure that the glitch location is always the same, or if it randomly disturbs the proper board function. Therefore this test would have to be repeated several times.

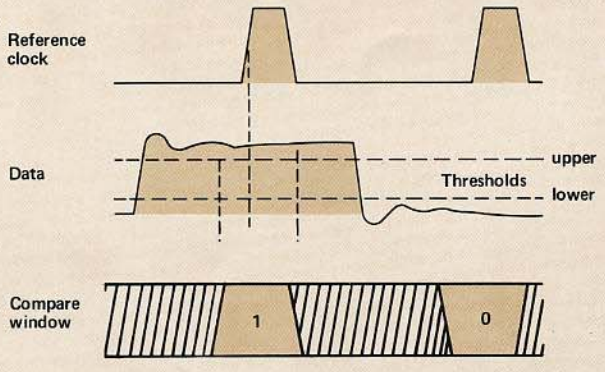
In contrast the 8182A offers an additional operating mode, the "real time compare mode" which does exactly what is required. In this mode, the instrument does not record any data, it compares incoming data with expected data at full speed. The comparison is done each period for a preprogrammed time (the 'window width') and the compare window can be placed anywhere within the period, with 100 ps resolution. Thus, it is very easy to see if data is stable a setup time before, and a hold time after the system clock transition.



The error map of the 8182A gives a quick overview of the result.

Furthermore, the comparison is done realtime. This allows the 8182A to operate in continuous loops without gaps, and ensures that all data can be compared and that even sporadic errors are detected.

The second step commences by dumping the data from the board into the 'expected data' memory, and then modifying for a valid pattern with the 8182A's convenient editing features. Then the 8182A is switched to real time compare mode, and the comparison window within which the data must be stable is placed. The 'error map' is then used to see if there are errors. Here too, the live keyboard allows variation of the compare window width and placement, while looking at the new compare result: a convenient, reliable way for measuring the limits of data stability.



Testing data stability during a programmed compare window, against the two thresholds gives immediate feedback about all critical parameters.

SUMMARY

The differences between PC-board test in a production environment and in board development are mentioned. The excellent matching of the 8180A, 8182A system features to the parametric PC-board test requirements is proven by an example. The system is enhanced by its window comparison feature.

Feature summary

Feature Summary of the 8180A/8181A Data Generator

- 1 Hz – 50 MHz data rate
- 8–64 NRZ-channels
- up to 8 RZ-channels and two clocks, all with delay and width resolution of 100 ps
- 1 kbit memory/channel, non-volatile
- –2 V to +17 V into open (–2 V to +5.5 V into 50 Ohm with 10 mV resolution)
- < 3.5 ns transition times for TTL, typically 1.5 ns for ECL
- comfortable data pattern editing; convenient softkey operation
- full HP-IB programmability
- tri-state capabilities

Feature Summary of the 8182A Data Analyzer

- 1 Hz – 50 MHz data rate (synchronous and asynchronous)
- 8–32 channels with 1 kbit memory/channel
- delayable sampling point with respect to the active clock slope with 100 ps resolution
- real time window compare with 100 ps resolution for window width and placement
- real glitch detection and storage
- single or dual threshold measurements
- comfortable compare pattern editing; convenient softkey operation
- full HP-IB programmability

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