Agilent ATF-50189
2.4 GHz high-linearity second stage LNA/ driver using ATF-50189
Application Note 5106

Introduction

Agilent Technologies's ATF-50189 is a high linearity, medium power, low noise E-pHEMT FET in a low cost surface mount SOT89 package. It is suitable for high output IP3 LNA Q2 & Q3 stages or driver amplifier in receiver or transmitter designs, respectively. This short note highlights a 2.4 GHz amplifier that is suitable for adaptation into WLAN & ISM-band products.

The ATF-50189 is packaged in an industry standard 4-lead SOT-89. The package has two source leads with large surface areas for efficient heat dissipation and low inductance RF grounding.

This application note describes the use of the ATF-50189 in an extremely high dynamic range low noise amplifier (LNA) or buffer amplifier. The demo-board's nominal performance at 2.4 GHz are: -G = 12.8 dB and output P1dB = 25dBm. With some optimization of the DC & RF operating conditions, an output intercept point of 45dBm can be easily achieved. The input and output return losses are better than 12 dB.

EPHEMT biasing

The enhancement mode technology provides superior performance while allowing a dc grounded source amplifier with a single polarity power supply to be easily designed and built. As opposed to a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Biasing an enhancement mode PHEMT is as simple as biasing a bipolar transistor. Instead of a 0.7V base to emitter voltage, the enhancement mode PHEMT requires about a 0.6V potential between the gate and source, V_{gs}, for the target drain current, Ids.

Circuit Description

Biasing is accomplished by the use of a voltage divider network consisting of R2 till R9. The voltage for the divider is derived from the drain voltage which provides a form of voltage feedback to help keep drain current constant.

At the input side, the combination of R1 and C7 enhance Q1's stability by terminating the gate resistively at low frequency. L1 and C5 form the bias-decoupling network. To reduce circuit loss, L1 should have the following characteristics: - high unloaded Q, (Q_{UL}) and, operated below its Self Resonant Frequency (SRF). C5 is dimensioned for low reactance at the operating frequency (f_{opr}). C1 & C2 form a capacitive tap matching for Q1's input.

At the output, the ferrite bead chip, L3, works in conjunction with C8 to provide a resistive termination down to the tens of MHz range. Although a resistor can provide the same function, the power dissipation will be high. L2 and C6 form the bias-decoupling network. L2 and C6 are chosen with the same criteria as L1 and C5. C3 & C4 form a capacitive tap matching for Q1's output.

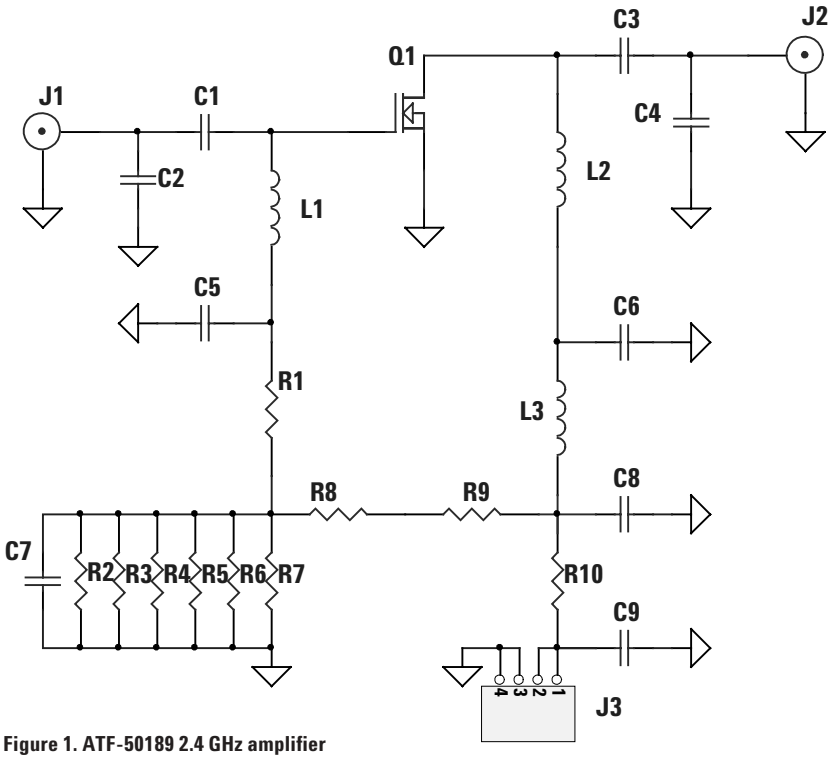


Figure 1. ATF-50189 2.4 GHz amplifier

Demoboard

A generic demonstration board is available for quick prototyping and evaluation of the ATF-50189 in the VHF till 3 GHz range. To replicate the material cost and space constraints imposed on consumer products, the demoboard was designed around low cost 0.031inch FR4 dielectric and small surface mount components. Unfortunately, the significant high frequency losses in FR4 and low Q inductors detract from the ATF-50189's true performance potential. RF connections to the demoboard are made via edge-mounted microstrip to SMA coax transitions, J1 and J2.

The demoboard requires a single 4.8 V power supply. The relatively high current (> 300 mA) drawn by the demoboard can result in appreciable voltage drop over long supply wires. The 4-pin connector, J3, permits 4-wire "Kelvin contact" to be used for compensating for voltage drop in conjunction with power supplies that support such function. If conventional 2-wire supply is used, J3's two outer leads are left unconnected.

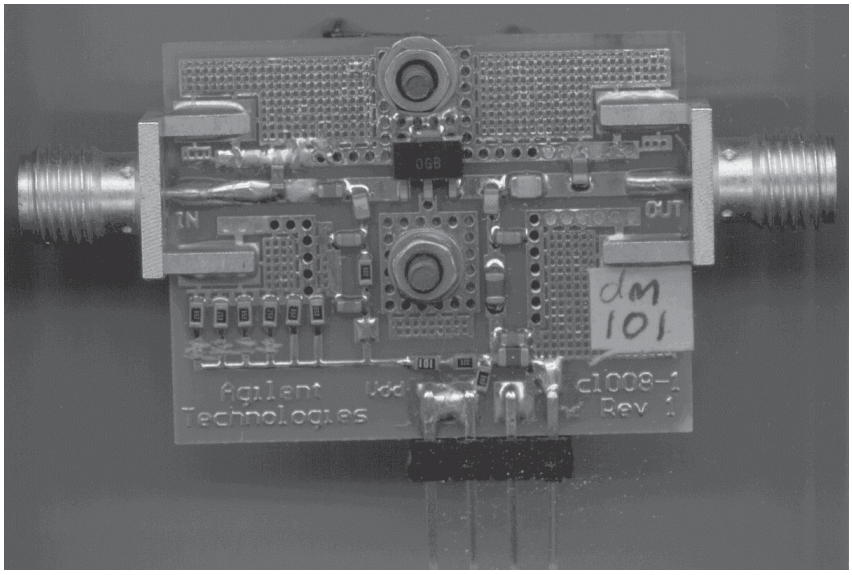


Figure 2. Fully assembled demoboard with connectors and screws for heatsink

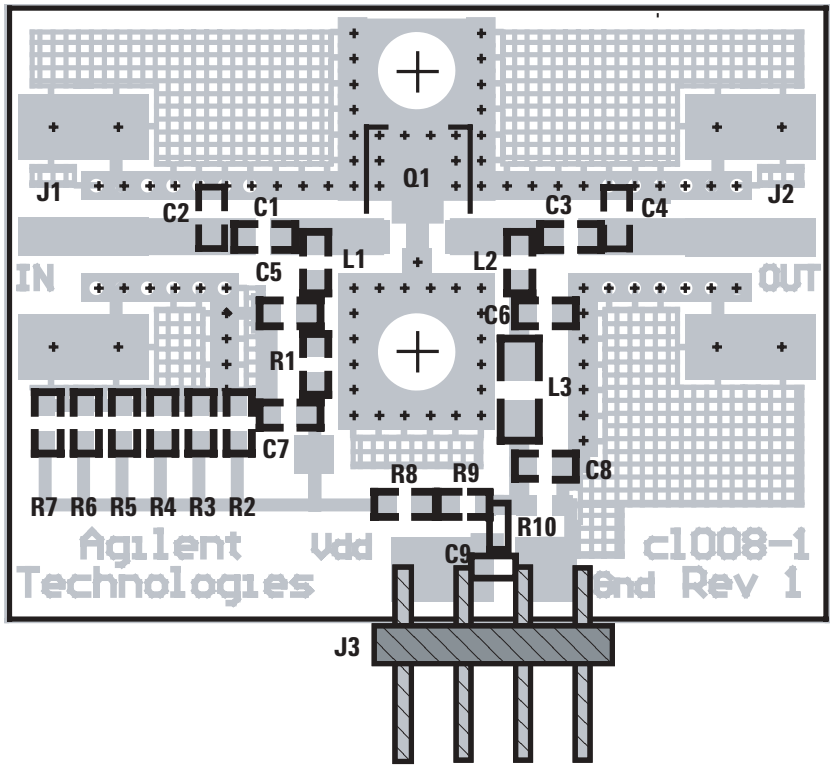


Figure 3. Component layout legend

Just like bipolar transistors, which exhibit a wide variation in HFE within a particular part number, the ATF-50189's forward transconductance, g_m, can vary from unit to unit. The resistor network, R3~R7, on the demoboard allows fine-tuning the gate bias, Vg, to cover the range of g_m variation. The individual PCB traces connecting to R3~R7 is cut one at a time until the demoboard draws the target current range of 315 ± 15 mA. This results in V_{ds} = 4.5 volt and I_{ds} = 280mA at the device-under-test, Q1.

The PCB trace leading to the positive supply needs to be cut to fit the resistor, R10. By connecting a voltmeter across R10, the current drawn by the demoboard can be monitored.

Two 3mm holes are provided for mounting a heat sink to the ground plane on the opposite side of the demoboard. Multiple via-holes around Q1, conduct heat to the ground plane and heat sink interface. To reduce the interface's thermal resistance, apply a thin layer of silicon grease thermal compound and tighten mounting screws with the correct torque recommended by the heat sink manufacturer (usually slightly beyond finger tight).

Table 1. Cut on R3~R7 traces versus initial demoboard current

Initial Idd (ma)		Cut the trace/s connected to the resistor/s				
Min	Max	R3	R4	R5	R6	R7
250	259	X	X	X	X	X
260	269		X	X	X	X
270	279			X	X	X
280	289				X	X
290	299					X
300	309					

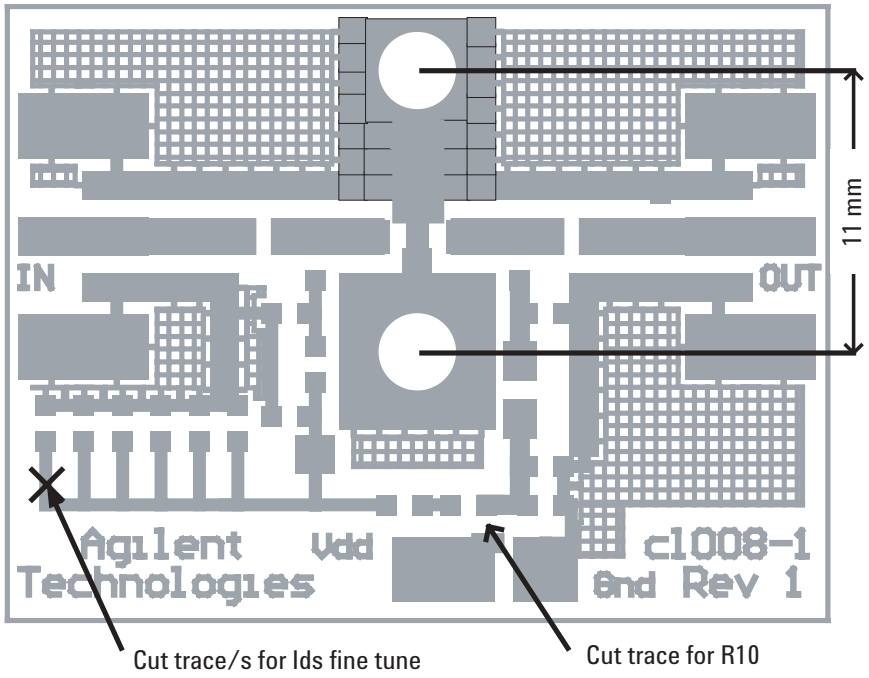


Figure 4. Positions of PCB trace cuts and distance between heatsink screws

Linear Simulation

A RF simulator like ADS allows the input and output tuning networks to be dimensioned with fewer "cut & try" iterations. In addition, critical parameters such as stability and gain can be predicted during the preliminary design stage. For example, if simulation forecasts a strong tendency to self-oscillation, the designer can pre-empt the problem by incorporating additional stabilization components into the preliminary circuit.

There is no need for preliminary characterization of the ATF-50189 as the Touchstone formatted "s2p" files at various DC biasing conditions and the ADS model can be downloaded from the Agilent Technologies website.

The correlation between simulation and measurement data hinges on how detailed the equivalent circuit is. To strike a reasonable compromise between circuit complexity and simulation accuracy, only the components' and PCB's most significant first-order parasitic are included. For example, when a ground return path consists of many via-holes in parallel, the resultant parasitic approximates ideal ground. So, the via-holes can be excluded from the simulated circuit without adversely affecting the accuracy.

The trajectories of the input match can be verified in a 'step-by-step' manner as shown in the figure 6. The curve marked as "1" represents the initial impedance at the position of the first matching component, C1. Subsequently, the addition of C1 moves the input-side impedance along the constant resistance circle to "2". The shunt capacitor, C2, shifts point "2" to the final position "3" near to the Smith chart centre whilst traveling along the constant admittance circle.

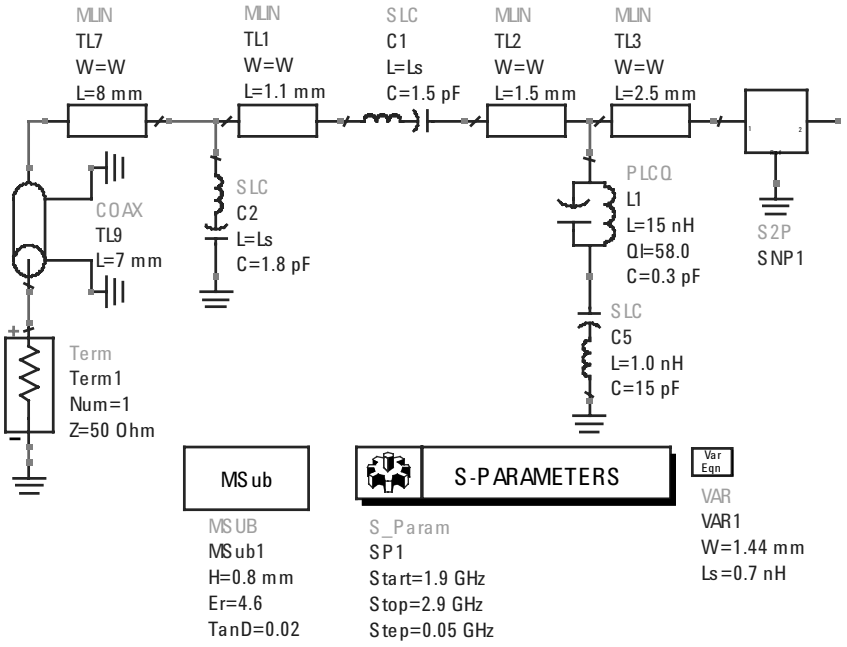


Figure 5. Input matching & biasing networks

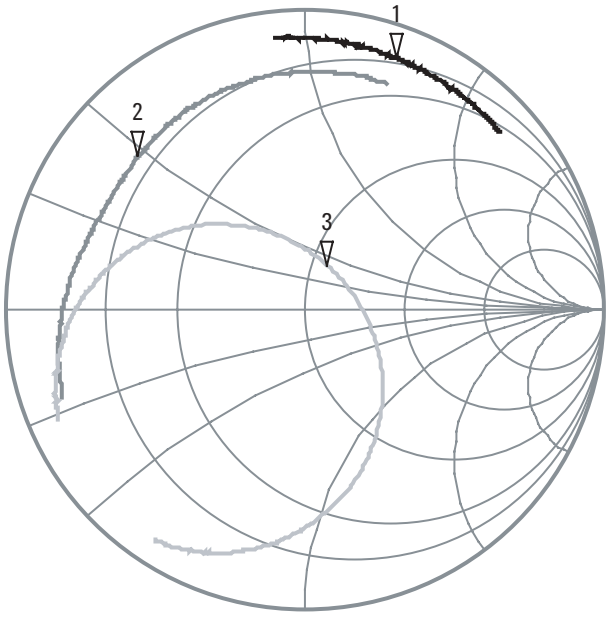


Figure 6. Measured trajectories of input impedance during the various phases of matching

Output:
C2~TL4 17 + j22

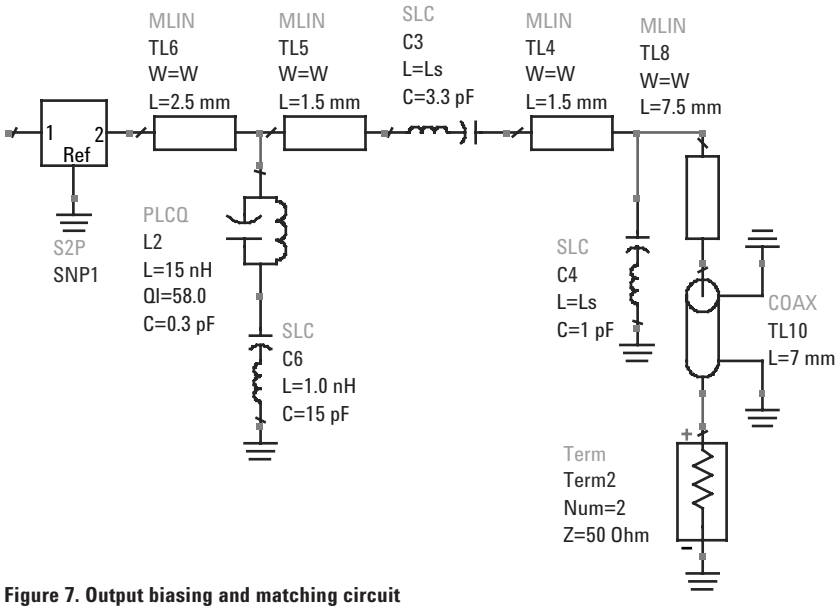


Figure 7. Output biasing and matching circuit

The trajectories of the output match are shown in figure 8. The curve marked as “1” represents the initial impedance at the position of the first output matching component, C3. Subsequently, the addition of C3 moves the trace along the constant resistance circle to “2”. The last matching component, C4 nudges the curve along the constant admittance circle to position “3” in the vicinity of the chart centre.

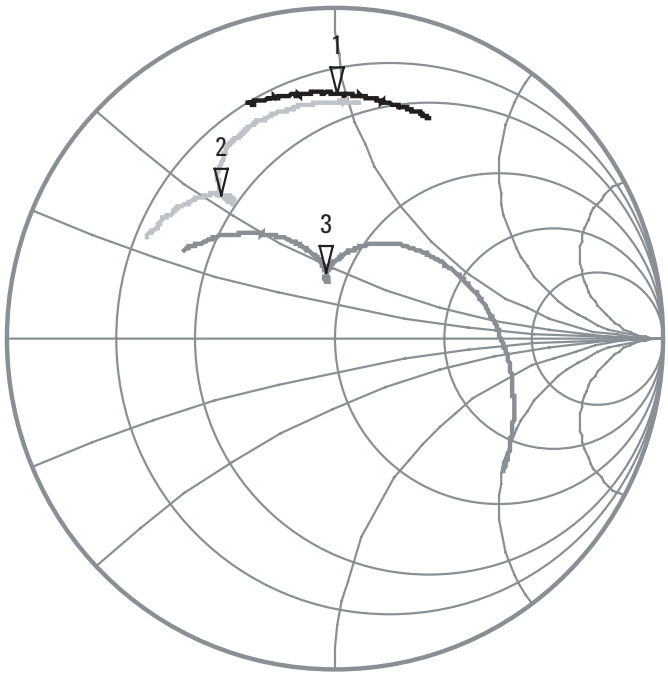


Figure 8. Measured trajectories of output impedance

Measured performance

The demoboard performance was measured under the following test conditions: - Vds = 4.5 V, Ids = 280 mA and f_c = 2.4 GHz.

The ATF-50189 is intended for either the driver amplifier, or the second-stage LNA slots, in transmit and receive chains, respectively. So, matching for minimum noise figure (NF) does not carry the same over-riding consideration as would have been in a first-stage LNA. However, good return loss over a broad bandwidth is required in these two slots. In line with this design goal, no attempt was made to tweak the input match for the lowest NF.

While satisfying the requirement for good input match, the NF can be improved, especially at higher microwave frequencies, by reducing the inevitable circuit losses. The low cost bias inductor at the input can be replaced with a higher Q component, e.g. air-cored spring wound inductor. The degradation in NF due to losses in the inductor can be estimated from: -

$$loss = 20\log\frac{Q_u - Q_l}{Q_u}$$

Additionally, some reduction in input-side loss may be obtained by changing the PCB material from FR4 to a lower loss substrate, such as Rogers RO4350.

The ATF-50189 demoboard amplifier exhibits good input and output return losses. This minimizes detuning effects when the amplifier is cascaded with other stages in the RF chain. For example, filters and aerials are especially susceptible to the adverse effects of reflective terminations. Designing the amplifier's input and output for a close match to 50Ω over the operating bandwidth, prevents unpredictable shift in the cascaded frequency response.

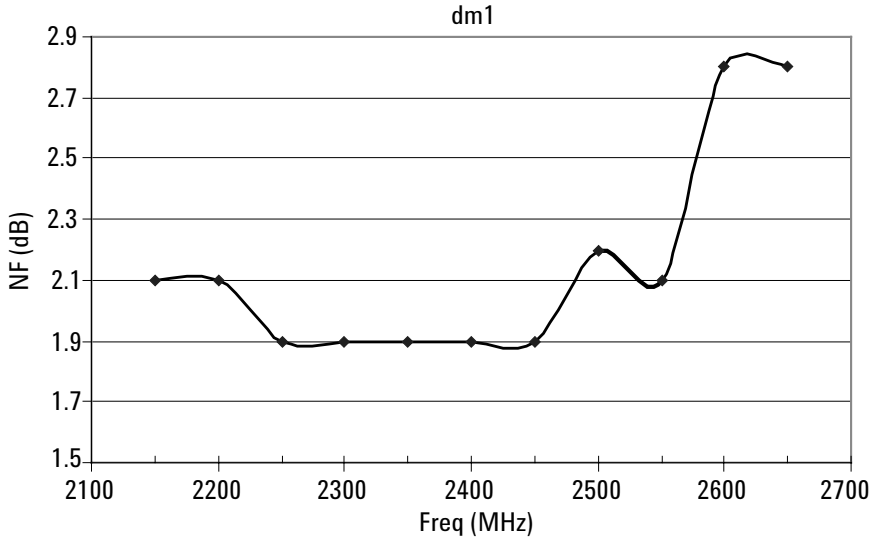


Figure 9. Measured NF

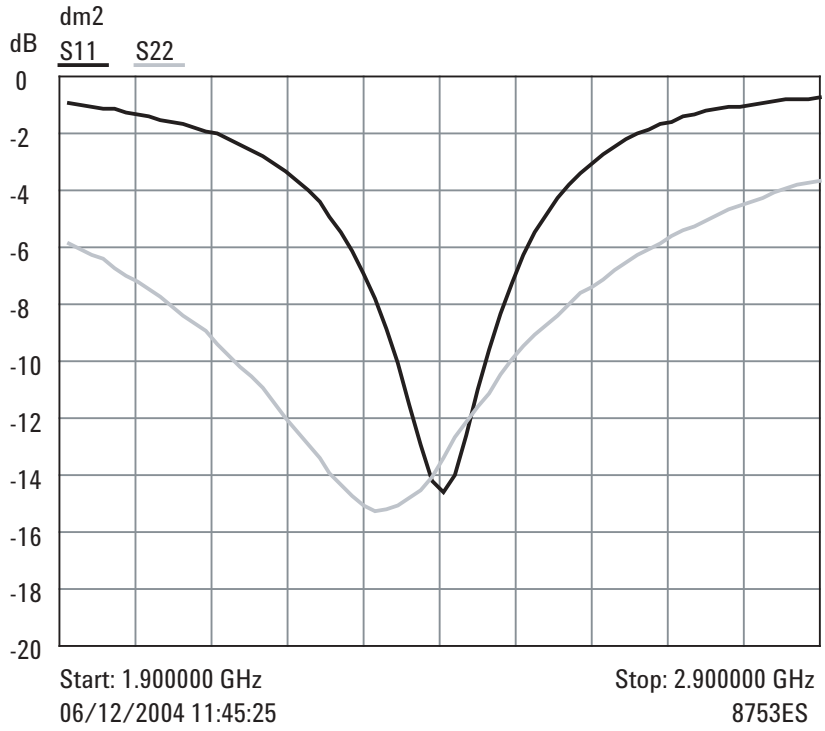


Figure 10. Measured input and output return loss

The gain was approximately 12.8 dB in the middle of the pass-band. Slightly more gain can be obtained at the expense of higher cost by using high Q inductors and/or a PCB substrate with lower loss.

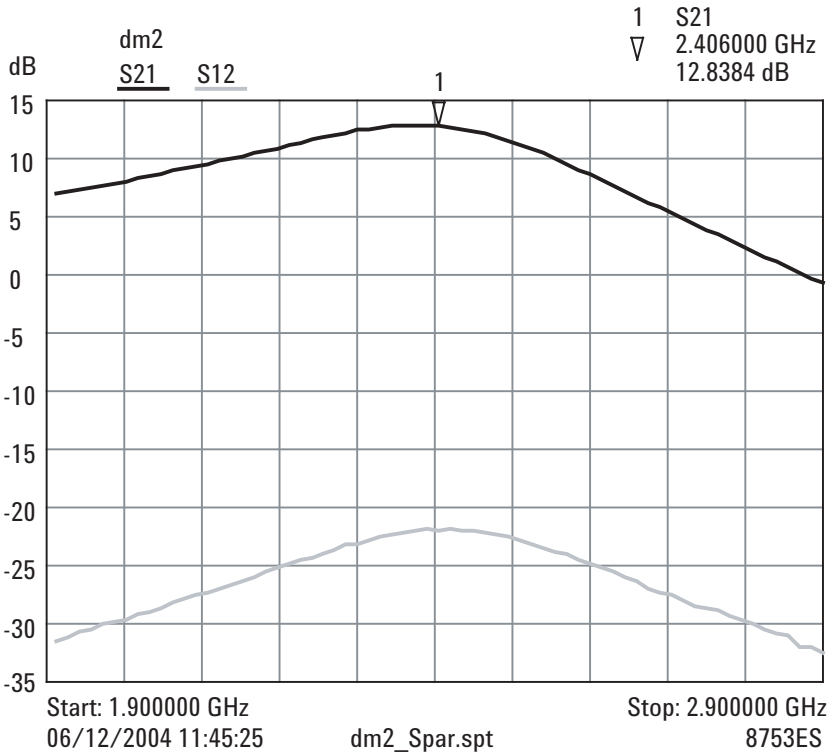


Figure 11. Measured forward gain and reverse isolation

The 1 dB gain compression point, P_{1dB}, indicates the upper limit of either the input or the output power level at which saturation has started to occur. Non-linear effects become increasingly prominent as the amplifier is driven to this limit. Linear modulation schemes require the power to be backed off several dBs from this limit. The P_{1dB} is measured by progressively increasing the input power while noting the point when the gain became compressed by 1 dB. P_{1dB} is customarily referred to the output. The demoboard nominal output P1dB is approximately 25dBm.

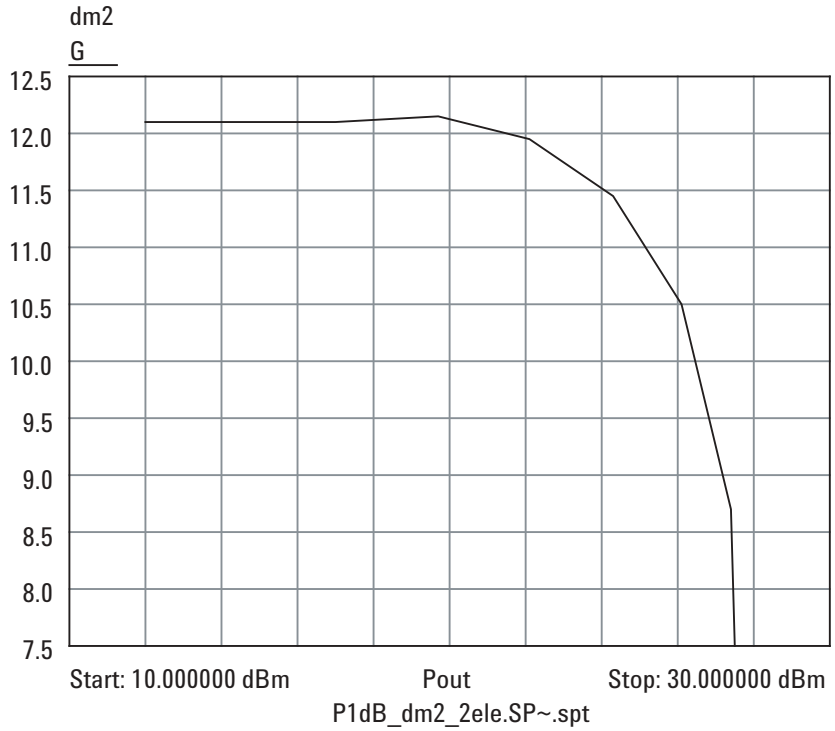


Figure 12. Measured gain vs. output power

The intercept point is another measure of amplifier linearity. The theoretical point when the fundamental signal and the third order intermodulation distortion are of equal amplitude is the third order intercept point, IP_3. The distortion level at other power levels can be conveniently calculated from the amplifier's IP_3 specification.

Two test signals spaced 5 MHz apart were used for evaluating the ATF-50189 demoboard. The large dynamic range between the fundamental tones and the intermodulation products meant that the latter is barely above the spectrum analyzer's noise floor. To measure the 3rd order product amplitude accurately, a very narrow sweep span can be used to improve the signal to noise ratio. As a tradeoff from the narrow sweep span, only one fundamental and one 3rd order intermodulation output signals can be practically displayed on the graph. Both the fundamental and intermodulation tones are overlaid over the same frequency axis for amplitude comparison purpose. The IP_3, referenced to the output, can be calculated from: -

$$IP_3 = P_{fund} + \frac{\Delta IM}{2}$$

where P_{fund} is the amplitude of either one of the fundamental outputs, and ΔIM is the amplitude difference between the fundamental tones and the intermodulation products.

The output intercept point, OIP_3, is approximately 45dBm.

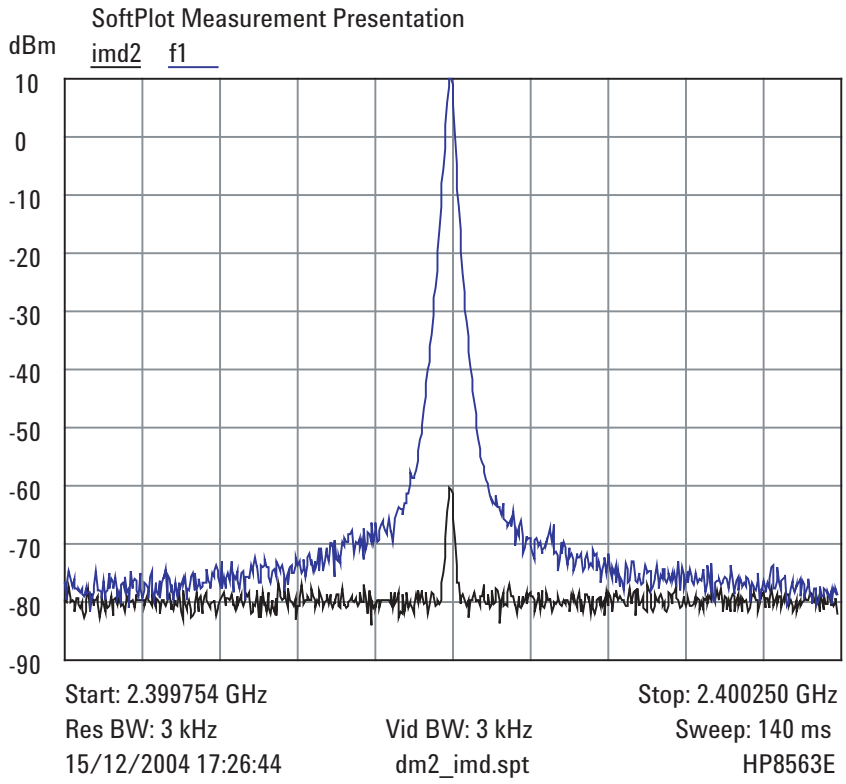


Figure 13. Overlay of fundamental tone and intermodulation product

Like all microwave transistors, the ATF-50189 demonstrates increasing gain corresponding with decreasing frequency. If this phenomenon is not tamed with the appropriate countermeasures, the amplifier can break into self-oscillation below its operating frequency - in the tens of MHz range. To assess the effectiveness of the low frequency circuit stabilization described previously, the Rollett stability criterion was calculated from the measurement of the demoboard's s-parameters. The ATF-50189 demoboard exhibits unconditional stability (k >1) over the range of frequencies that an 8753 network analyzer is capable of operating. This reduces the design effort required to adapt the ATF-50189 into the final product.

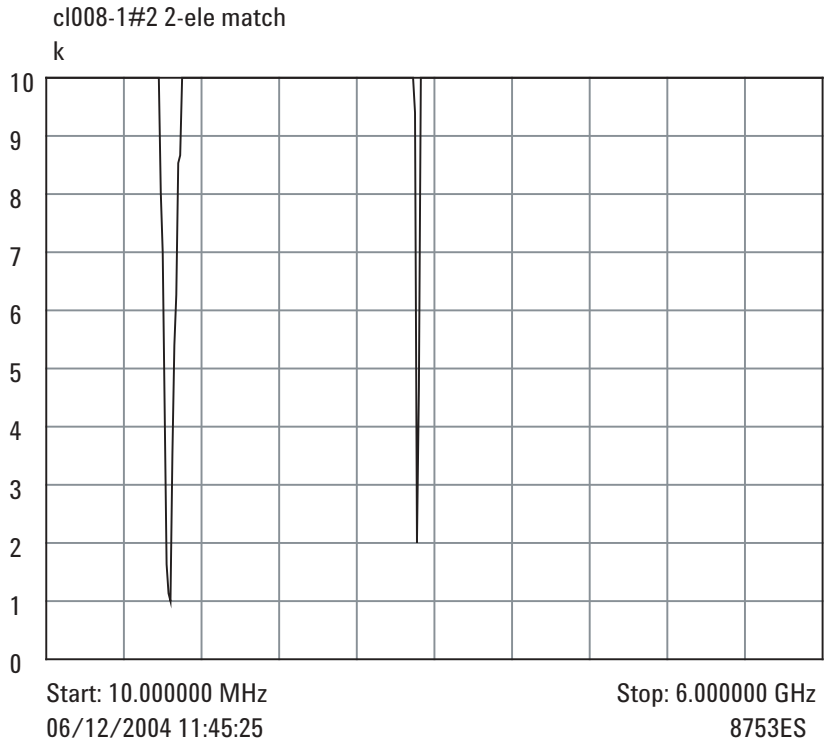


Figure 14. Stability (k) calculated from measured s-parameters

Inadvertent coupling between the amplifier's input and output and component parasitic can lead to instability in the upper microwave region. If there are pronounced gain peaks above its operating frequency, the amplifier may oscillate under certain operating conditions. In a wideband sweep test of the ATF-50189 demoboard up to 18 GHz, no abnormal peak was recorded in the frequency response.

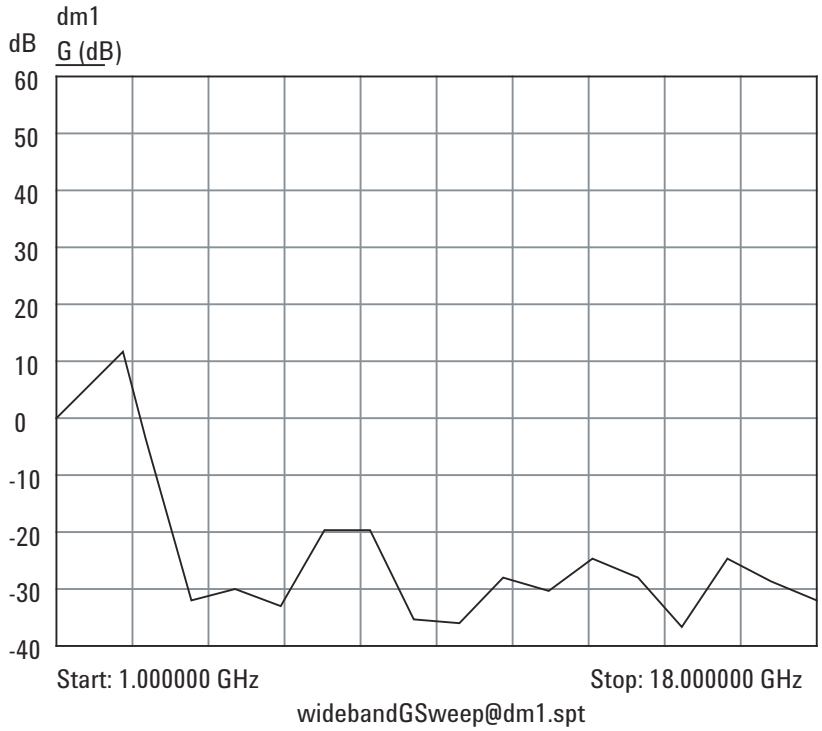


Figure 15. Wideband gain sweep

The nominal performance of the ATF 50189 demoboard is summarized below:

Table 1. Demoboard nominal performance values

Vsupply (V)	4.8
Isupply (mA)	320
Fc (MHz)	2400
G (dB)	12.8
RL in (dB)	< -12
RL in (dB)	< -12
k>	1
P1dB (dBm)	25
OIP3 (dBm)	45

Demoboard part list

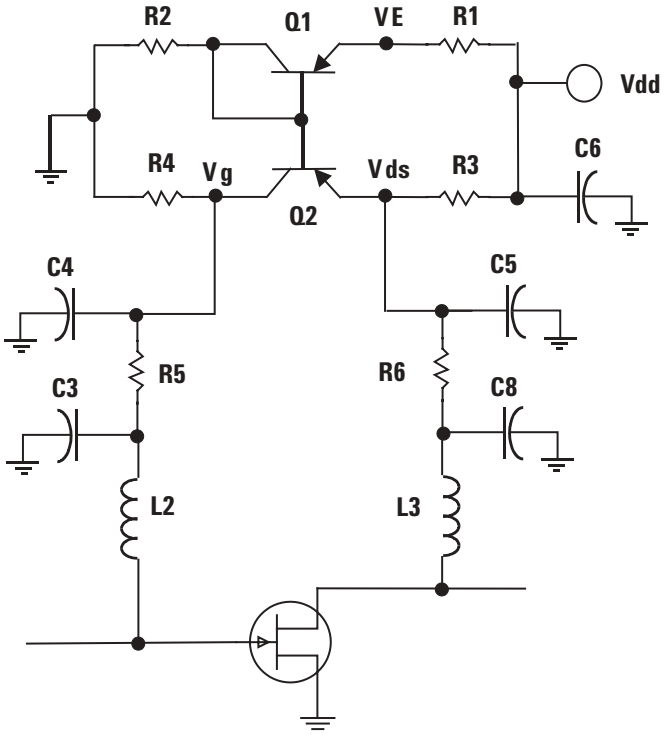
The demoboard's table of components is listed here. L3 is a ferrite bead inductor in surface mount package.

Table 2. List of components

Pos.	Value	Size	Description	Manfacturer
C1	1.5 pF	0603		Murata
C2	1.8 pF	0603		Murata
C3	3.3 pF	0603		Murata
C4	1.0 pF	0603		Murata
C5	15 pF	0603		Murata
C6	15 pF	0603		Murata
C7	10 nF	0603		Murata
C8	10 nF	0603		Murata
C9	2.2 uF	0603		Murata
J1	SMA conn.		0.8mm Pcb edge mount	
J2	SMA conn.		0.8mm Pcb edge mount	
J3	4 pin header		2.54mm spacing	
L1	15 nH	0603		Toko
L2	15 nH	0603		Toko
L3	60 R	0805	BLM21PG600SN1D	Murata
Q1	ATF-50189			Agilent
R1	10 R	0603		
R2	15 R	0603		
R3	1.5 k	0603		
R4	1.5 k	0603		
R5	1.5 k	0603		
R6	1.5 k	0603		
R7	1.5 k	0603		
R8	100 R	0603		
R9	12 R	0603		
R10	1 R	0603		

Active bias

Passive biasing was used in this application note for circuit simplicity and low component count. However, active biasing is imperative for the ATF-50189 amplifier in volume production. Active biasing confers the ability to hold the drain to source current constant over variations in both g_m and temperature. A very inexpensive method of accomplishing this is to use two PNP bipolar transistors arranged in a pseudo-current mirror configuration.



Due to resistors R1 and R3, this circuit is not acting as a true current mirror, but if the voltage drop across R1 and R3 is kept identical then it still displays some of the more useful characteristics of a current mirror. For example, transistor Q1 is configured with its base and collector tied together. This acts as a simple PN junction, which helps temperature compensate the Emitter-Base junction of Q2.

To calculate the values of R1, R2, R3, and R4 the following parameters must be know or chosen first:

I_{ds} is the device drain-to-source current;

I_R is the Reference current for active bias;

V_{dd} is the power supply voltage available;

V_{ds} is the device drain-to-source voltage;

V_g is the typical gate bias;

V_{be1} is the typical Base-Emitter turn on voltage for Q1 & Q2;

Therefore, resistor R3, which sets the desired device drain current, is calculated as follows:

$$R3 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{c2}}$$

where, I_{C2} is chosen for stability to be 10 times the typical gate current and also equal to the reference current I_R.

The next three equations are used to calculate the rest of the biasing resistors.

Note that the voltage drop across R1 must be set equal to the voltage drop across R3, but with a current of I_R.

$$R1 = \frac{V_{dd} - V_{ds}}{I_R} \qquad (5)$$

R2 sets the bias current through Q1.

$$R2 = \frac{V_{ds} - V_{be1}}{I_R} \qquad (6)$$

R4 sets the gate voltage for the FET.

$$R4 = \frac{V_g}{I_{C2}} \qquad (7)$$

Thus, by forcing the emitter voltage (V_E) of transistor Q1 equal to V_{ds}, this circuit regulates the drain current similar to a current mirror. As long as Q2 operates in the forward active mode, this hold true. In other words, the Collector-Base junction of Q2 must be kept reversed biased.

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