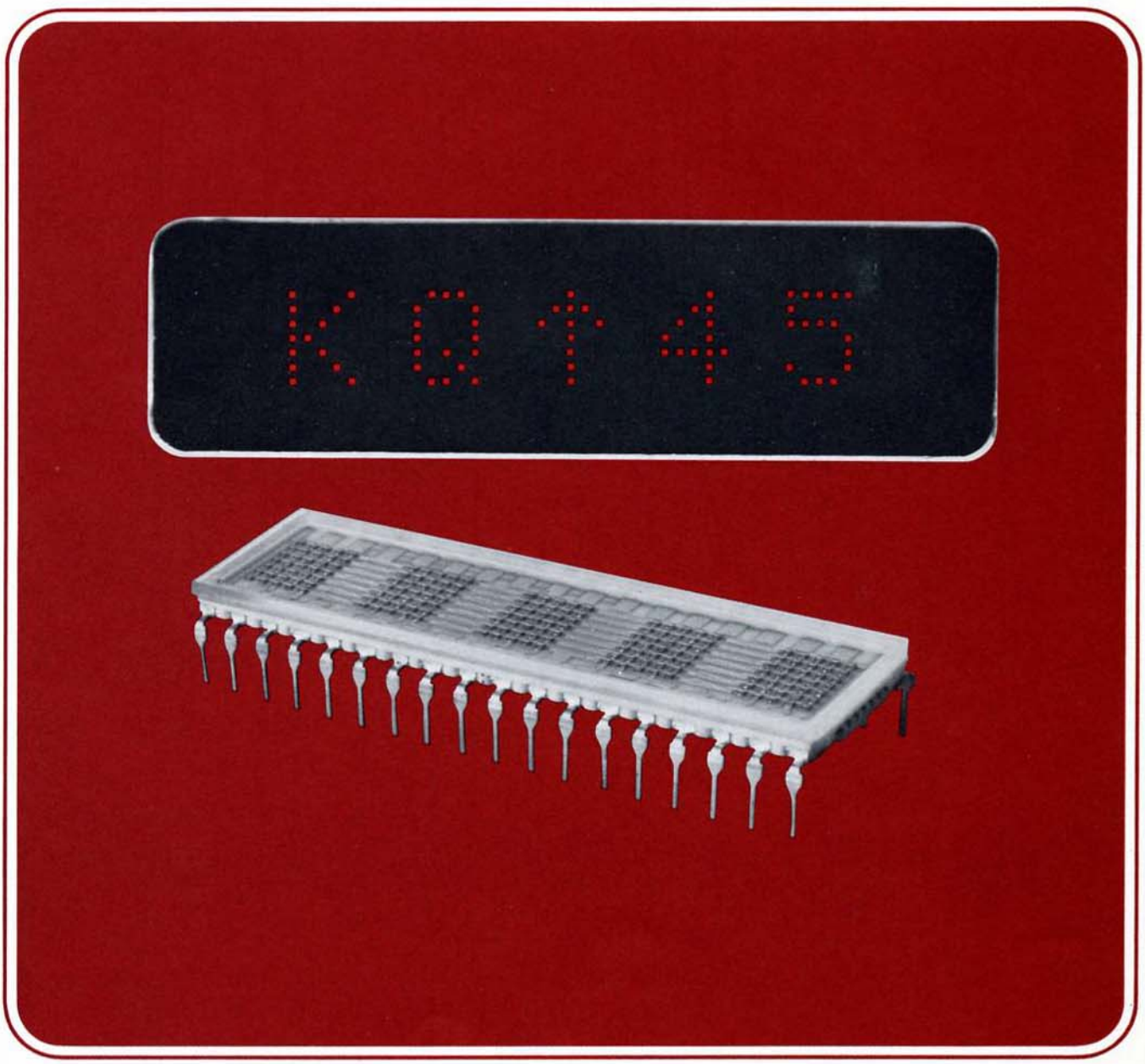
APPLICATION NOTE 931

SOLID STATE ALPHANUMERIC DISPLAY

DECODER/DRIVER CIRCUITRY



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Introduction

Hewlett Packard offers a series of solid state displays capable of producing multiple alphanumeric characters utilizing 5x7 dot arrays of GaAsP light emitting diodes (LED's). These 5x7 dot arrays exhibit clear, easily read characters. In addition, each array is X-Y addressable to allow for a simple addressing, decoding, and driving scheme between the display module and external logic.

There are three main advantages with the use of the X-Y addressable array:

1. X-Y addressing the 5 column to 7 row, 35 dot array utilizes the minimum number of pin connections.

2. X-Y addressing allows sharing of the read only memory (ROM) character generator and scanning elements over several characters for substantial cost savings.

3. X-Y addressing allows using circuit elements already available in system digital logic circuits such as clock/timing elements and buffer storage elements.

Methods of addressing, decoding and driving information to such an X-Y addressable matrix are covered in detail in his application note. The note starts with a general definition of the scanning or strobing technique used for this simplified addressing and then proceeds to describe horizontal and vertical strobing. Finally, a detailed circuit description is given for a practical vertical strobing application.

Description of Scanning Techniques

To form alphanumeric characters with an X-Y addressable array of light emitting diodes (LED's), a technique called "scanning" or "strobing" is utilized. This technique is basically timing-sharing of information across the rows or columns of the display, one row or column at a time. Information is addressed to the display by selecting one row (or column) of diodes at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all rows have been selected, in order, the cycle is repeated. By scanning all rows at least 100 times a second, briefly lighting the appropriate LED's, a flicker-free character composed of illuminated LED's is formed.

When information is scanned from row to row of the display (top to bottom) the mode is called **vertical** strobing. Information can also be scanned from column to column (left to right across the display) in the **horizontal** strobing mode. (See Figure 1.)

Figure 2 indicates how with **vertical** strobing the letters "HP" would be formed by sequentially selecting the rows and energizing the correct diodes in each column. When row I is selected only columns 1A, 1E and 2A, 2B, 2C, 2D

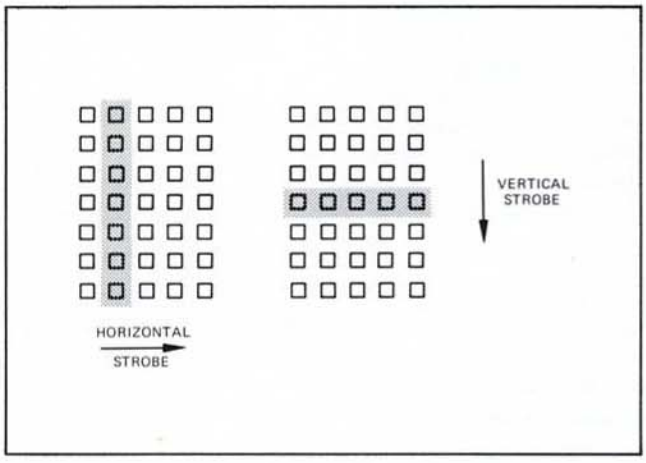


Figure 1.

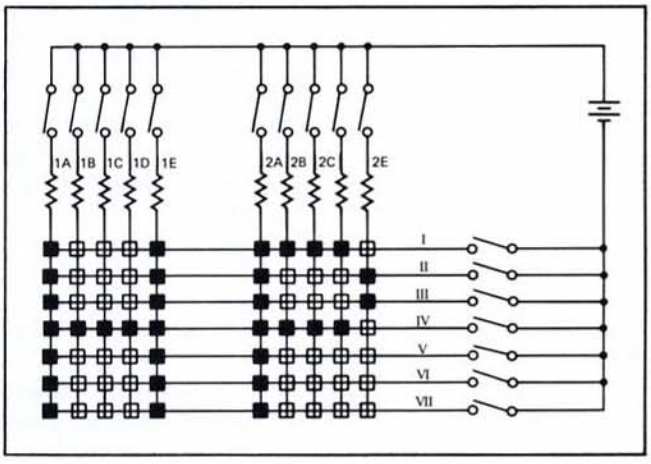


Figure 2.

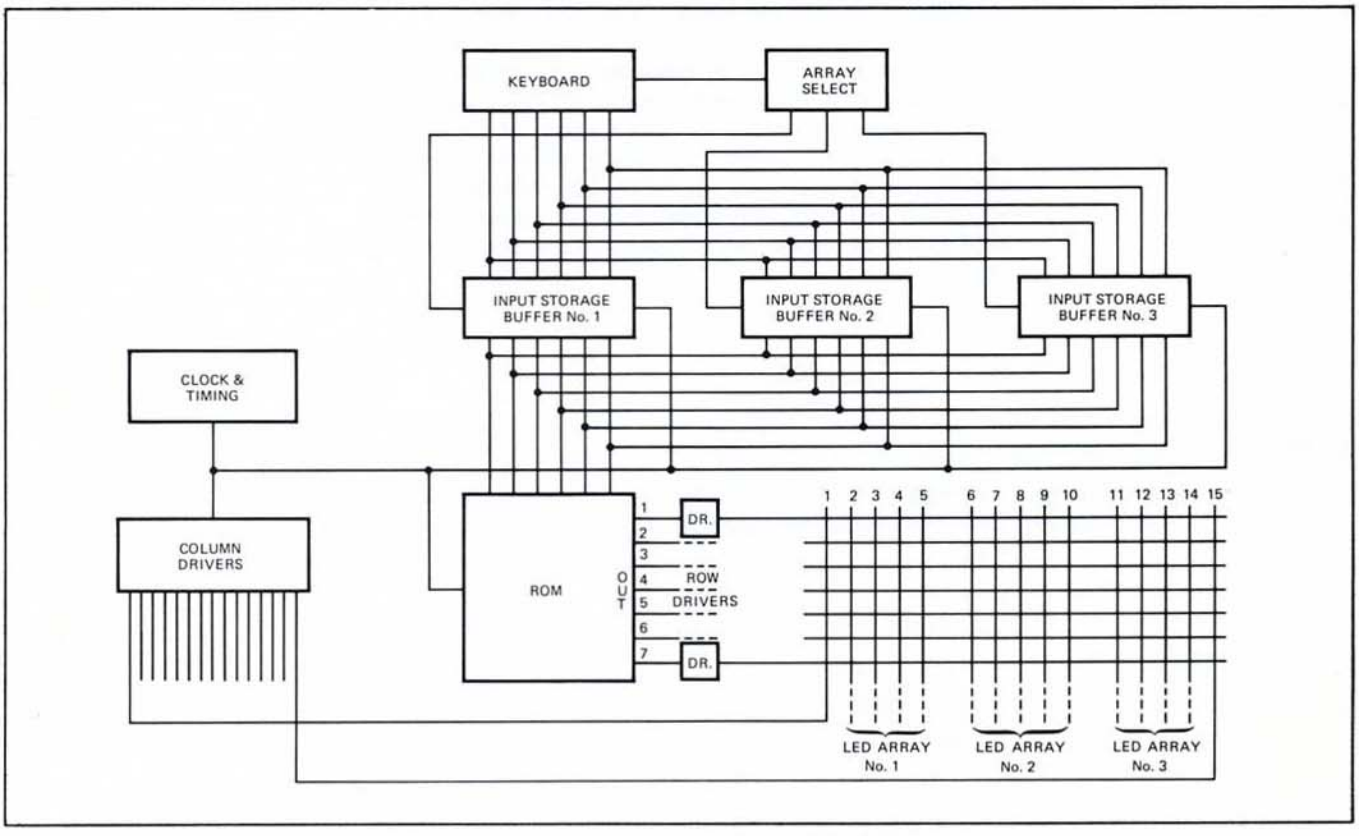


Figure 3. Horizontal Strobing Circuit Block Diagram

are energized. When selecting row II, columns 1A, 1E and 2A, 2E are energized and the process is continued as indicated by the solid squares.

To form the characters "HP" with **horizontal** strobing, the columns would be sequentially selected and the correct diodes in each row lighted. For example, when column 1A is selected, rows I, II, III, IV, V, VI, VII are energized. When selecting column 1B, row IV is energized and the process continues to form "HP", indicated by the solid squares.

Strobing Circuitry

The digital circuitry which performs the high speed sequential switching between rows (or columns) of diodes in strobing, can be classified in four major parts.

1. STORAGE BUFFERS: Flip-flops that store input or output digital information.

2. CLOCK/TIMING CIRCUITRY: A sequential pulse generator that times and keys the activity of all circuit components.

3. READ-ONLY-MEMORY: A character generator that accepts a binary coded input and furnishes a sequential 5x7 dot array information output.

4. ROW AND COLUMN DRIVERS: Current sources necessary to provide proper current drive levels to the LED's.

All of these circuit elements are commercially available in the form of IC's or discrete components.

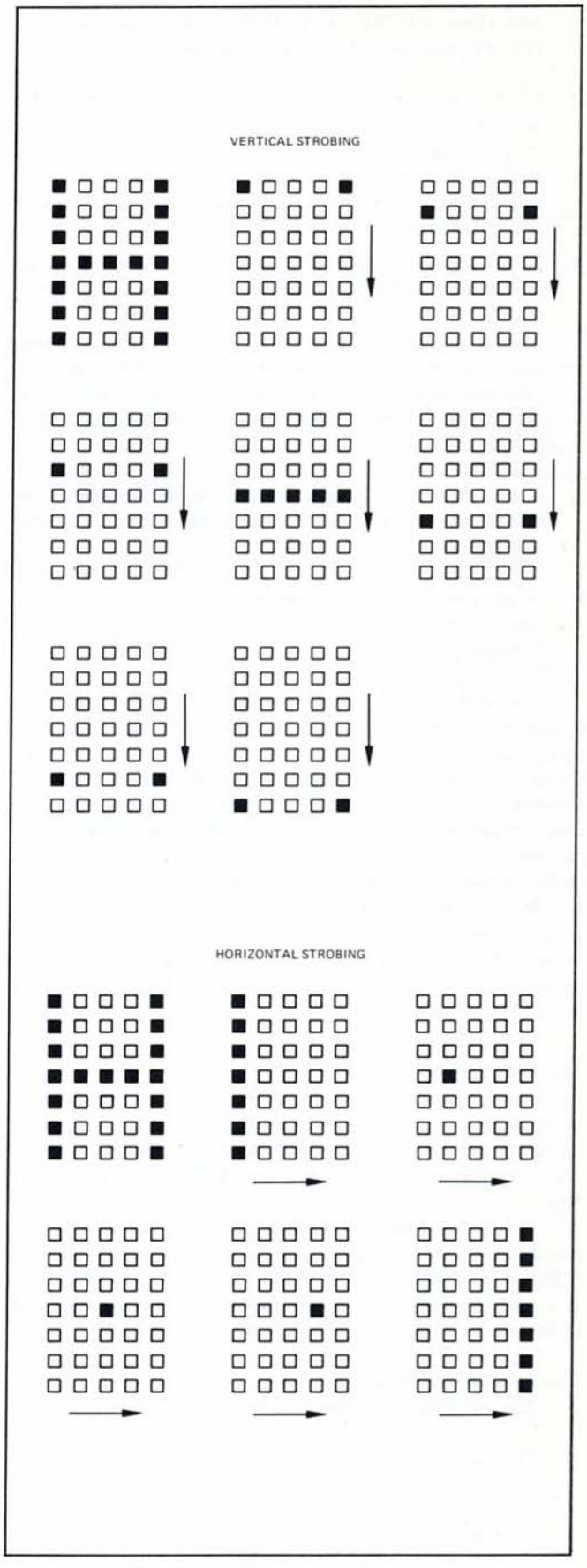
Horizontal Strobing

A simplified circuit diagram for horizontal strobing is shown in Figure 3. This particular technique describes three characters, however, operation of 1 — 4 characters is similar.

A. Coded, 6 bit, alphanumeric information is sequentially entered and stored in three, 6 bit, input storage buffers. The input information code in this example is a 6 bit (line) ASCII, but could be some other code if desired. Information is entered bit parallel, character serial to the appropriate input storage buffer. An array select line steers the information to the proper storage buffer.

B. Next, with the input information stored in the input buffers, timing circuitry enables the ROM and first input storage buffer so its stored 6 bit code is read into the ROM. (All other input storage buffers are disabled.)

C. The 6 bit input is decoded by the ROM and the first column of character information appears at the 7 line output of the ROM. The output signal is converted from a voltage to a current source by the row drivers. At the same time the output signal appears at the appropriate rows, the timing circuitry connects the



Vertical and Horizontal Strobing

first column of the first LED character to complete the current path and light the appropriate diodes.

D. Next, a timing pulse triggers the ROM to present the second column of character information at its 7 line output. Again, the signals are converted to current sources by the output drivers which light the appropriate diodes in the second column with connection of the second column drivers.

E. Repeating this sequence. The ROM cycles through the remaining third, fourth and fifth columns.

F. After tracing out the first character, the timing circuitry next enables input storage buffer #2 and information flows to the ROM which, in turn, sequentiallly presents the output character information to the second LED array.

G. Next the third input storage buffer character is decoded by the ROM and sequentially presented to the third LED array.

H. When this cycle is repeated at the rate of 100 times a second or faster, a flicker-free group of characters is formed.

The display duty cycle for each of the 15 vertical columns is about 6.6% and, therefore, the peak currents going into the diodes must be 15 times their average current. The high peak current demand is the reason for the discrete transistor driver stages on both the horizontal rows and vertical columns; about 75 mA peak in this example.

With horizontal strobing, the number of vertical columns that can be energized in one field of scan is limited by the peak current that any one diode can stand. Since the peak current limit of any one diode is about 100 mA and because the diodes require an average of 5 mA for 100 foot Lamberts, then about 20 columns could be run with the horizontal strobing technique.

Vertical Strobing

For applications requiring more than four characters, it is desirable to use the technique of vertical strobing. This mode is similar to horizontal strobing except that the scanning field moves vertically along the seven horizontal rows.

This vertical strobing technique has the advantage that more arrays may be added without affecting the display "ON" duty cycle of the light-emitting diodes. In general, it is a preferrential mode. A typical system is now described in detail.

Vertical Strobing Circuitry

The circuitry is divided into three main functions:

1. The clock and timing circuits,

2. The information handling storage buffers and read only memory (ROM),

3. The current limiting and driver stages.

1. Clock and Timing

In the block diagram of Figure 4, the control function occurs as follows: Data in ASCII code is entered and stored in a series of input storage buffers. The particular circuit described obtains the information from a keyboard which puts out ASCII code as well as an advance pulse. Only one of the input storage buffers is enabled to receive this code at a time. At the receipt of an advance pulse, the timing circuit enables the next input storage buffer.

Another portion of the timing circuit is concerned with getting the ASCII code from the input storage buffers to the character generating ROM, and in getting the character information into the output storage buffers. In the circuit shown, a binary counter and a 1/10 decoder provide the gating pulses for the storage buffers. If the number of arrays in the display is N_A, the binary counter's reset line is connected for counting to N_A (i.e., a mod N_A counter). The input storage buffer #1 is energized at its output at the same time that the output storage buffer #1 is energized at its input. Likewise, input storage buffer #2 and output storage buffer #2 are always operated together.

The total number of arrays that can be serviced by a single ROM is a function of the minimum field rate and line duty cycle, the ROM's access time (approximately 1 microsecond) and how fast the output storage buffers can be loaded (approximately 50 nanoseconds). With a field rate of 140 Hz and a 90% row duty cycle, up to 100 arrays could be serviced by one ROM. The field rate is well above the flicker rate that is visible to the eye. However, each application should consider if the display is subject to vibration during operation. Since the LED's are so fast in switching speed, — and have no persistance after the drive current is turned off, the eye will notice some character breakup if there is vibration of the display. This can be alleviated by speeding up the clock and corresponding field rate.

For a very large number of arrays, or a multi-line matrix of arrays, there may be better ways of partitioning the scan. For example, the ROM might be shared among different clusters of arrays with some additional switching. These circuits are intended primarily as examples and the particular application should determine how a given timing circuit or data handling circuit is designed.

2. Storage Buffers and ROM

The input storage function is one of the most flexible portions of the design. Information may come in a number of forms, including character serial or parallel ASCII code to each input buffer. The basic function however, is to present and store six or seven bit ASCII code in a series of input buffers.

The input storage buffers, as shown in the diagram, all have parallel outputs to the ROM. Thus, whenever the code in a given input buffer is gated out by a pulse from the timing circuitry, the buffer's ASCII information will be presented to the ROM's input.

In theory, the ROM could be used to decode all 35 bits of an ASCII coded character and store them in a read-write memory. However, the 35 bits per array would be relatively expensive so modified and less expensive approach is shown.

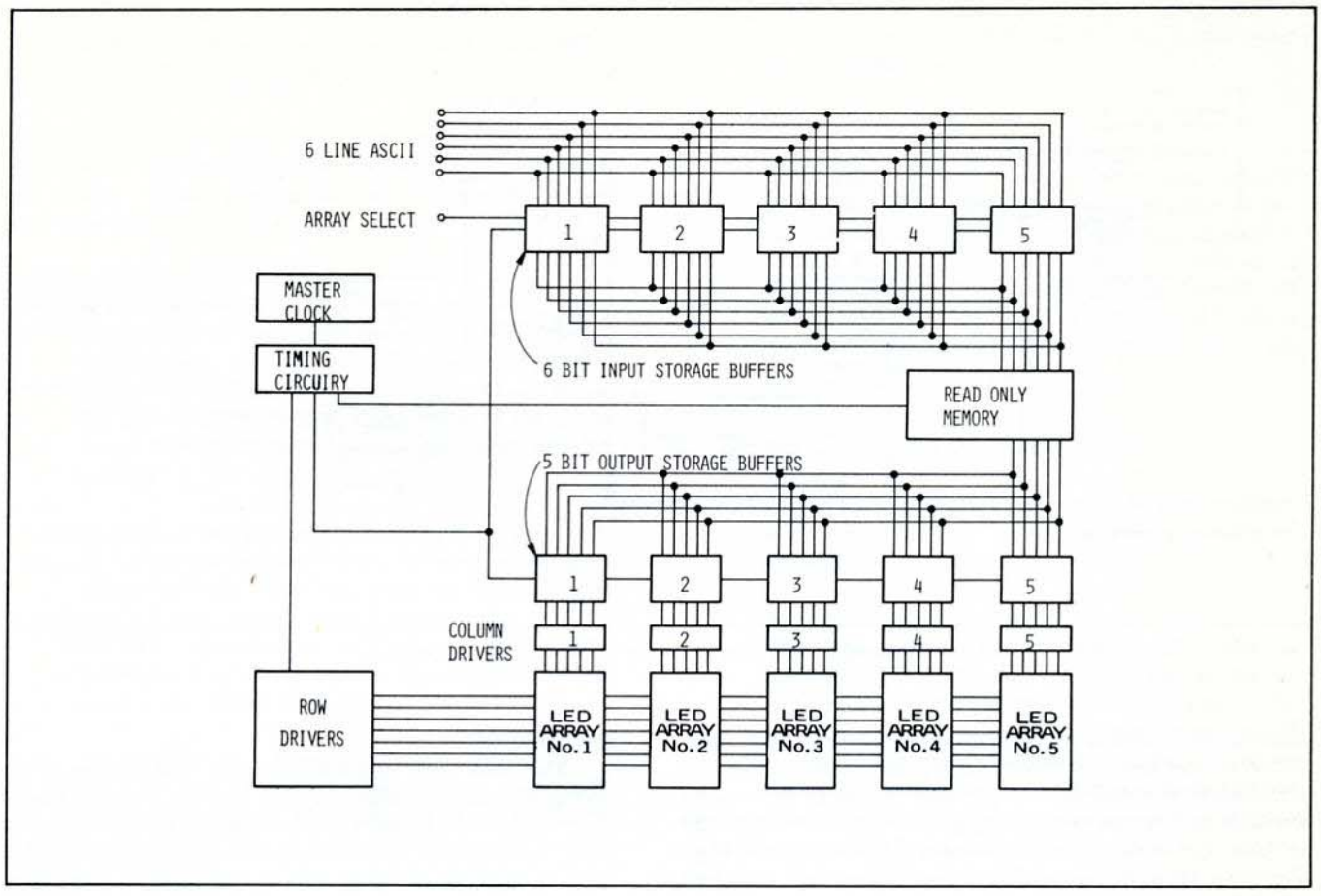


Figure 4. Vertical Strobing - Block Diagram

Assume that we are writing horizontal row number I, for all of the LED arrays. This means that for LED array #1, we need five bits stored in its output storage buffer which represent the five diodes in the top row of the character to be presented. The input storage buffer for LED array #1 is energized and applies its ASCII code to the ROM's input while the ROM is triggered to provide a five line output which represents the five bits of the top row of the character. Output storage buffer #1, corresponding to LED array #1, is then enabled to receive and store this five bit word. Next, ASCII information in input storage buffer #2 is fed to the ROM and a resulting five bit top row word is fed and enabled into output storage buffer #2. This sequence is continued for as many input storage buffers and output storage buffers as there are characters to be displayed.

3. Current Limiting and Driver Stages

After the output storage buffers are loaded with column drive information, the appropriate horizontal row is turned on to complete the current path. In this case, with the top row, row number I, the timing circuitry switches on the row I driver. This allows any light-emitting diode along the entire top row of the display to be energized wherever there is a vertical column driver turned on. Thus, if all the characters to be displayed were "T", the top row driver would enable all of those light-emitting diodes. At the same time, each of the output storage buffers would show that all five diodes on top of each array should be lit, and therefore, all five columns would be energized in every array.

Ignoring the relatively small load time, in vertical strobing the display cycle for seven line characters is 1/7 or approximately 14% of the total time on. In general, it is recommended that the strobing take place at as high a field rate as feasible. In this case, the circuitry shown represents a field rate of 125 Hz. Thus, the on-time for each row is 1150 microseconds, assuming the load time is negligible. After row number I is energized for one 1/7 of the total duty cycle, the timing circuitry directs the ROM to read the input storage buffers and to load the output storage buffers with the bits required to display row number II for each character. At that point, row number II is switched on by the row driver transistor which stays on for one 1/7 of the total duty cycle.

Because of duty cycle considerations, the diodes must be driven at relatively high peak currents, since they will only be on for one 1/7 of the time. For the vertical column drivers, the diode must be driven with a current that is seven times the average current so that the eye will average the light output. Assuming that an average current of five mA is adequate for approximately 100 fL light output, then the column drivers must handle 35 mA peak current. The drive circuitry, as shown in Figure 5 is arranged so that

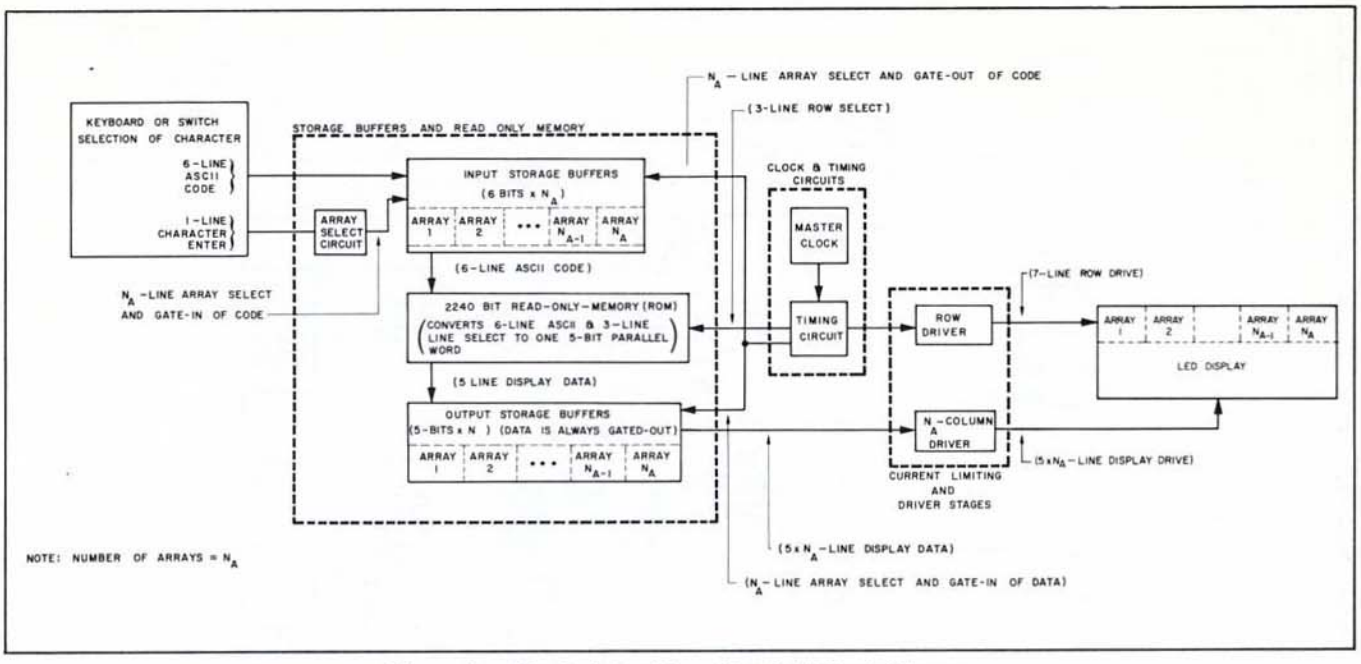


Figure 5. Vertical Strobing - Detailed Block Diagram

limiting is provided by the column driver stages. Two different methods of column drive are possible. Discrete transistors with the peak capabilities required are readily available and inexpensive. They generally cost less than 25¢ in large quantities. Also, a number of power gates (e.g., Motorola MC858) and multiple core drivers (e.g. Fairchild SH6502) will handle these currents.

Since the current limiting takes place primarily at series resistor in the vertical column drive, the large switch transistor which is used to enable the horizontal row only has to be an on-off type of switch. It would be impossible to current limit on the horizontal row because the circuit would not know how many diodes were to be turned on. The peak row current can be high, since it must switch drive currents to all the light-emitting diodes along its line. As an example, if the characters being displayed are "T"'s and there are 10 characters, then 50 diodes must be enabled. With a peak current of 35 mA for each diode and 50 diodes, over 1.7 amps switching current is needed. The row driver transistors, as noted on the materials list, are adequate for up through 10 arrays. If more arrays are needed, one can either use higher rated row drivers or divide the display into groups of arrays with each group having its own row driver stage. A buffer stage following the 9301 1/10 decoder may be needed to drive the additional loads.

Since LED efficiency increases with operating current, additional display efficiency is gained through strobing. It should also be noted that it's easy to adjust the display's intensity by changing the row duty cycle of the row drivers. The application is set up so that the on-time of the horizontal row switches can be varied. Thus, if the on-time for ach horizontal row were cut from 1150 microseconds to 575 microseconds, while the field rate is constant, intensity would be halved. This function is not shown on the circuit diagram.

System Interface

The area with greatest potential cost savings is the timing and drive circuitry. In the display circuitry shown, the timing is set up with commercially available circuits. In many applications, a substantial amount of timing and shift register clock phases may already be available and can be used as part of the strobing circuitry. As an example, if the character code is stored in existing shift registers, then a separate input storage buffer may not be needed. Instead, a set of character serial, bit parallel ASCII lines could be fed directly into the ROM with its own time sequence.

Pin Requirements

In the 5x7 dot array, each of the light-emitting diodes is mounted at the intersection of an X and a Y drive line. The display therefore acts much like a cathode ray tube with the X-Y input address determining which diode or set of diodes lights. Each array is a 5x7 matrix requiring five vertical column drive lines and seven horizontal row drive lines. Drive line economy is achieved by clustering arrays since all of the horizontal rows run in parallel. Thus, the total number of pin connections of such a package is 7 (for horizontal drive rows) plus $5N_A$ (for vertical drive columns), where N_A is the number of arrays in the display package. Within any package, the current per line should never exceed 2 amps.

Circuit Changes to Vertically Strobe Other Than 5 Arrays

The vertical strobing circuitry described previously was specifically designed for flexibility in strobing between four and ten arrays. For each additional array above five, the following components are needed:

3 SN7475N Quad Latch DIP's;

5, 33 ohm, 5%, 1/4 W resistors;

2, 2 K ohm, 5%, 1/4 W resistors;

1/4, MC3003P Quad 2-input OR Gate DIP;

1 3/4, MC858P Quad 2-input Power NAND Gate DIP's;

1 1/2, 9946 Quad 2-input NAND Gate DIP's.

Similarly, the drive circuitry for a four array display requires less components than for five arrays by the amount listed above. Actual component and wiring changes are described below:

A. Master Clock and Timing Circuits

1. 1/10 decoder that drives IG2- and ϕG-:
   For each additional array, one more output line of the decoder is utilized, requiring one more 2-input Power NAND Gate (1/4 – MC858P) and one more 2K ohm pull-up resistor. Connection of the additional NAND Gate is similar to those already present.

B. Storage Buffers and Read-Only-Memory

1. **Input Storage Buffers:**
   Since for each additional array one more 6-line ASCII coded character needs to be stored, 1 1/2 – SN7475N Quad Latch DIP's for output gating. Connection of gating lines is the same as for the other input storage buffers.

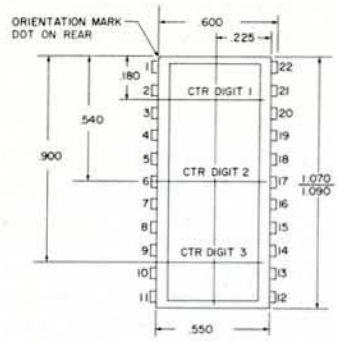
2. **Output Storage Buffers**
   As with the input storage buffers, for each additional array, 1 1/2 – SN7475N Quad Latch DIP's are needed for the output storage buffer. Gating connections follw those used in the other output storage buffers.

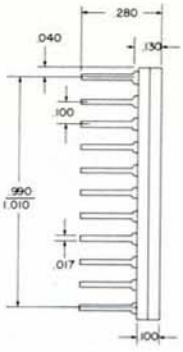
3. **Array Select Circuit:**
   Changes here are similar to those made for the 1/10 decoder in the clock and timing circuits block. For each additional array, one more output line of the decoder is utilized, along with another 2-input power NAND Gate (1/4 – MC858P) and 2 K ohm pull-up resistor, and another 2-input OR Gate (1/4 – MC3003P). The reset signal is taken from the N_A output line (except for $N_A = 10$, where the "9" line is used).

C. Current Limiting and Driver Stages

1. **Column Drivers**
   For every added array, five more 33 ohm resistors and 2-input Power NAND Gates (1 1/4 – MC858P) are required.

2. **Row Drivers**
   The drive current is a function of N_A ($I_C = (5)(35$ mA) (N_A)). The values of resistors R_1 and R_2 are dependent on this current, and therefore, on the number of arrays. However, the variance of optimum values is so small that the resistors can be kept the same for displays of between four and ten arrays.





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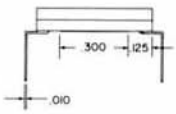
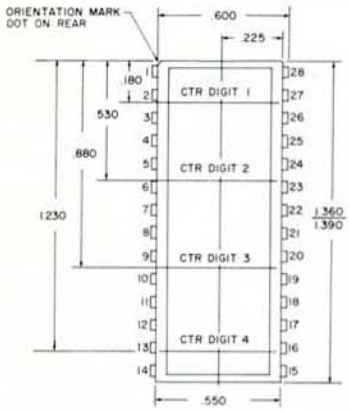
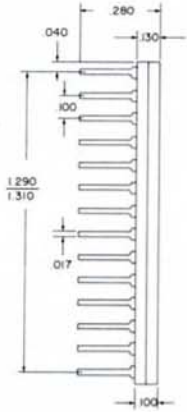


PIN NO.			PIN NO.	
1.	VII	(+)	12.	II (+)
2.	1C		13.	3D
3.	1D		14.	3B
4.	VI	(+)	15.	I (+)
5.	V	(+)	16.	2E
6.	2B		17.	2C
7.	2D		18.	2A
8.	III	(+)	19.	IV (+)
9.	3A		20.	1E
10.	3C		21.	1B
11.	3E		22.	1A





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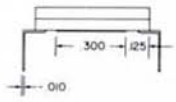
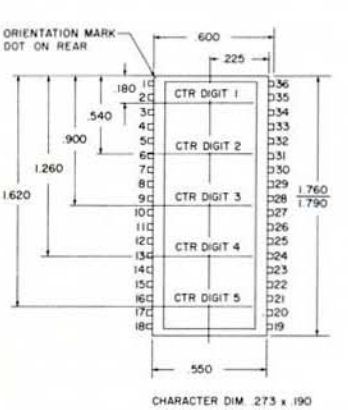
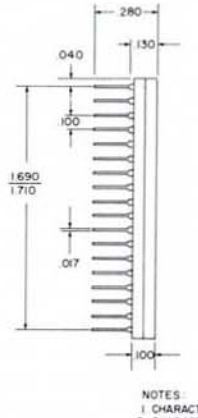


PIN NO.			PIN NO.	
1.	OPEN		15.	III (+)
2.	1C		16.	4C
3.	1E		17.	4A
4.	VII	(+)	18.	II (+)
5.	2B		19.	3E
6.	2D		20.	3B
7.	IV	(+)	21.	3A
8.	V	(+)	22.	2E
9.	3C		23.	2C
10.	3D		24.	2A
11.	VI	(+)	25.	I (+)
12.	4B		26.	1D
13.	4D		27.	1B
14.	4E		28.	1A



CHARACTER DIM. .273 x .190



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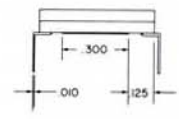
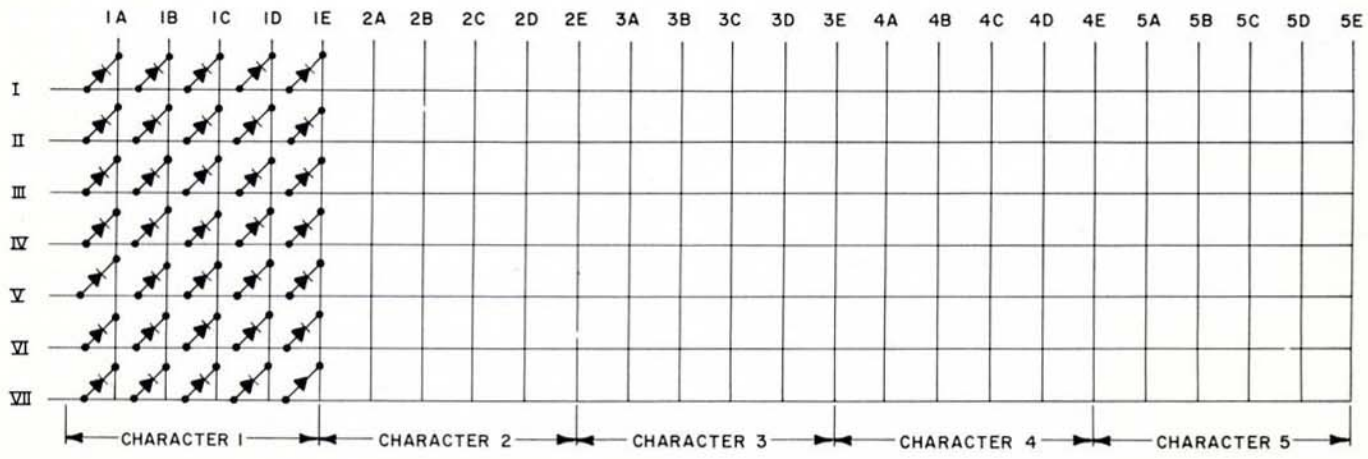


PIN NO.			PIN NO.	
1.	OPEN		19.	5E
2.	1C		20.	5C
3.	1E		21.	5A
4.	VI	(+)	22.	IV (+)
5.	2B		23.	4E
6.	2D		24.	4C
7.	2E		25.	OPEN
8.	V	(+)	26.	III (+)
9.	3C		27.	3D
10.	3E		28.	3B
11.	VII	(+)	29.	3A
12.	4A		30.	II (+)
13.	4B		31.	2C
14.	4D		32.	2A
15.	OPEN		33.	I (+)
16.	5B		34.	1D
17.	5D		35.	1B
18.	OPEN		36.	1A

NOTES:
1. CHARACTER COLUMNS ARE DESIGNATED A THROUGH E
2. CHARACTER ROWS ARE DESIGNATED I – VII



5082-7100 / 7101 / 7102 SCHEMATIC WIRING DIAGRAM

GLOSSARY

1. **ARRAY**: A 5x7 matrix of LED's from which the characters are formed by selective illumination.

2. **ASCII CODE**: A Standard binary code used to represent common symbols and alphanumeric characters. The 6-line version is obtained by dropping the most significant bit from 7-line ASCII. (American Standard Code for Information Interface.)

3. **CHARACTER**: The information or font that is perceived by the observer.

4. **COLUMN**: The vertical string of LED's in an array.

5. **DISPLAY DUTY CYCLE**: Of the time that it takes to cycle through all rows (columns), the percent that one row (column) driver is enabled. In vertical strobing, the Display Duty Cycle = (1/7) (Row Duty Cycle).

6. **FIELD RATE**: The refresh rate of the whole display.

7. **HORIZONTAL STROBING**: A display technique where the information to be displayed is addressed to the arrays by selecting one column of diodes at a time, energizing the appropriate diodes in that column and then proceeding to the next column. After all columns have been selected one at a time, the process is repeated.

8. **LED**: Light Emitting Diode; a diode that emits visible light.

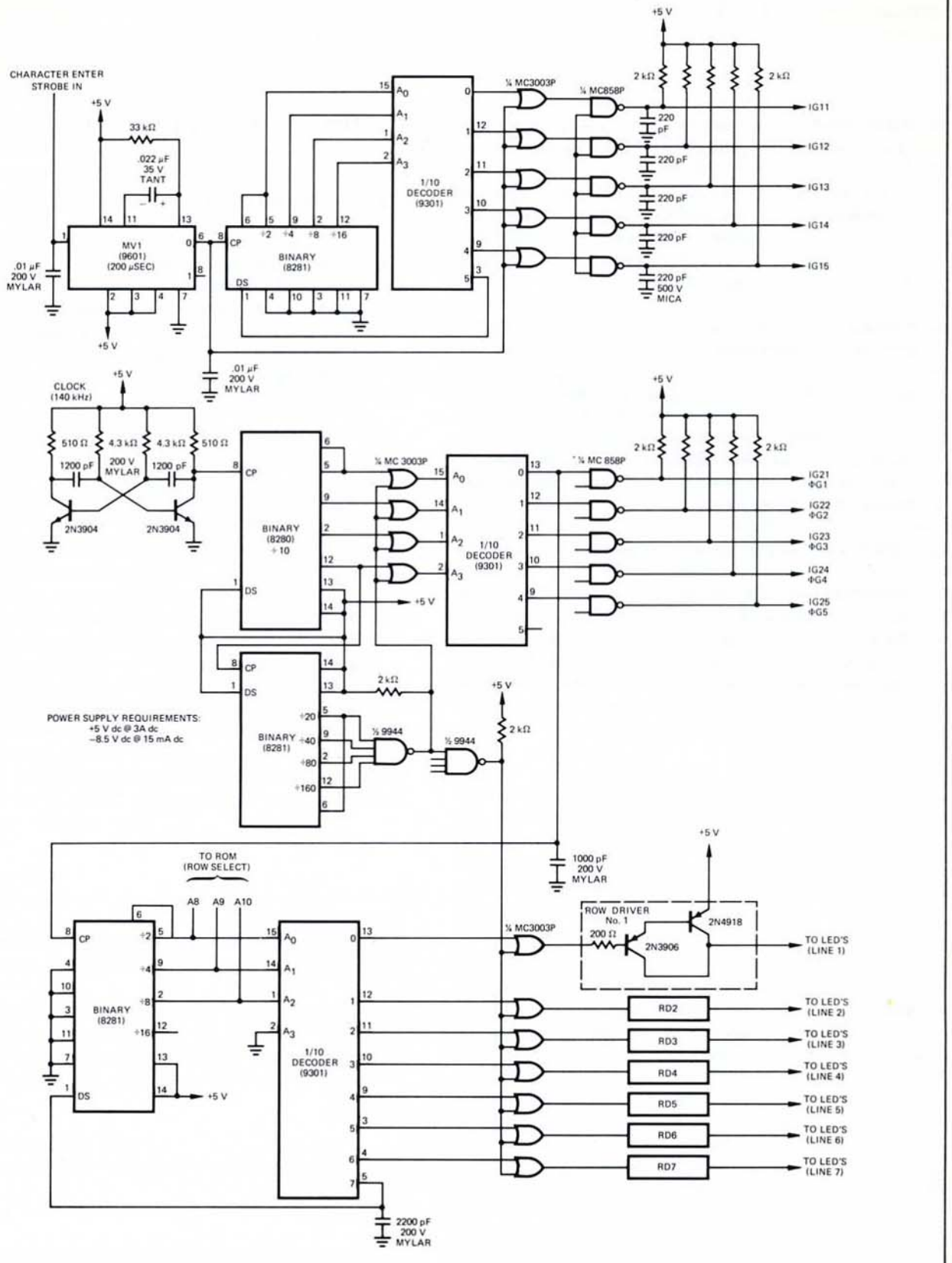
9. N_A: The number of arrays in a display.

10. **ROM**: Read Only Memory; an electronic "reference table" of fixed information, where the input determines what data we "look up". The ROM used here provides the 5x7 (35 points) character font data for any one of 64 different alphanumeric characters and symbols. (2240 bits.)

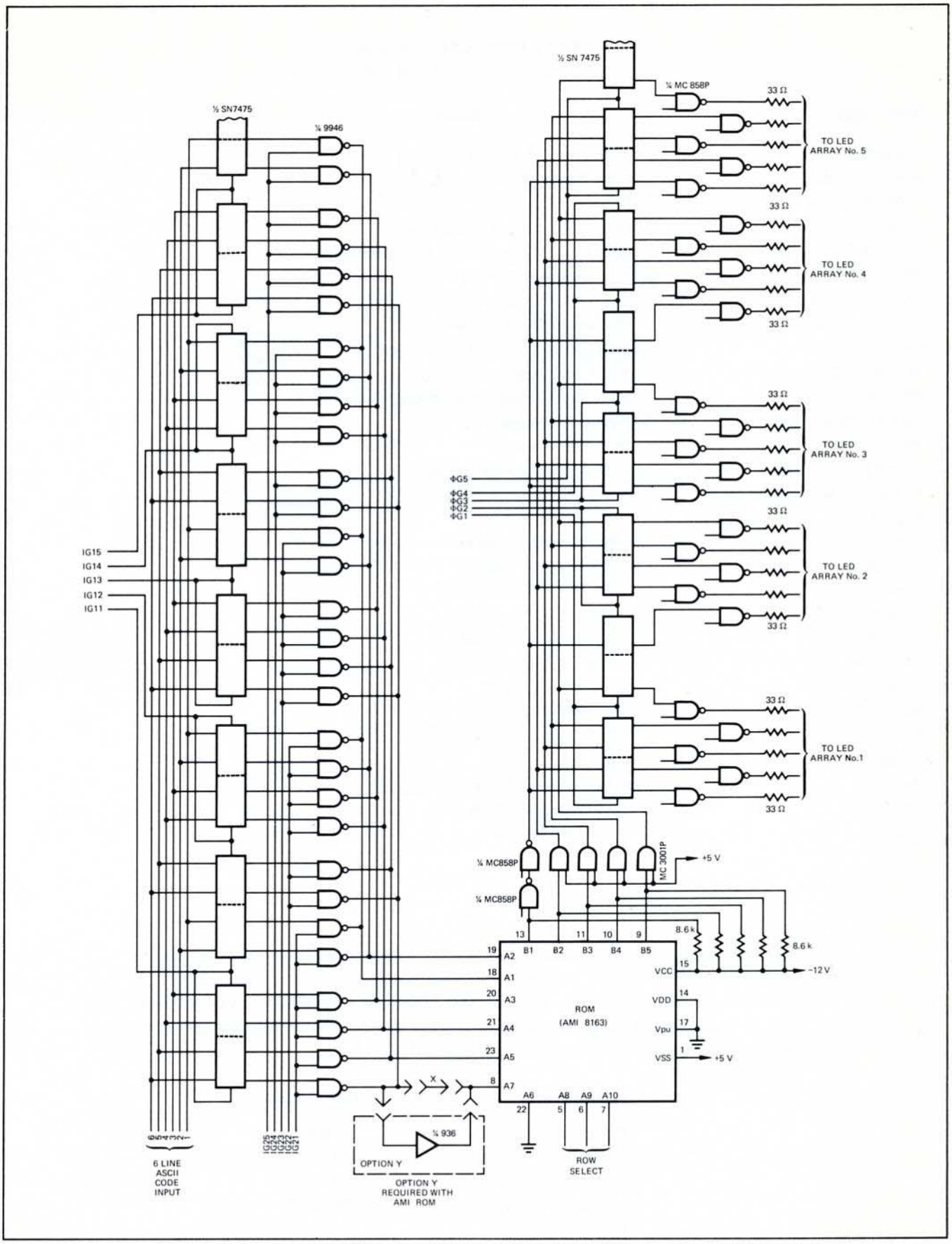
11. **ROW**: The horizontal string of LED's in an array.

12. **ROW DISPLAY DUTY CYCLE**: Of the total time spent loading and displaying a row of information in vertical strobing, the percent (of time) that we display the information.

13. **VERTICAL STROBING**: A display technique where the information to be displayed is addressed to the arrays by selecting one row of all arrays at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all seven rows have been elected one at a time, the process is repeated.



P/O 5 Character Vertical Strobing Schematic Diagram



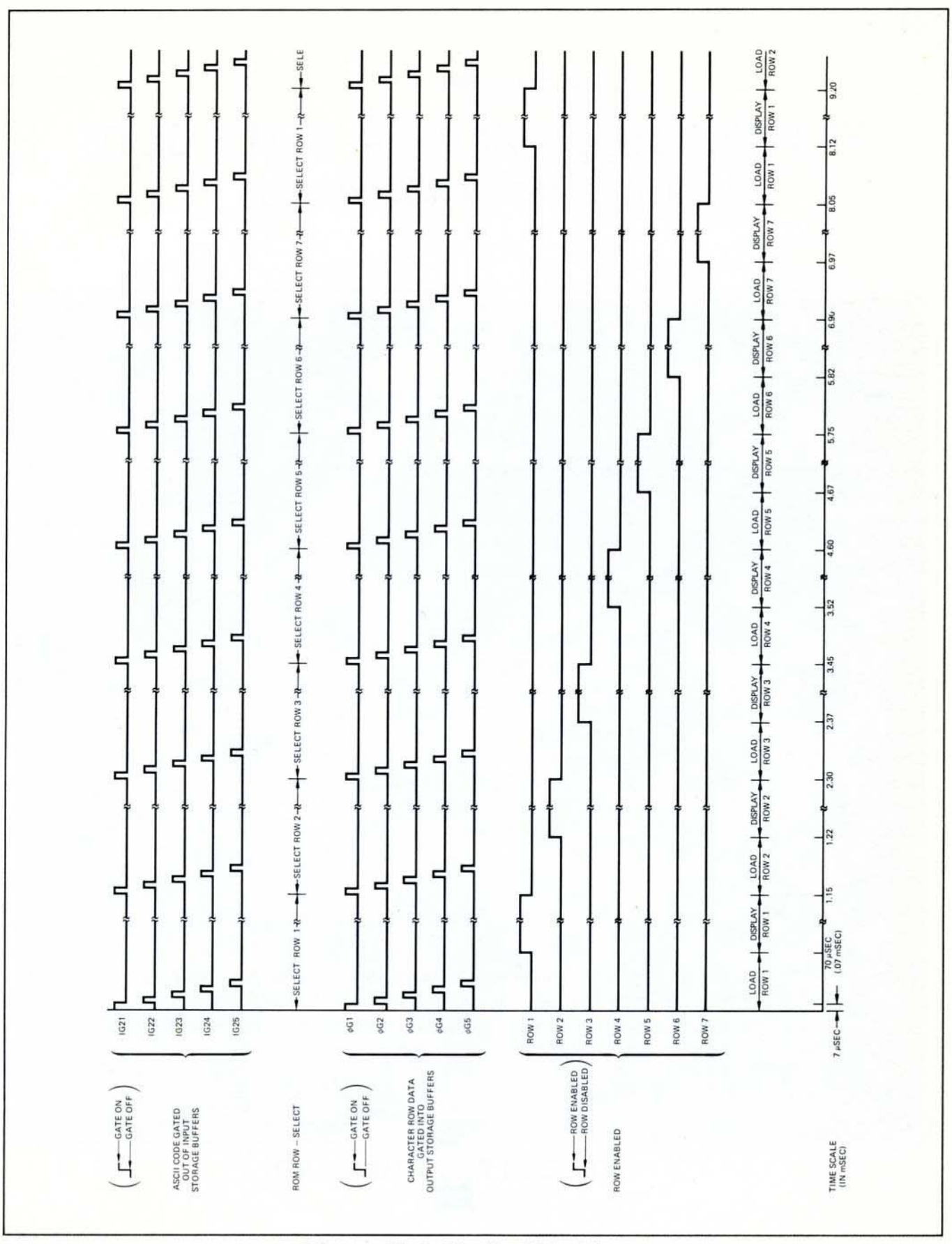
P/O 5 Character Vertical Strobing Schematic Diagram

5 ARRAY VERTICAL STROBED DRIVE CIRCUIT – PARTS LIST

Item (Mfg.)	Description	Quantity
8280 (Signetics)	4-Bit Decade Counter	1
8281 (Signetics)	4-Bit Binary Counter	3
9301 (Fairchild)	T^2L 1/10 Decoder	3
9946 (Fairchild)	DTL Quad 2-input NAND Gates	8
MC858P (Motorola)	DTL Quad 2-input Power NAND Gates	10
MC3003P (Motorola)	T^2L Quad 2-input OR Gates	4
SN7475N (Motorola)	T^2L Quad Latch	16
9601 (Fairchild)	Monostable Multivibrator	1
S8163 (AMI) *	2240-Bit ROM with 5 line output	1
MC3001P (Motorola)	T^2L Quad 2-input AND Gates	1
9944 (Fairchild)	DTL Dual 4-input Power NAND Gates	1
2N3904 (Motorola)	NPN Si Transistor	2
2N3906 (Motorola)	PNP Si Transistor	7
2N4918 (Motorola)	PNP Medium Power Transistor	7
36 pin DIP socket (Cambion)	Socket #703-3791-01-04-16	1
Capacitor	220 pF, 500 V, mica	5
Capacitor	1000 pF, 200 V, mylar	1
Capacitor	1200 pF, 200 V, mylar	2
Capacitor	2200 pF, 220 V, mylar	1
Capacitor	0.022 μF, 35 V, tantalum	1
Capacitor	0.01 μF, 200 V, mylar	2
Capacitor	150 μF, 15 V, tantalum	3
Resistor	33 Ω, 5%, C, 1/4 W	25
Resistor	200 Ω, 5%, C, 1/4 W	7
Resistor	510 Ω, 5%, C, 1/4 W	2
Resistor	2 kΩ, 5%, C, 1/4 W	12
Resistor	4.3 kΩ, 5%, C, 1/4 W	2
Resistor	8.6 kΩ, 5%, C, 1/4 W	5
Resistor	33 kΩ, 5%, C, 1/4 W	1

* The following list illustrates additional 2240 bit character generators which are suitable for vertically strobing 5 x 7 alphanumeric displays. However, since these ROM's are not necessarily PIN replaceable with the AMI S8163 and may require a V_{SS} of greater than 5 v and 2 phase clocks, some minor redesign will be necessary to make the units compatible with the circuit illustrated on pages 10 and 11.

Manufacturer	Part Number
Electronic Arrays	EA 3501
Fairchild	3257
Central Instruments	RO-1-22-40
Mostek	MK2100P
National	5240
Texas Instruments	2400



5 Character Vertical Strobing Timing Diagram

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