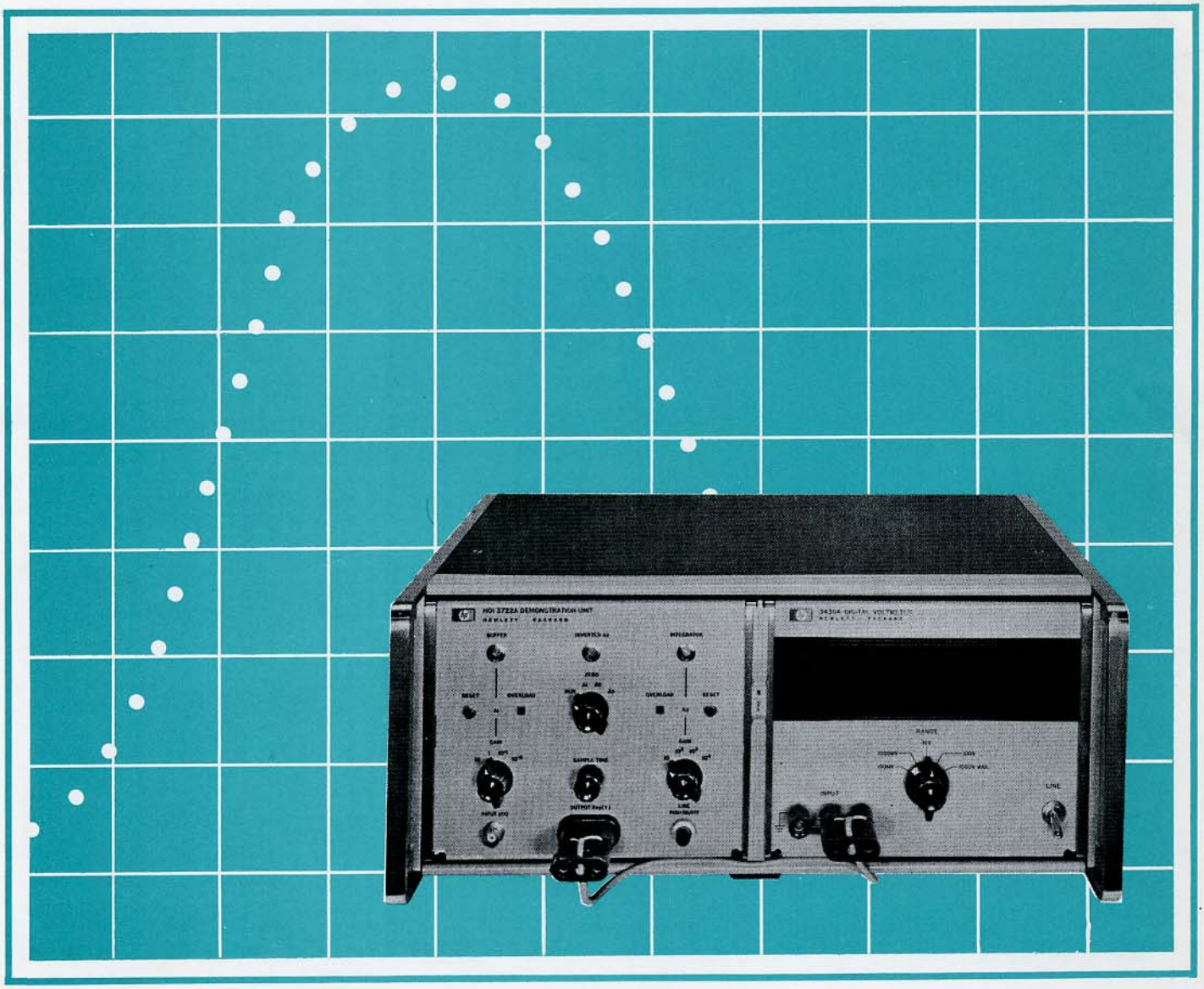
APPLICATION NOTE 98-2

Noise at Work

A point by point correlator for the H01–3722A



HEWLETT hp PACKARD

APPLICATION NOTE 98-2

A point by point correlator for the H01–3722A

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SOUTH QUEENSFERRY, WEST LOTHIAN, SCOTLAND.

PRINTED AUGUST 1969

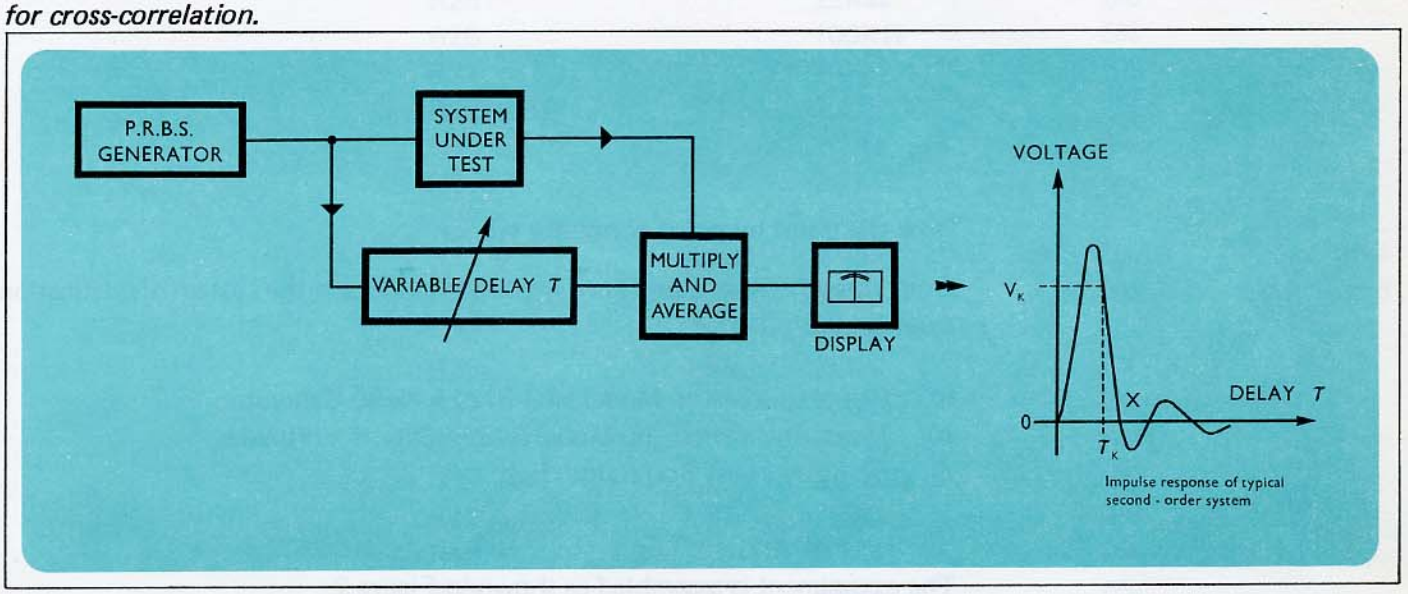
Introduction

Finding the transfer function of a system, or system identification, using pseudo-random binary sequences (p.r.b.s.) has recently gained popularity primarily because instruments which generate such sequences are becoming increasingly available. The Hewlett-Packard Model H01-3722A Noise Generator is such an instrument; its specification is outlined in Appendix A.

The use of pseudo-random binary sequences in system identification is now an established and well documented technique. [1,2]

Briefly, an approximation to the impulse response of a linear system may be determined by applying to the system input a suitable p.r.b.s., and cross-correlating a delayed version of the p.r.b.s. with the system output signal. Cross-correlation involves continuous multiplication of the two signals, and averaging (integrating) the product over a fixed interval of time. The multiplication and averaging process is repeated with various delays between input and output signals, and the averaged products are then plotted against delay time to give an amplitude/time curve corresponding closely to the impulse response of the system under test. Figure 1 illustrates the basic experimental arrangement.

Figure 1. Basic arrangement for cross-correlation.



The ideal technique

The use of noise to obtain the impulse response overcomes the main disadvantage of conventional impulse testing, namely the tendency of impulse-type test signals to overload all but the simplest passive systems. If the impulse-type test signal is made small enough to avoid overload, the output from the system can become buried in noise, and hence not detectable. The noise test signal, however, can be applied at a very low level, resulting in almost no system disturbance and very small perturbations at the output. Cross-correlation, which is essentially a process of accumulation, builds up the result (that is, the product of output and delayed input) over a long period of time. Hence, although the perturbations may be very small, a measurable result can be obtained provided that the integration time is selected with care.

A significant advantage of the noise/cross-correlation technique is that the test signal can, in many cases, be applied while the system is on line . . . the low-level noise is mixed with the main input signal to the system, and the impulse response is extracted from the main signal plus noise-induced ripple at the output. This technique is particularly useful in the analysis of process control and other systems having long time constants.

The contents of this application note describes, in detail, a point by point correlator which enables p.r.b.s. system identification measurements to be carried out using the hp Model H01-3722A Noise Generator.

How the point by point correlator works

Only three hardware units are required to perform the system identification experiment:-

a) Signal source - hp Model H01-3722A Noise Generator
b) Measuring device - hp Model 3430A Digital Voltmeter
c) Point by Point Correlator Unit

The experiment is assembled as shown in Figure 2.

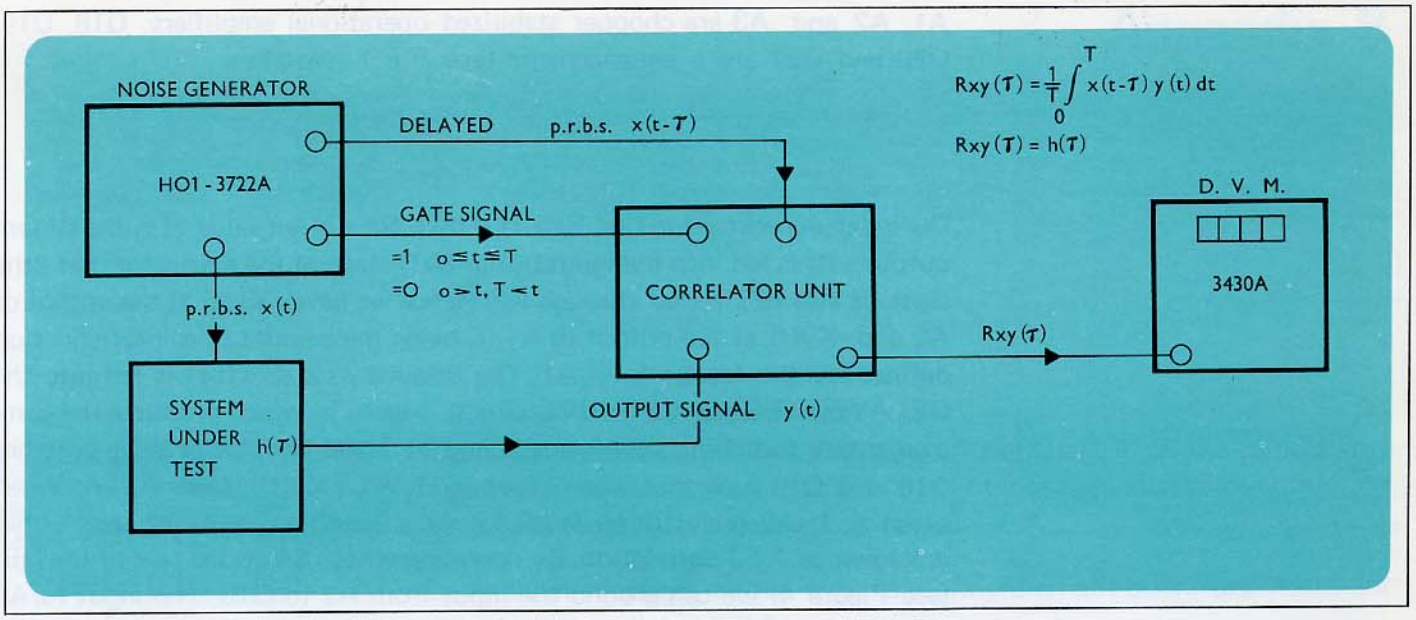
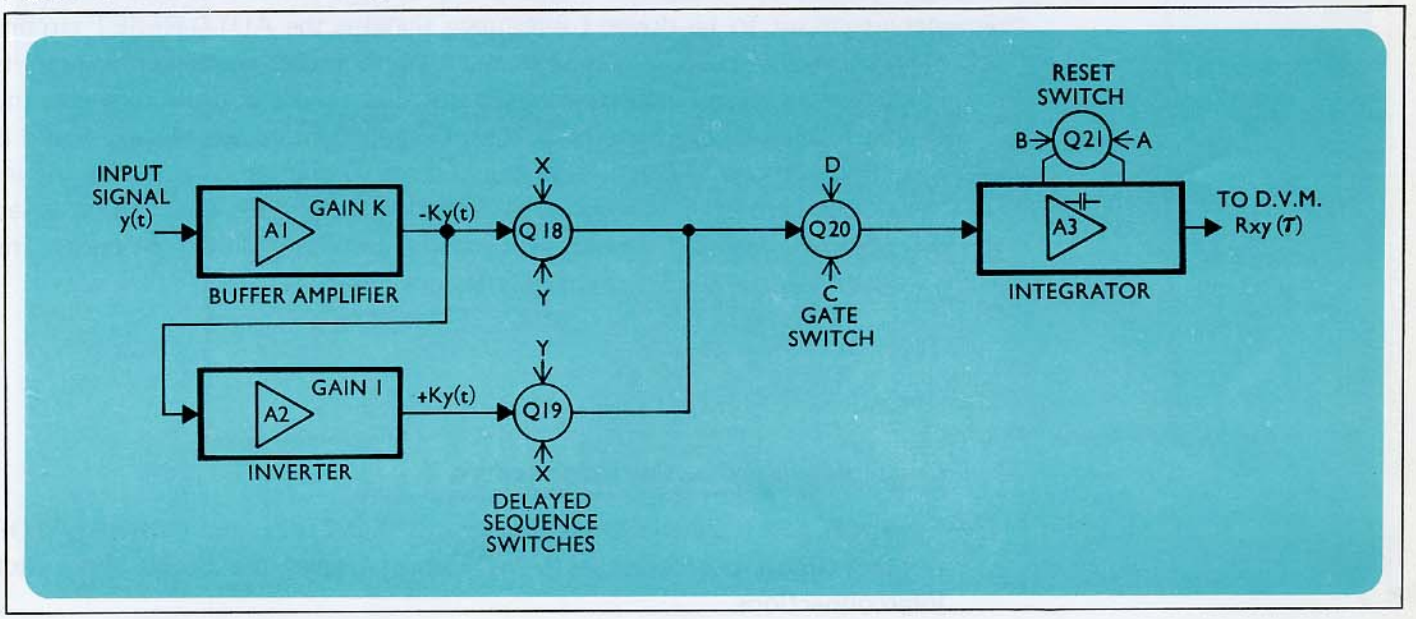


Figure 2. A practical correlation experiment

With the p.r.b.s. as the test signal, multiplication is a simple matter since the only digits of the multiplier are +1 and -1. In the simplest practical system, the multiplication can be performed by a changeover switch which will input the system signal y(t) to the integrator in a positive or negative sense depending on whether the delayed p.r.b.s. x(t - τ) is in a +1 or -1 state. Figure 3 illustrates the correlator unit signal flow paths.

Figure 3. Correlator block diagram



A1, A2 and A3, are chopper stabilized operational amplifiers: Q18, Q19, Q20 and Q21 are p enhancement type F.E.T. switches.

During an experiment to find $Rxy(\tau) = h(\tau)$, for a given value of τ, the system output y(t) is fed into the input buffer (A1) stage of the correlator unit - the signal is also re-inverted through A2. Hence we have +Ky(t) at the output of A2 and -Ky(t) at the output of A1, K being the amount of gain/attenuation defined by the feedback on A1. The delayed p.r.b.s., $x(t-\tau)$ is fed into the DELAYED SEQUENCE DRIVE circuit, Figure 5, which produces the complementary switching waveforms X and Y. These waveforms drive switches Q18 and Q19 such that when $x(t-\tau)$ is +1, A1 (-Ky(t)), feeds A3 and when $x(t-\tau)$ is -1, A2 (+Ky(t)), feeds A3, i.e. we are multiplying by +1 and -1; this is known as 1 : 1 correlation. By operating switch S4 on the rear of the unit (see Figure 4) we can ground the input from A2 to Q19. The input to A3 will now become zero instead of +Ky(t) when $x(t-\tau)$ is -1 i.e. we are multiplying by +1 and 0: this is known as 1:0 correlation.

The experiment time T, to determine one point of $R(\tau)$ is defined in terms of the number of complete p.r.b. sequences by the GATE signal transmitted from the H01-3722A. A switch on the front panel of the H01-3722A can be used to set this to 1, 2, 4 or 8 sequence lengths. The control circuits in the correlator unit are fed by the gate signal. The first of these is the GATE DRIVE circuit, Figure 5, which produces the complementary switching waveforms C and D. These waveforms are used to control Q20 which allows an input to the integrator (A3) during the experiment time T only. The second circuit to be driven by the gate signal is the AUTO-RESET circuit, Figure 5, whose purpose is to reset the integrator after enabling it to hold its final value for several seconds immediately after time T in order to enable the output to be measured on the D.V.M. Complementary waveforms A and B operating through Q21 perform the necessary function of resetting the integrator to zero after readout time. The D.V.M. readout time can be varied by means of a sample time control, on the correlator unit front panel. The gains of A1 and A3 are also adjustable from the front panel.

Circuit details and setting up procedure

Figures 5 and 6 illustrate the circuitry of CONTROL and CORRELATOR printed circuit boards respectively. Figure 4 gives the board and switch interconnections.

Figure 4. Board and switch inter-connections.

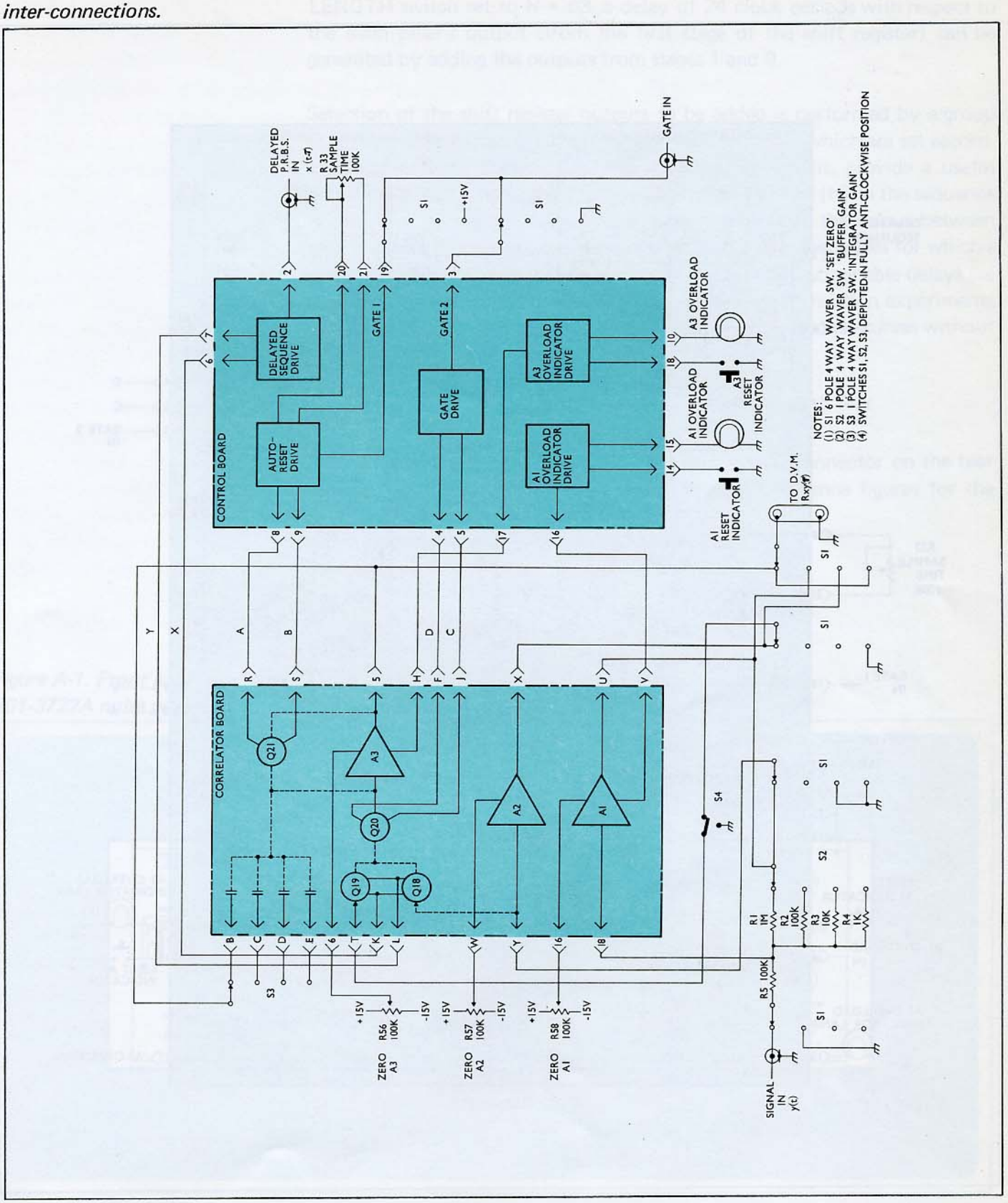


Figure 5. Control board circuitry.

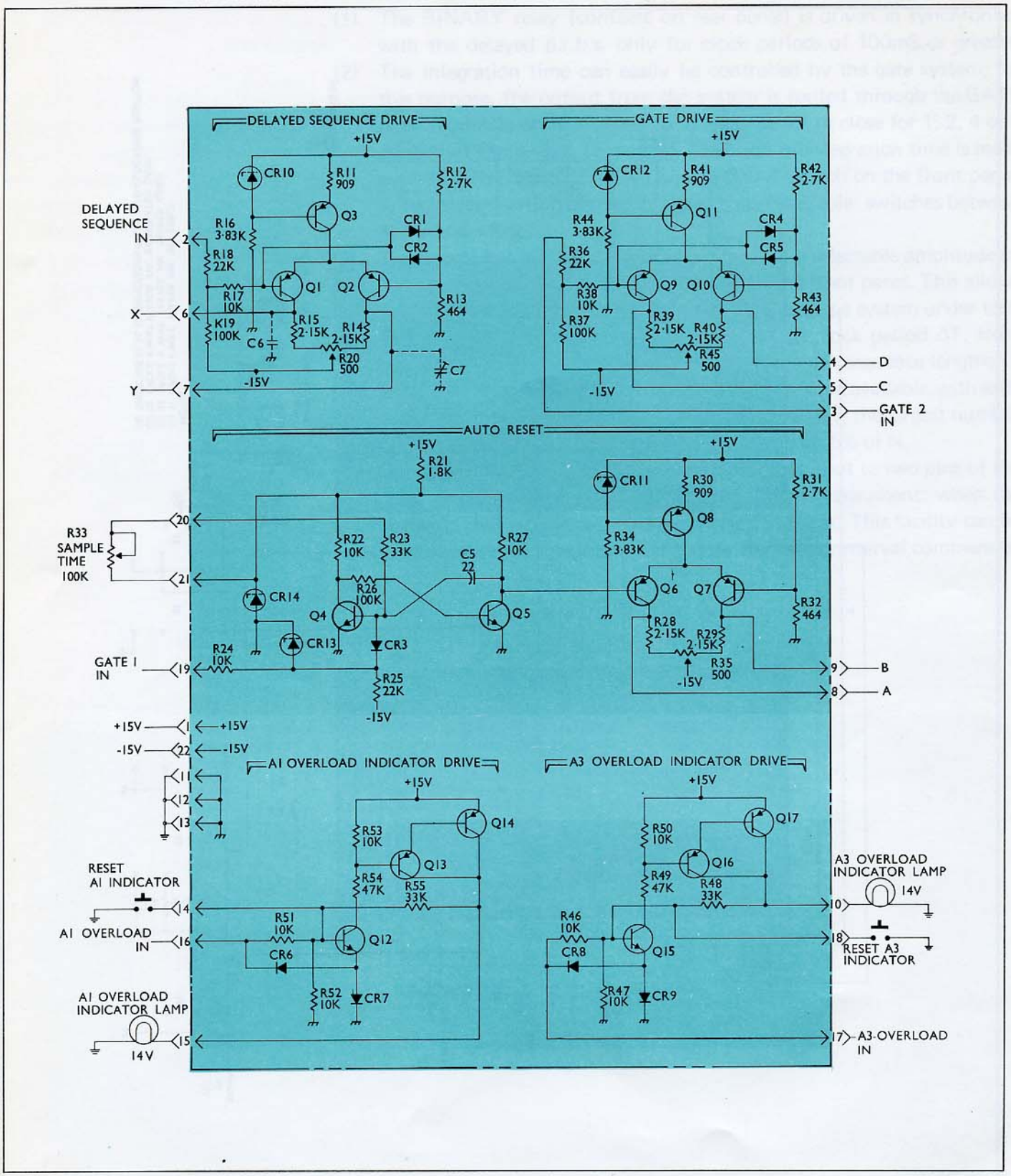
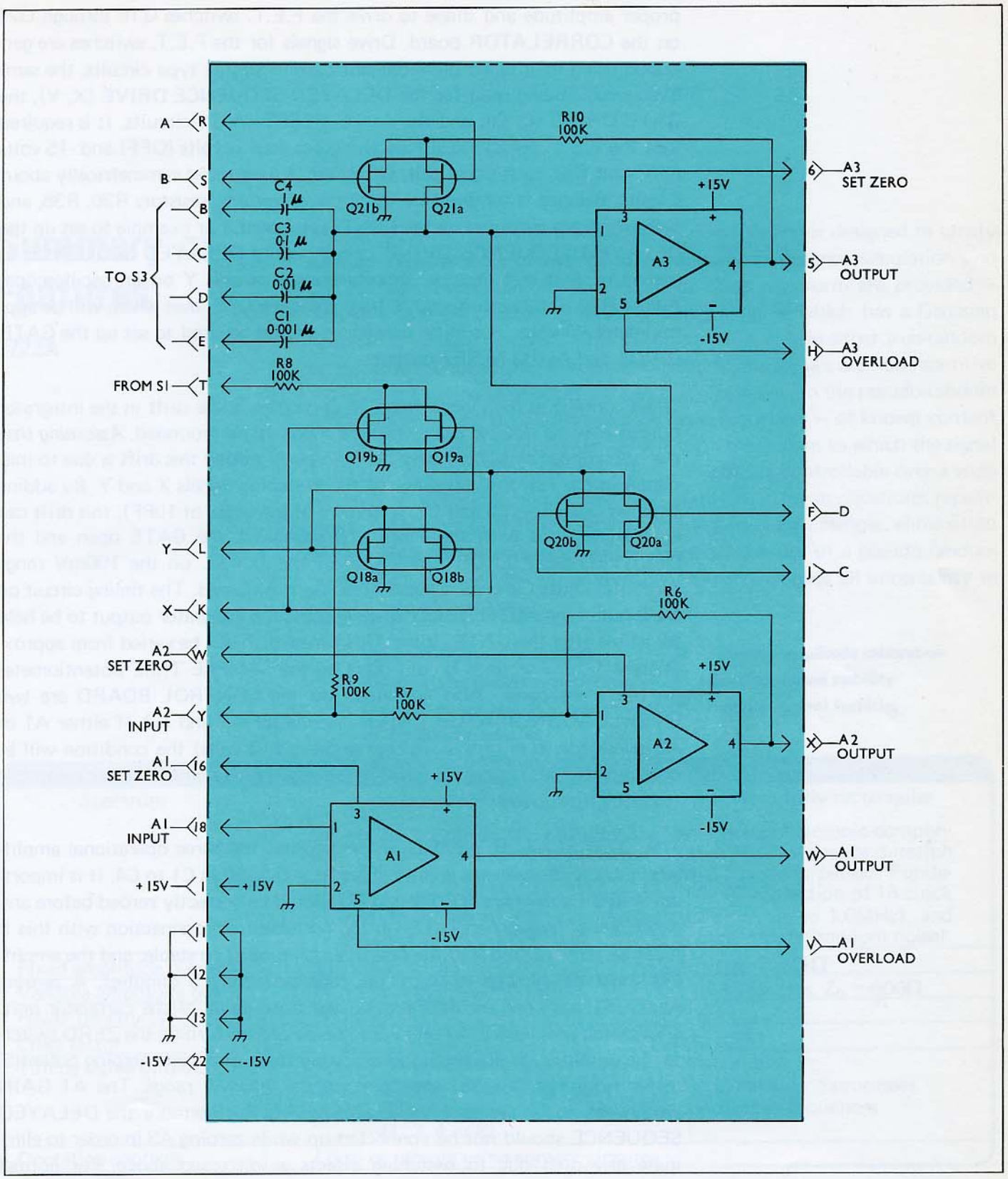


Figure 6. Correlator board circuitry.



The CONTROL BOARD contains all of the circuitry, required to convert the GATE and the DELAYED SEQUENCE signals from the H01-3722A, into the proper amplitude and shape to drive the F.E.T. switches Q18 through Q21 on the CORRELATOR board. Drive signals for the F.E.T. switches are generated using long tailed pair/constant current source type circuits, the same basic circuit being used for the DELAYED SEQUENCE DRIVE (X, Y), the GATE DRIVE (C, D), and the AUTO RESET (A, B) circuits. It is required that the F.E.T. switching signals swing between 0 volts (OFF) and -15 volts (ON) and that each signal pair, (A, B) etc. are balanced symmetrically about 0 volts. Balance is achieved by using preset variable resistors R20, R35, and R45 which are mounted on the CONTROL board. For example to set up the DELAYED SEQUENCE DRIVE circuit, apply DELAYED SEQUENCE to correlator unit and observe, simultaneously, X and Y on an oscilloscope. Adjust R20 until both X and Y have the same OFF level which will be approximately 0 volts. A similar procedure should be used to set up the GATE DRIVE and AUTO RESET outputs.

When running at high clock rates, in particular, some drift in the integrator output may be noticed even when the input y(t) is grounded. ***Assuming that the operational amplifiers have been properly zeroed*** this drift is due to mismatch in the rise and fall times of the switching signals X and Y. By adding trimmer capacitors C6 and C7, (typically of the order of 10PF), this drift can be trimmed out with the input y(t) grounded, the GATE open and the DELAYED SEQUENCE running. With the D.V.M. on the 100mV range carefully adjust C7 until a steady reading is obtained. The timing circuit on the input of the AUTO RESET drive permits the integrator output to be held for a time after the GATE closes. This time which can be varied from approximately 1 to 3 seconds is controlled by the SAMPLE TIME potentiometer on the front panel. Also contained on the CONTROL BOARD are two OVERLOAD INDICATOR DRIVE circuits for A1 and A3. If either A1 or A3 overloads, (i.e. output voltage exceeds ±10 volts) the condition will be displayed on front panel lamps. These circuits are latching and are resettable from the front panel.

The CORRELATOR BOARD accommodates the three operational amplifiers, the F.E.T. switches and the integrator capacitors C1 to C4. It is important that all amplifiers A1, A2 and A3 should be correctly zeroed before any experiments are carried out with the correlator. In connection with this it must be remembered that the power supplies must be stable, and the amplifiers must be allowed to warm up, (approximately 5 minutes). A zeroing switch S1 has been incorporated on the front panel of the correlator unit. This switch enables A1, A2 and A3 to be zeroed by turning the ZERO switch to the amplifier in question and adjusting the appropriate zeroing potentiometer until the D.V.M. reads zero on the 100mV. range. The A1 GAIN switch should be set to 1 while zeroing A1. Furthermore the DELAYED SEQUENCE should not be connected up while zeroing A3 in order to eliminate any drift due to switching effects as discussed above. For normal

operation the ZERO switch should be set to 'RUN'.

Note that the overload circuits will normally indicate an overload condition when the correlator unit is switched on, but can be reset after several seconds.

Calibration and checking

In order to carry out a quantitive measurement with the correlator unit it is necessary to check its 'gain'. The gains of both the input buffer amplifier A1 and the integrator A3 are variable, the theoretical value of the gains being read off the front panel; this in most cases may be sufficient. The total gain of the unit is K x G where K is the gain of A1 and G the gain of A3 (the units of G are sec $^{-1}$). For example, if a constant voltage V was applied to input y(t) and the integrator allowed to run for time T the final output voltage V_T at $R_{xy}(\tau)$ would be V x T x K x G. Therefore, we can measure the product K x G by applying a known constant voltage to the input y(t) and integrating for a known time T i.e. K x G = $V_T/(V \times T)$. For a given gain setting this should be carried out with the DELAYED SEQUENCE input in the 1 and also the 0 state, integrating positively and negatively respectively. Both values of K x G should be the same.

The overall drift of the correlator unit can be checked by grounding the input y(t) and opening the GATE input, letting the instrument run and recording its output $R_{xy}(\tau)$ signal. This experiment should be performed with the DELAYED SEQUENCE input in the 1 state and again in the 0 state. Switching transient drift can be checked as described previously.

1. *Hughes M. and Noton A. "The Measurement of Control System Characteristics by means of a Cross-correlator." Proc.IEE.Jan.1962.*

2. *Hewlett-Packard application note 98-1 "Model 3722A aids design of process control systems."*

Appendices

Appendix A

Summary of Features

3722A

The hp 3722A is a precision low frequency noise generator designed to satisfy all user requirements in two fields – random disturbance simulation and control systems evaluation. Two types of noise waveform are provided – BINARY and GAUSSIAN (the latter being a signal which has a Gaussian probability density function). Both outputs are available in either true-random or pseudo-random forms. In the random mode, the signals are non-repetitive yet have well defined statistical and spectral properties. In the pseudo-random mode, however, the signals are repeated noise sequences – of known content and duration – each having a similar effect on the system to which the signal is applied. The noise outputs from the hp 3722A are controllable over a wide range, both in bandwidth and sequence length. In many applications, repeatability of test signal offers immediate advantages . . . for example, elimination of statistical variance in test results. Further, the use of a pseudo-random noise signal in place of its random counterpart removes all uncertainty in calculations of test time.

- **Very wide frequency coverage**
- **Excellent low frequency performance**
- **Constant power output – independent of bandwidth selected**
- **Accurate amplitude calibration**
- **Good zero level stability**
- **Remote control facilities**

	BINARY	GAUSSIAN
Spectrum	$(\sin x/x)^2$ shape	Nominally rectangular
	In pseudo-random mode, both spectra have discrete harmonic components: in random mode, spectra are continuous. Noise sequence duration = N ΔT, where N is sequence length and ΔT is clock period. Fundamental = lowest frequency in spectrum = 1/N ΔT. Selection of 18 clock periods, from 1μS to 333 seconds (external clock up to 1.0MHz), and 17 sequence lengths, from 15 to 1,048,575, plus infinite (random noise).	
Fixed amplitude output	±10V, Z_0 <10Ω	3.16Vrms, Z_0<1Ω
Variable amplitude output	±0.1V to ±10V, Z_0 = 600Ω	0.1 to 3.16V rms, Z_0 = 600Ω
Power density (V^2/Hz)	200 ΔT	200 ΔT
Crest factor	-----	Up to 3.75
Timing signal outputs	Sync – pulse occuring once in each noise sequence Gate – allows synchronous control of external measuring processes. Gate signal lasts for selected number of noise sequences (1, 2, 4 or 8).	
Operating controls	Local or remote using contact closures	

Modified Specification

H01-3722A

General information

Specification H01-3722A is a standard hp Model 3722A Noise Generator modified to provide a second binary output which can be delayed by a selectable number of clock periods with respect to the main binary output. The delayed binary output is available only when the instrument is in the pseudo-random mode, that is, generating repetitive noise sequences.

Basis of the hp 3722A is a clock-controlled binary waveform generator arranged so that transitions between output levels can occur only on 'beats' of the clock. The clock signal is normally taken from an internal crystal-controlled timebase which gives a selection of 18 clock frequencies ranging from 0.003Hz to 1MHz (clock period, ΔT, from 333 seconds to 1μS): alternatively, the clock signal may be supplied by an external timebase (up to 1.0MHz).

The binary waveform generator is a shift register which, in the pseudo-random mode, operates in a closed loop condition. Feedback is so arranged that the output from the shift register is a repeated, fixed length sequence of binary ones and zeros. The length of a 'pseudo-random binary sequence' (p.r.b.s.) of this type is stated in terms of a number of clock periods, and is equal to $N = 2^n - 1$, where n is the number of shift register stages used to generate the sequence. In the hp 3722A, n is selectable from 4 to 20 stages, giving sequence lengths from 15 to 1,048,575. (The total length of the register is in fact 32 stages, but of these only 20 maximum are used in sequence generation).

Delay generation

Since the output from one stage of the shift register is identical with that from the preceding stage, but delayed by one clock period, binary sequences delayed by up to 31 clock periods could be taken direct from the shift register. This delay, however, is insufficient for all sequence lengths other than N = 15 and N = 31. To create the necessary longer delays, use is made of the 'shift and add' property of pseudo-random sequences — a sequence which is modulo-two added to a delayed version of itself produces yet another

delayed version of the original sequence. For example, with the SEQUENCE LENGTH switch set to N = 63, a delay of 24 clock periods with respect to the main binary output (from the first stage of the shift register) can be generated by adding the outputs from stages 1 and 9.

Selection of the shift register outputs to be added is performed by a group of decade switches on the front panel. These switches, which are set according to a conversion table supplied with the instrument, provide a useful number of delays ranging from zero to the number of bits (N) in the sequence in use. With the longer sequences in particular, not all the delays between zero and N are obtainable: however, with each of the sequences for which a conversion table is provided (N = 15 to N = 2047), the obtainable delays are well enough distributed to avoid difficulties in cross-correlation experiments (sufficient 'points' are available to generate impulse response curves without misleading omissions).

Delayed binary output

The delayed binary output is available from a BNC connector on the rear panel of the H01-3722A instrument. Typical performance figures for the delayed output are:-

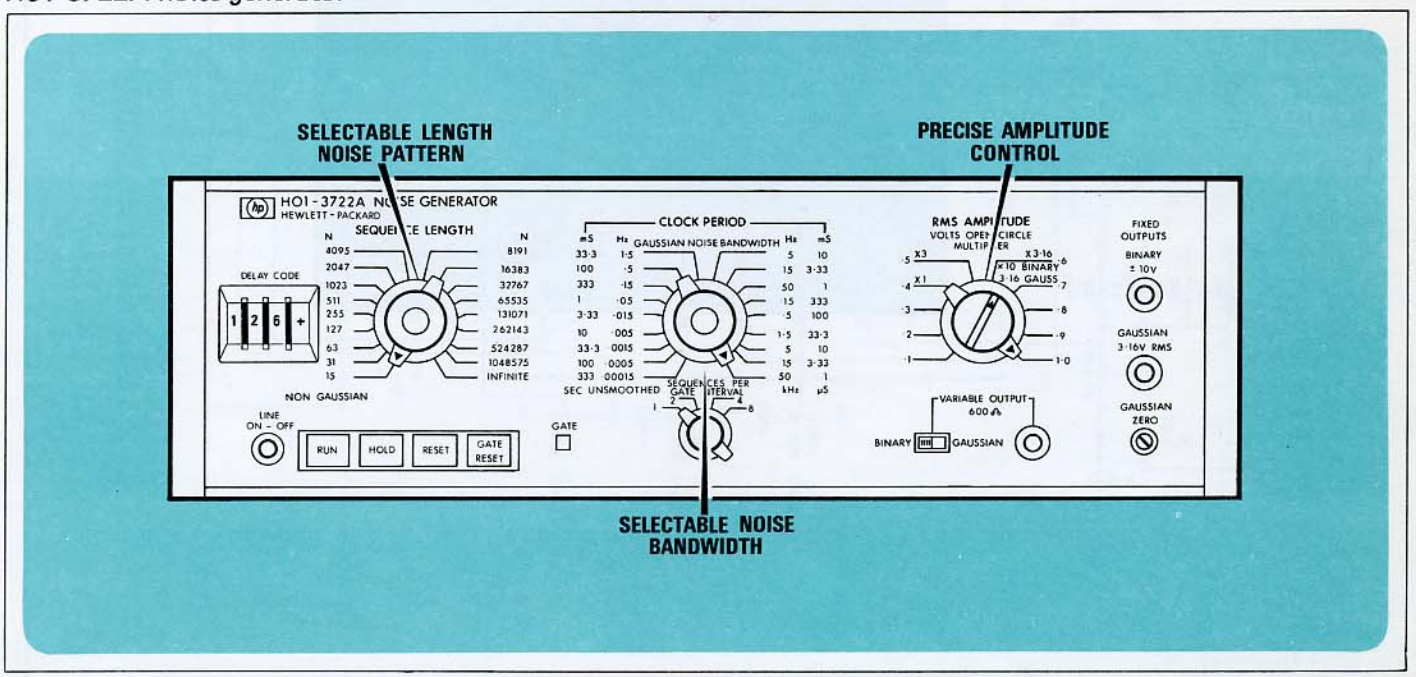
Amplitude: switches between +1.5V and +12V

Maximum sink current at 1.5V level: 10mA

Rise time: <50nS

Fall time: <20nS

Figure A-1. Front panel of model H01-3722A noise generator



The H01-3722A, together with an integrator, provides all the facilities required for point-by-point correlation.

(1) The BINARY relay (contacts on rear panel) is driven in synchronism with the delayed p.r.b.s. only for clock periods of 100mS. or greater.

(2) The integration time can easily be controlled by the gate system; for this purpose, the output from the system is routed through the GATE relay (contacts on rear panel), which can be set to close for 1, 2, 4 or 8 periods of the p.r.b.s. (Figure 5). Selection of integration time is made by the SEQUENCES PER GATE INTERVAL switch on the front panel. A 'logic level' version of the gate signal is also available: switches between +1.5V and +12V.

(3) The undelayed BINARY signal is available at a selectable amplitude of up to ±10V from the VARIABLE output on the front panel. This allows the operator easily to set the input level to suit the system under test.

(4) The delay τ is selectable, in increments of the clock period ΔT, from zero to $N\Delta T$ where N is the sequence length. With sequence lengths 15, 31 and 127, all values of τ between zero and N are available: with each of the other documented sequences (up to N = 2047), the largest number of consecutive missing points is never greater than 5% of N.

(5) Contacts of the GATE RESET button are brought out to two pins of the CONTROL receptacle on the rear panel of the instrument: when the button is pressed, the two pins are shorted together. This facility can be used to reset the integrator just before the gating interval commences.

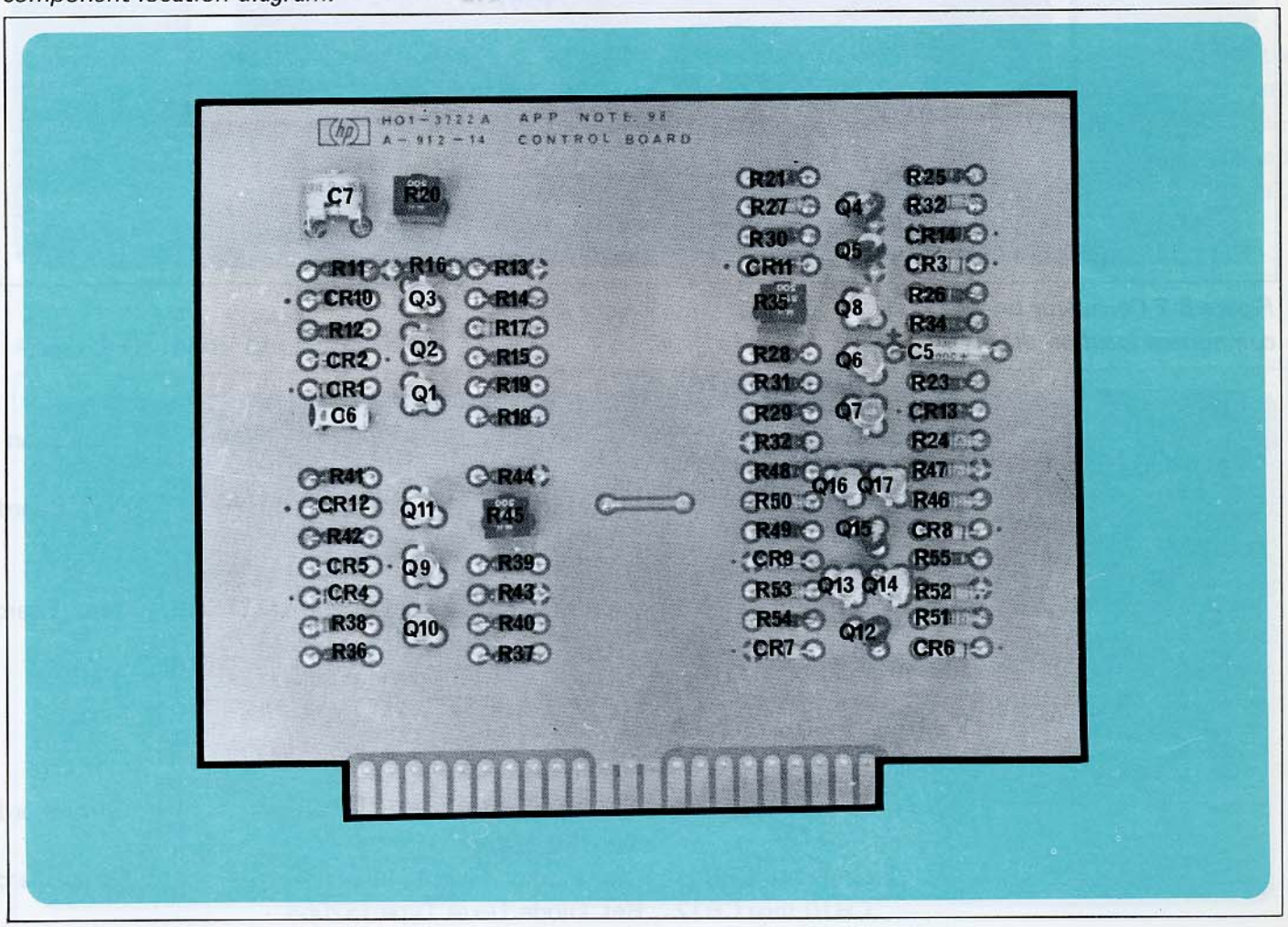
Appendix B

Control & Correlator Board Components

The following components list does not contain details of all the components required to build a correlator unit, but only those elements which enable the circuits to be built to the correct standard.

Component locations on the two main printed circuit board assemblies are given in Figures B-1 and B-2.

Figure B-1. Control board component location diagram.



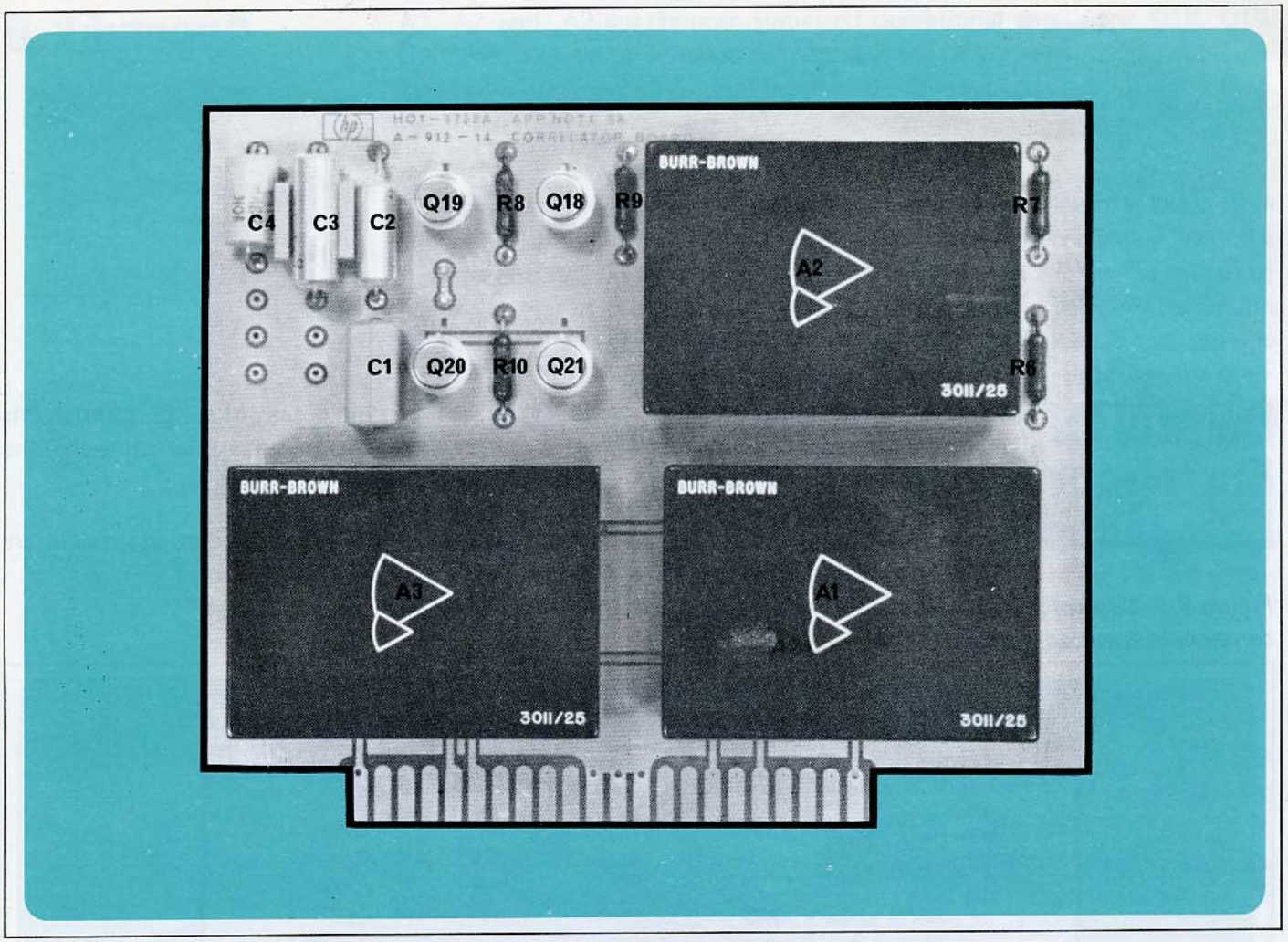


Figure B-2 Correlator board component location diagram.

COMPONENTS LIST

Comp. No.	Type	Location
A1	Op. Amp. Burr Brown Type 3011/25	Corr. Board
A2	"	"
A3	"	"
Q1 thru Q3	P.N.P. Transistor Texas Type 2N727	Cont. Board
Q4, Q5	N.P.N. Transistor Texas Type 2N914	"
Q6 thru Q11	P.N.P. Transistor Texas Type 2N727	"
Q12, Q15	N.P.N. Transistor Texas Type 2N914	"
Q13, Q14, Q16, Q17	P.N.P. Transistor Texas Type 2N727	"
Q18 thru Q21	P. Enhancement M.O.S.T. Plessey Type ML102A	Corr. Board
CR1 thru CR9	Diode Texas Type 1S44	Cont. Board
CR10 thru CR12	Ref. Diode Texas Type 1S2068	"

Comp. No.	Type				Location
CR13	Ref. Diode Texas Type 1S2051				Cont. Board
CR14	Ref. Diode Texas Type 1S2043				"
C1	Capacitor Polycarbonate 0.001μF				Corr. Board
C2	"	"	0.01μF		"
C3	"	"	0.1μF		"
C4	"	"	1μF		"
C5	Capacitor Tantalum 22μF				Cont. Board
C6	Fixed Trimmer Capacitor Approx. 10PF				"
C7	Variable Trimmer Capacitor 2PF-20PF				"
R1	Resistor	1MΩ	High Stab	0.5%	Switch Mounted
R2	"	100KΩ	"	0.5%	"
R3	"	10KΩ	"	0.5%	"
R4	"	1KΩ	"	0.5%	"
R5	"	100KΩ	"	0.5%	"
R6 thru R10	"	100KΩ	"	0.5%	Corr. Board
R11	"	909Ω	"	1%	Cont. Board
R12	"	2.7KΩ		5%	"
R13	"	464Ω		5%	"
R14, R15	"	2.15KΩ		1%	"
R16	"	3.83KΩ		5%	"
R17	"	10KΩ		5%	"
R18	"	22KΩ		5%	"
R19	"	100KΩ		5%	"
R20	Variable Resistor 500Ω Linear			5%	"
R21	Resistor	1.8KΩ		5% 1/4W	"
R22	"	10KΩ		5%	"
R23	"	33KΩ		5%	"
R24	"	10KΩ		5%	"
R25	"	22KΩ		5%	"
R26	"	100KΩ		5%	"
R27	"	10KΩ		5%	"
R28, R29	"	2.15KΩ		1%	"
R30	"	909Ω		1%	"
R31	"	2.7KΩ		5%	"
R32	"	464Ω		5%	"
R33	Variable Resistor 100KΩ Linear			5%	Front Panel
R34	Resistor	3.83KΩ		5%	Cont. Board
R35	Variable Resistor 500Ω Linear			5%	"
R36	Resistor	22KΩ		5%	"
R37	"	100KΩ		5%	"
R38	"	10KΩ		5%	"
R39, R40	"	2.15KΩ		1%	"
R41	"	750Ω		1%	"
R42	"	2.7KΩ		5%	"
R43	"	464Ω		5%	"

Comp. No.	Type			Location
R44	Resistor	3.83KΩ	5%	Cont. Board
R45	Variable Resistor	500Ω Linear	5%	"
R46, R47, R50	Resistor	10KΩ	5%	"
R48	"	33KΩ	5%	"
R49	"	47KΩ	5%	"
R51, R52, R53	"	10KΩ	5%	"
R54	"	47KΩ	5%	"
R55	"	33KΩ	5%	"
R56, R57, R58	Variable Resistor	100KΩ Linear	5%	Front Panel

NB All fixed resistors 1/8W unless otherwise specified

Appendix C

Power Supply Requirements

While the power supply voltages used with the operational amplifiers are not critical, best results are obtained if the supply voltages are maintained close to their rated values.

Rated Supply Voltage	±15 V d.c.
Voltage Range	±12 to ±18 V d.c.
Max. Current Drain	±250mA.
Supply Regulation	1%
Noise and Ripple	<1mV. r.m.s.

Note:-
High frequency performance will be improved and crosstalk between adjacent amplifier channels will be prevented if the supply impedance seen from the operational amplifiers' connectors is held to a low value at all frequencies from d.c. to 100kHz.

Printed in U.K.

5952-3101