Direct Power MOSFET Capacitance Measurement at 3000 V

Application Note B1505-4

Agilent B1505A Power Device Analyzer/Curve Tracer

Introduction

The input, output and reverse transfer capacitance of power MOSFETS (Ciss, Coss and Crss respectively) are critical device parameters for switching applications. Unfortunately, the DC voltages applied to power MOSFETs during many switching applications are in the hundreds or even thousands of volts; this has made the measurement of these parameters under specified DC bias voltage conditions impossible using conventional capacitance meters. Therefore, many elaborate schemes have been developed to measure these parameters using a variety of homemade test setups that usually involve measuring a device's step response and extracting the value of capacitance from the resulting RC time constant.

The Agilent B1505A Power Device Analyzer/Curve Tracer supports a high-voltage source/monitor unit (HVSMU), a multi-frequency capacitance measurement unit (MFCMU) and a high-voltage bias-T that permit direct measurement of high-power MOSFET capacitance measurement.

This solution makes it easy to directly measure Ciss, Coss and Crss at DC bias voltages of up to 3000 V. This application note will explain the theory behind these measurements and illustrate the measurement techniques required to make these measurements using Agilent B1505A.

High-Voltage Bias-T

The high-voltage bias-T is an available option for the B1505A that is designed to work with the MFCMU and HVSMU. A simplified circuit schematic of the high-voltage bias-T is shown in Figure 1.

Note: *When using the bias-T the measurement capabilities of the MFCMU are reduced. The measurement frequency and capacitance measurement range to maintain 1% measurement accuracy when using the bias-T are as follows:*

Frequency Range: 10 kHz to 1 MHz
Capacitance Range: 1 pF to 10 nF

The 10 nF limit on the capacitance of the device under test (DUT) is due to the effects of the series combination of the 100 nF bias-T capacitance with the DUT capacitance.

There are two versions available of the high-voltage bias-T. One version is designed to work with the N1259A high-power packaged device test fixture, and it is an option for the test fixture. The inputs to the N1259A bias-T version for testing packaged devices are shown in Figure 2.

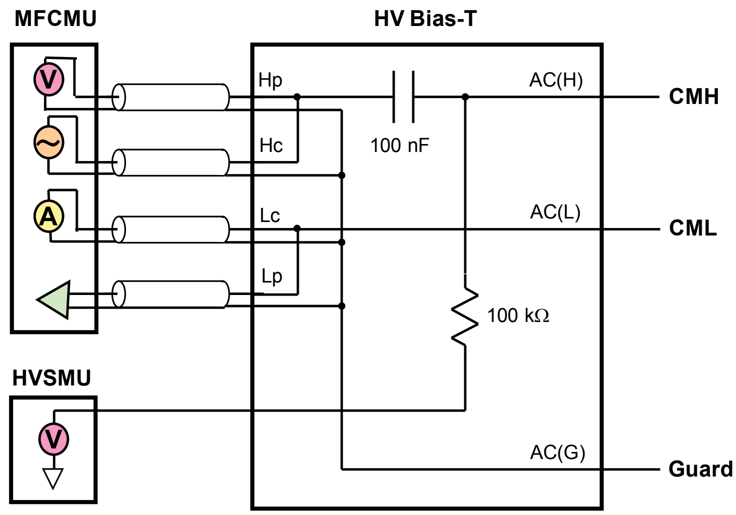

Figure 1. The B1505A high-voltage Bias-T connects to the B1505A's MFCMU and HVSMU modules to provide up to 3000 V of DC bias during capacitance measurements.

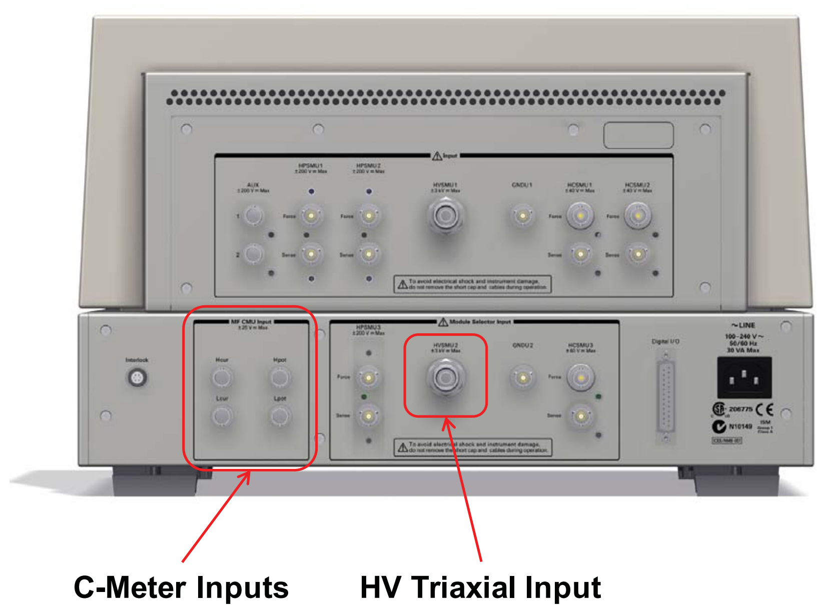

Figure 2. Rear view of the N1259A high-power packaged device test fixture showing the high-voltage bias-T option. Note: Module selector option is also shown in this example.

The inside of the test fixture allows the user to access the CMH, CML and AC guard signals and connect them up to devices using furnished jumper cables.

Figure 3 shows the N1260A, which is the wafer prober version of the high-voltage bias-T. The CMH and CML outputs of the N1260A are SHV (safe high voltage) connectors, as is the AC guard signal. Note that for both versions of the high-voltage bias-T, the AC guard of the MFCMU is available. To understand the use of the AC guard it is first necessary to review the basics of high-power MOSFET capacitance measurement.

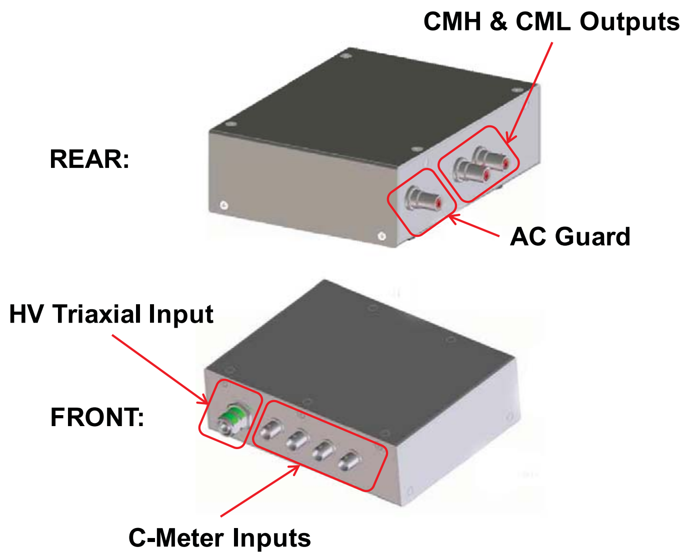

Figure 3. The N1260A high-voltage bias-T for use with wafer probers.

High-Voltage MOSFET Capacitance Measurement Basics

A conceptual diagram of a power MOSFET showing the various junction capacitances is shown in figure 4.

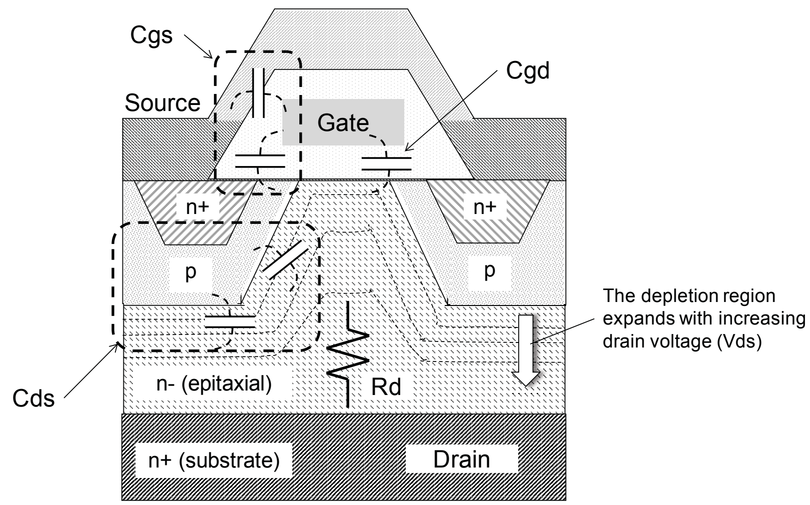

Figure 4. Cross-section of a power MOSFET showing the various components of junction capacitance.

For power MOSFETs the drain is biased to a very high voltage, and both the drain-to-source capacitance (Cds) and the gate-to-source capacitance (Cgs) are dependent on the DC value of the drain voltage. The AC model of a MOSFET is shown in figure 5.

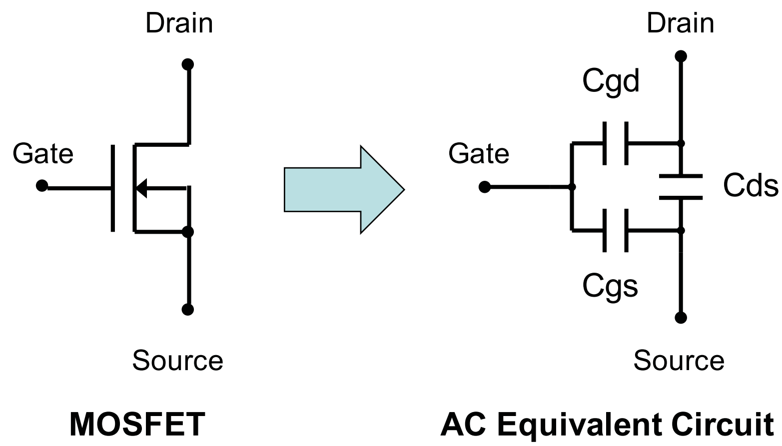

Figure 5. AC equivalent circuit model of a power MOSFET showing the various junction capacitances.

Let us now consider what happens when we try to measure any single one of these three capacitances using a capacitance meter. Figure 6 shows the situation when we try to measure an unknown capacitance (Cx) on a 3-terminal device without using the AC guard (i.e. unused terminal is floating). This figure shows that when the unused terminal is floating current can flow through the other two capacitors resulting in erroneous measurement results. The best way to prevent this from occurring is to provide an alternative current path so that the current flowing through Ca does not flow back through Cb into the CML node. We can achieve this by connecting the unused terminal to the AC guard of the capacitance meter. Note: It is important to understand that the AC guard is the circuit common of the auto-balancing bridge and that it is connected to the shields of the four-terminal pair connectors. The AC guard is NOT the same as the ground terminal, which is connected to the chassis ground.

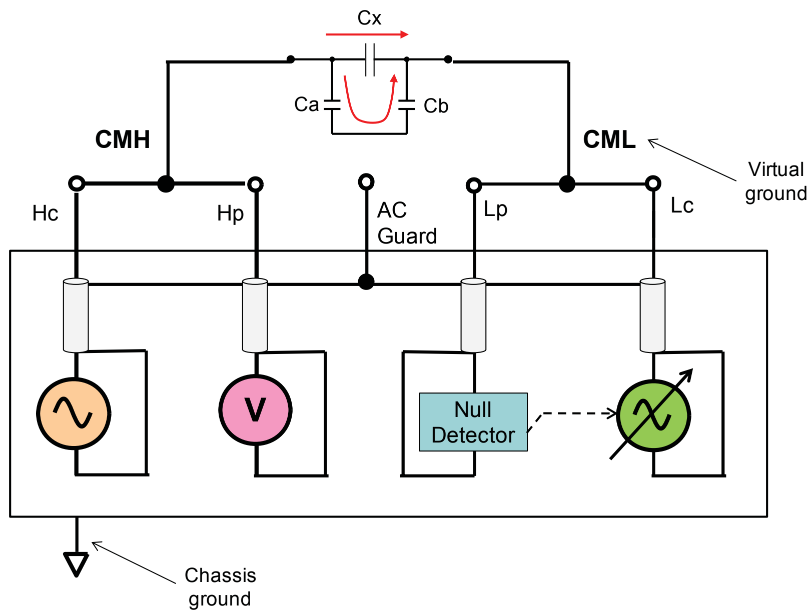

Figure 6. Measuring junction capacitance with a capacitance meter not using the AC guard.

Figure 7 shows the benefit of connecting the AC guard to the unused measurement terminal. When the AC guard is connected to the third terminal the current flowing through the parasitic path (Ca) does not affect the accuracy of the measurement of the unknown capacitance (Cx), since the capacitance measurement is done through the CML node. Of course, this scheme assumes that the impedance of the AC guard node is much less than that of the parasitic path (Cb). Although this discussion did not include the use of the HVSMU and HV bias-T, we will explain how to incorporate them as we examine each capacitance measurement individually.

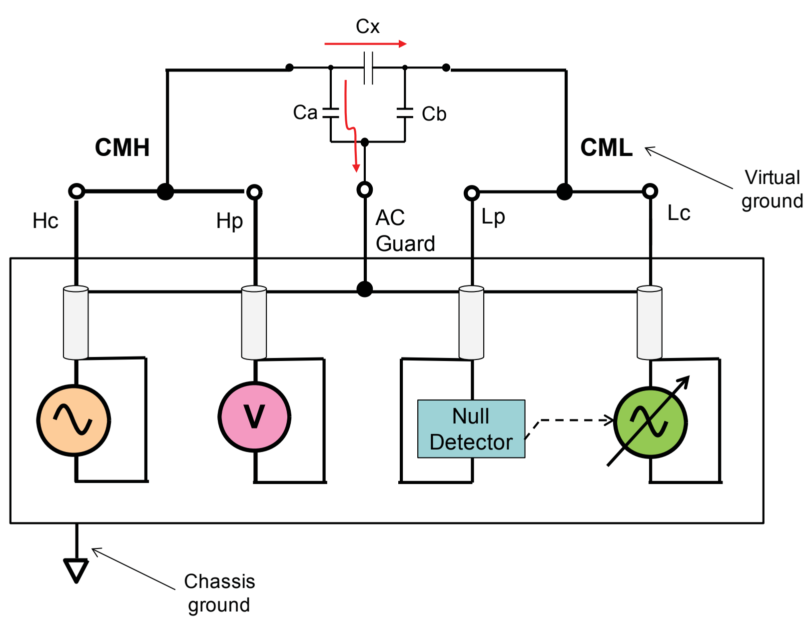

Figure 7. Measuring junction capacitance with a capacitance meter using the AC guard.

Measuring Ciss, Coss and Crss

The junction capacitances can be related back to the more common power MOSFET datasheet specifications through the following equations:

$$C_{iss} = C_{gd} + C_{gs}$$
$$C_{oss} = C_{gd} + C_{ds}$$
$$C_{rss} = C_{gd}$$

Since the output capacitance (Crss) and reverse transfer capacitance (Coss) measurements are simpler to make than the input capacitance (Ciss) measurement we will discuss them first.

Crss is equivalent to Cgd, so to make this measurement we need to remove any interference from Cds and Cgs by using the AC guard. Figure 8 shows the correct way to measure Crss using the HV bias-T.

To measure Coss we simply need to short the gate and source terminals using a wire as shown in Figure 9.

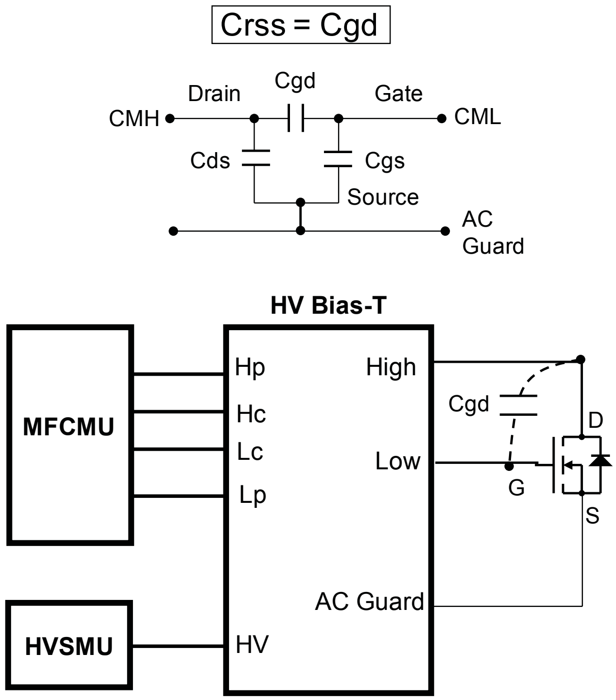

Figure 8. Connection scheme to measure the reverse transfer capacitance (Crss).

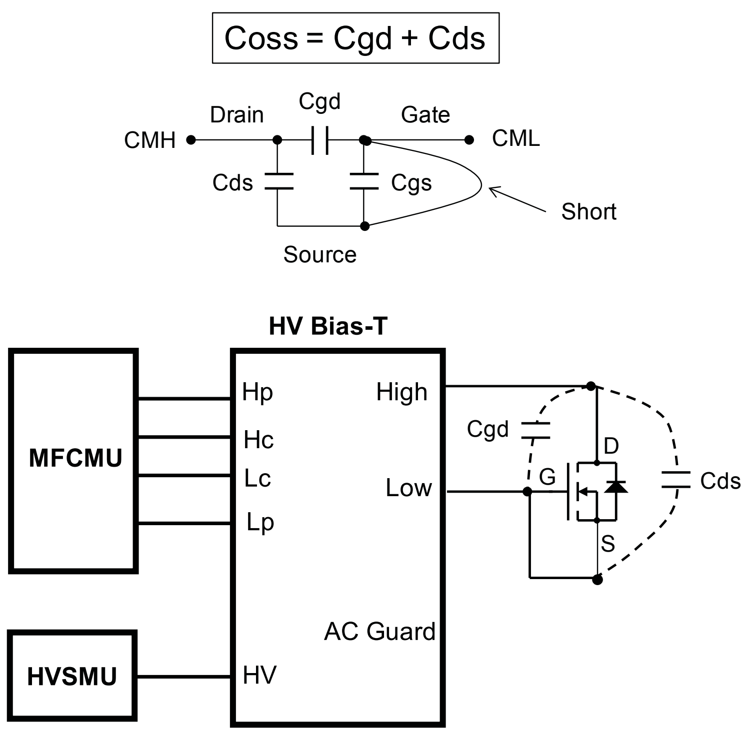

Figure 9. Connection scheme to measure the output capacitance (Coss).

Note that when making this measurement we do not need to use the AC guard since we want to measure the current flowing through both Cgd and Cds. Figure 10 shows a direct capacitance measurement of Coss on a high power MOSFET made using the B1505A.

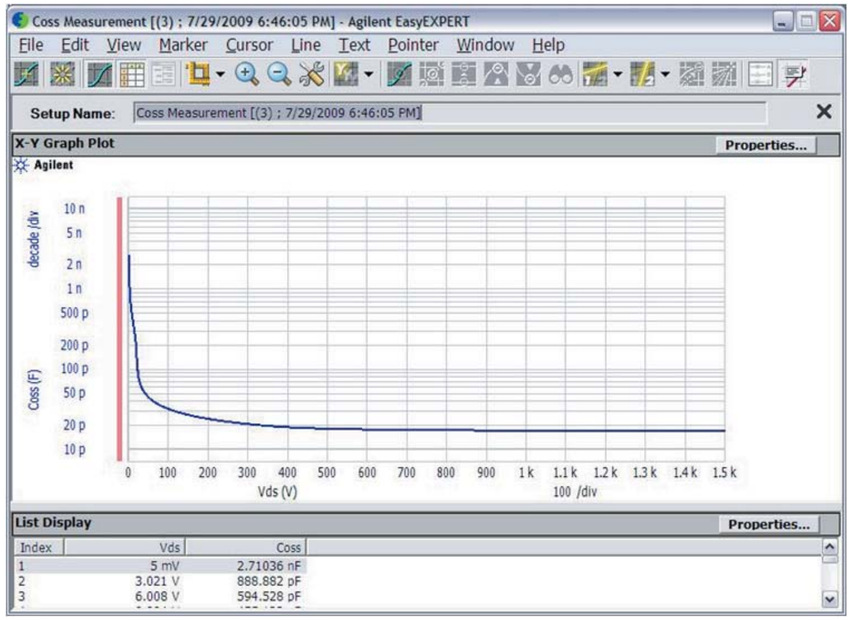

Figure 10. Output capacitance (Coss) measured at 1500 V of DC bias.

Measuring the input capacitance (Ciss) presents some challenges that are not present for the Crss and Coss measurements. Although we need to short the AC guard to the drain, we also need to bias the drain to high-voltage. However, this is not possible to do using the high-voltage bias-T. Therefore, in this case it is necessary to bypass the high-voltage bias-T and use an external blocking resistor and capacitor. In addition, the capacitor used to connect the drain and AC guard has to be much larger than Cgd or Cds such that the impedance seen by the drain with respect to the AC guard is much smaller than the impedance that it sees to either the source or to the gate. Conversely, we need to connect the HVSMU up to the drain through a relatively large resistor to prevent the HVSMU from interfering with the AC signal coming from the MFCMU. Figure 11 illustrates this technique.

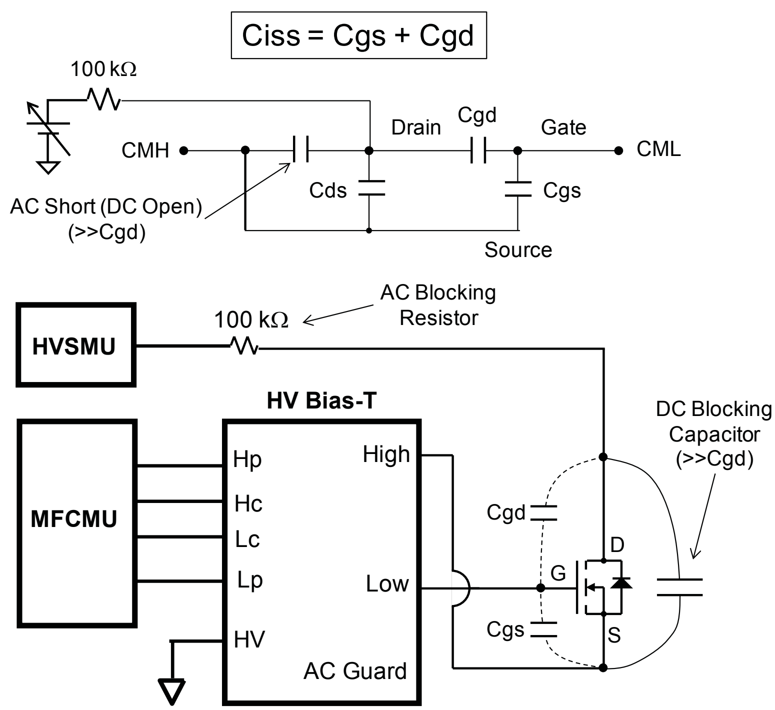

Figure 11. Connection scheme to measure the input capacitance (Ciss).

The size of the blocking capacitor required of course depends upon the value of Cgd. Figure 12 shows the connections necessary to correctly measure Ciss using the N1259A test fixture.

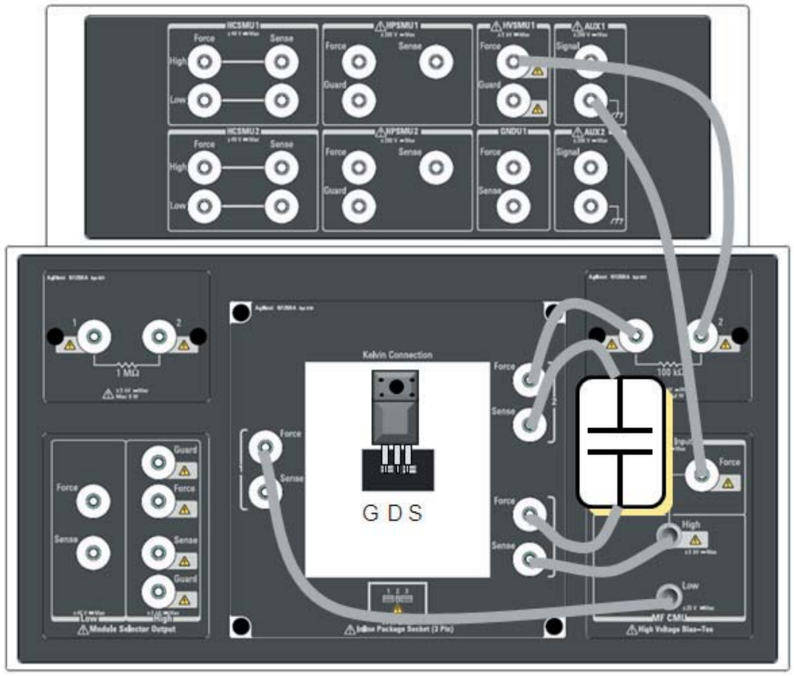

Figure 12. Example showing the connections required to measure Ciss on a packaged device (using the N1259A high power test fixture).

Figure 13 shows a direct capacitance measurement of Ciss on a high power MOSFET made using the B1505A.

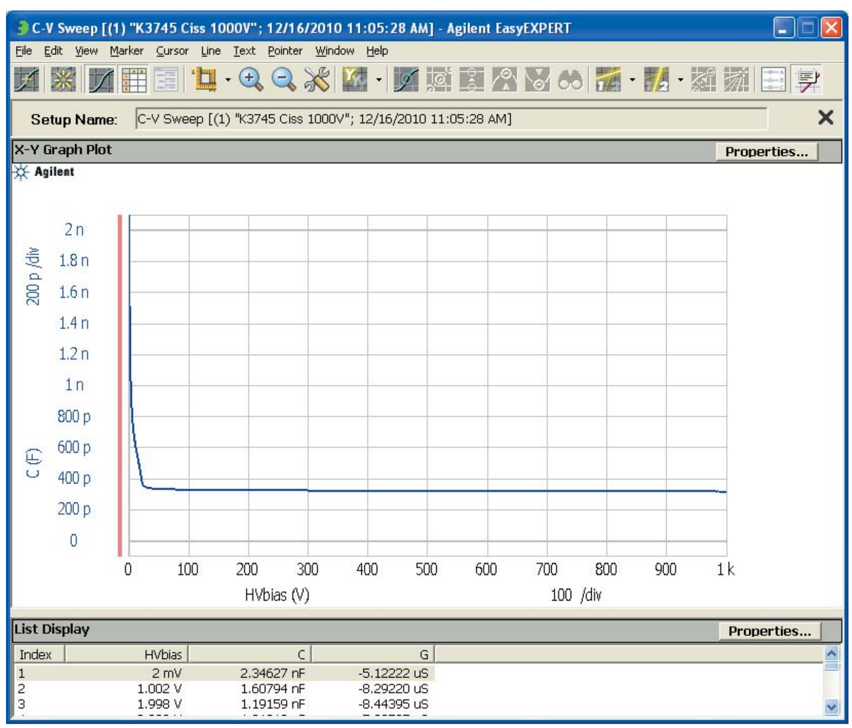

Figure 13. Input capacitance (Ciss) measured at 1000 V of DC bias.

Measurement Frequency and Compensation Considerations

Most data sheets specify the Ciss, Coss and Crss at a frequency of 1 MHz. However, accurate capacitance measurements using a capacitance meter require that proper compensation of the cables and fixturing be performed first. This process is discussed at great length in the Agilent Parametric Measurement Handbook (5990-5278EN), but as a quick review there are three types of capacitance compensation that can be performed:

Open Compensation – The CMH and CML outputs of the capacitance meter through all of the attached cabling and test fixturing are left open, and the capacitance meter performs an open compensation.

Short Compensation – The CMH and CML outputs of the capacitance meter through all of the attached cabling and test fixturing are shorted together, and the capacitance meter performs a short compensation.

Load Compensation – The CMH and CML outputs of the capacitance meter through all of the attached cabling and test fixturing are connected to a load standard of known impedance, and the capacitance meter performs a load compensation.

For low-power capacitance measurements load compensation generally only needs to be performed for measurements above 5 MHz. However, when using the high-voltage bias-T and making high-power capacitance measurements, load compensation needs to be performed at much lower frequencies to insure accurate measurement results.

Figure 14 shows a plot of gate to source (Cgs) capacitance (Cp-G) versus frequency using the high-voltage bias-T after performing open/short capacitance compensation. As this data shows, the measured conductance becomes negative as the frequency increases beyond 100 kHz.

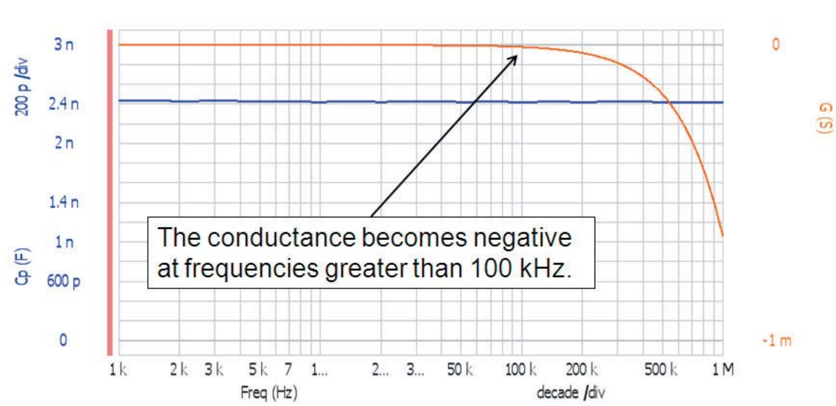

Figure 14. Plot of Cp-G versus frequency using the high-voltage bias-T showing that the conductance (G) becomes negative for frequencies above 1 kHz when only an Open/Short calibration sequence has been performed.

While this effect can be eliminated by performing a load capacitance compensation, it is not very practical to do a load compensation in most high-power device wafer probing environments. Therefore, if the load compensation cannot be performed it is best to measure the MOSFET capacitance parameters at frequencies no greater than 100 kHz. Figure 15 shows a table that summarizes the relative measurement accuracy of a Cp-G measurement on a power MOSFET as a function of compensation performed for the both 100 kHz and 1 MHz (when using the high-voltage bias-T).

	100 kHz		**1 MHz**	
	Cp	**G**	**Cp**	**G**
Open	Small error (1%)	OK	Large error	Large error
Open/Short	OK	OK	OK	Large error
Open/Short/Load	OK	OK	OK	OK

Figure 15. Table comparing relative accuracy of Cp-G measurements at 100 kHz and 1 MHz for different levels of capacitance compensation when using the high-voltage bias-T.

Note: The table shown in Figure 15 is based on the relatively large junction capacitances (on the order of nanofarads) that are typical of power MOSFETs.

Conclusion

Using the techniques explained in this application note, it is possible to directly measure MOSFET capacitances at voltages up to 3000V. All three of the data sheet MOSFET capacitance parameters (Ciss, Coss and Crss) can be directly measured using the B1505A and its high-voltage bias-T. This represents considerable improvement over the conventional methods to measure these same parameters, which typically require measuring a device's step response and extracting the value of capacitance from an RC time constant.

For the input capacitance (Ciss) measurement, care must be taken to ensure that properly sized bypass resistors and capacitors are used. In addition, unless you have the ability to perform load compensation on your system, you should restrict your maximum measurement frequency to no more than 100 kHz.

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Revised: July 8, 2010

Printed in USA, January 10, 2011
5990-7145EN

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