HEWLETT® PACKARD

MGA-64135 GaAs MMIC

Application Note G003

Introduction

The Hewlett-Packard MGA-64135 GaAs MMIC is a 50 Ω -matched gain block providing broadband operation from 1 to 10 GHz, with performance guaranteed from 2 to 6 GHz. It is housed in an inexpensive metal-ceramic 0.085-inch micro-X surface-mount-compatible package, and requires only a single-polarity power supply. The MGA-64135 combines the high frequency performance of GaAs with resistive feedback techniques proven in Hewlett-Packard's MODAMP silicon bipolar MMIC family.

Device Performance

The MGA-64135 is designed as a general purpose gain block to be used in a 50 Ω system. Device voltage is specified at 10 volts at a typical device current of 50 mA. Typical parameters at T_A = 25°C are as follows:

Frequency Range:	2.0 to 6.0 GHz
Power Gain:	12 dB
Gain Flatness:	±0.8 dB
Input VSWR:	1.5:1
Output VSWR:	1.4:1
Output Power at 1 dB Gain Compression:	+ 12 dBm
Noise Figure:	7.5 dB
Isolation:	35 dB

The expected gain variation over a -25°C to +85°C case temperature is typically ±0.5 dB.

MMIC Design

The basic topology of the MGA-64135 consists of a cascade of two GaAs FET feedback amplifier stages. As noted, feedback techniques are used throughout Hewlett-Packard's family of silicon bipolar MMICs. Although the use of feedback provides the same basic performance benefits in GaAs MMICs, the design of a GaAs FET feedback amplifier requires a slightly different approach. The bandwidth of a feedback amplifier is a function of the device transconductance gm, the ft of the device, and the series and shunt feedback elements. A major difference between the bipolar transistor and the FET is that the gm of the FET is substantially lower. Thus, it is not generally desirable to incorporate series feedback in a FET amplifier design, since it would lower gain to an unacceptable level. In the bipolar transistor, gm is a function of emitter current, whereas in the case of the FET, gm is proportional to gate width. Increasing the gate width of a FET to increase its gm and, hence, gain, has the drawback of increasing gate-to-source capacitance, which tends to cause a roll-off of high frequency gain. Therefore, obtaining a particular gain-bandwidth product in a GaAs FET amplifier is primarily a matter of selecting an appropriate gate width for the transistor and of adjusting the amount of shunt feedback. There is a limitation, however, in the choice of gate widths, since narrower gates generally produce a better input match at the expense of lower gain. Based on these tradeoffs, the MGA-64135 was designed around a 250-µm-gate-periphery FET in the first stage, providing about 4 dB gain, and a 350-µm FET in the second stage, providing about 8 dB of gain. Shunt feedback across each FET helps to set the match and gain-bandwidth product.

Designing an MMIC at microwave frequencies becomes more difficult when the MMIC is to be supplied in a package. The approach taken with the design of the MGA-64135 was to take the package parasitics into account when designing the chip. The result is flatter gain and better input and output match than would be obtained if package parasitics were neglected.

As with any packaged microwave semiconductor, additional parasitic reactances appear when the device is installed in a circuit board. When the MMIC is tested at the factory, a low-loss, high-frequency transistor test fixture is used, with a common-lead length of only several thousandths of an inch. In an actual operating circuit board, the common lead grounds are generally separated from the device by at least the thickness of the printed circuit board. Excessive inductance in the common leads will cause gain peaking to occur in the lower half of the band, while causing higher-frequency gain to decrease.

A unique feature of the MGA-64135 is its biasing arrangement. Whereas bipolar devices often have 4 to 8 V across the collector-to-emitter junction, the voltage across the drain-to-source junction of a FET is only 2 to 3 V. In the MGA-64135, advantage is taken of this low drain-to-source voltage by operating two FET devices in DC series to minimize current consumption. The circuit is arranged so that the source current of the second stage supplies the drain current of the first stage. The result is reduced DC power consumption compared to standard GaAs biasing techniques. The schematic diagram of MGA-64135 is shown in Figure 1.

In the MGA-64135, the operating voltage is applied to the output pin of the MMIC package, which connects to the drain of the second-stage FET. A portion of the second stage drain current flows through the

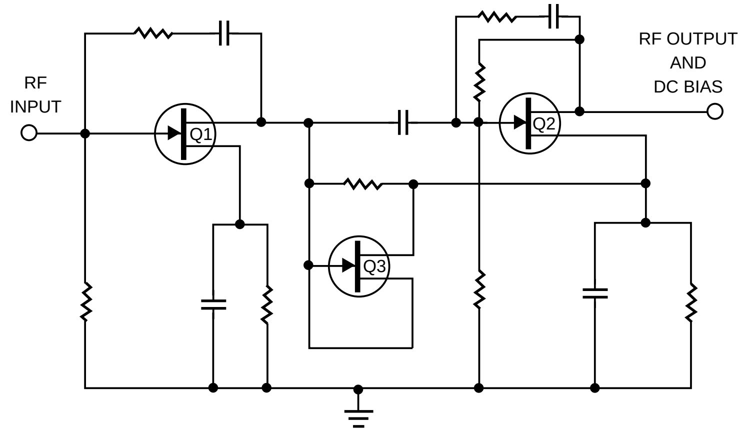

Figure 1. MGA-64135 Schematic Circuit

source resistor and a portion flows to the drain of the first stage through a third FET connected as a current source. The first-stage FET is then self-biased with another source resistor, with the gate of this FET at DC ground. A resistive voltage divider sets the voltage at the gate of the second-stage FET to achieve the desired bias point. Both source resistors are bypassed with capacitors to place the sources at RF ground.

The MGA-64135 is fabricated using Hewlett-Packard’s high-performance VPE material and nominal 0.3-µm recessed Schottky-barrier-gate lengths which result in approximately 160 mS gm and 1 pF Cgs per millimeter gate width. Gold metalization and silicon nitride passivation ensure a rugged, reliable device.

Circuit Layout

Package

The MGA-64135 is packaged in a four-lead surface-mount-compatible “micro-X” microstripline package as shown in Figure 2. Pin 1 is the RF input and is denoted by the slashed lead. Pin 3, the one opposite pin 1, is the RF output and also the DC input lead. Pins 2 and 4 are the ground leads.

A test circuit can be easily constructed using 50 Ω transmission lines on the input and output, a bias feed network, and DC blocking capacitors.

Circuit Board

To achieve the high frequency performance of which the MGA-64135 is capable, the device must be used in a microstrip or stripline circuit. A low-loss-dielectric PC board material such as Rogers Duroid™ or PTFE-woven glass is a must. Epoxy-glass PC materials are too lossy above several GHz and will severely degrade high frequency performance. Substrate thickness should be 0.031 inches or less so that common lead inductance is minimized.

In a microstrip circuit the device and RF conductors are on the top side of the board and the “real” RF ground plane is the bottom of the circuit board. Two or three plated through

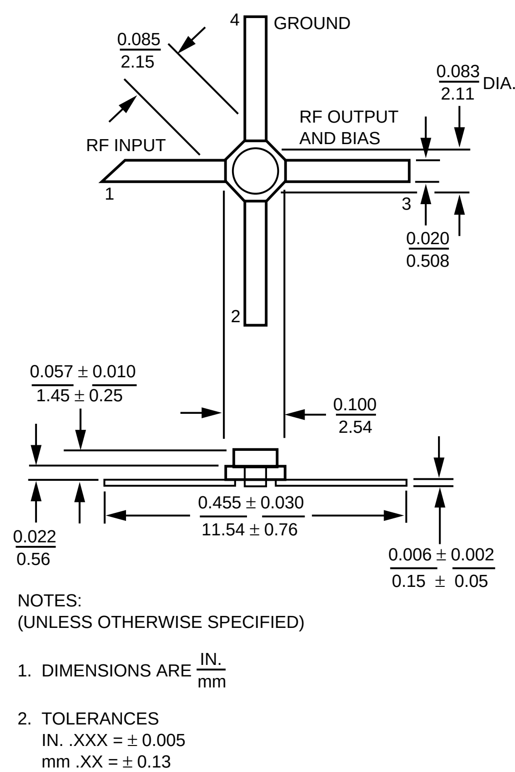

Figure 2. Hewlett-Packard 35 Micro-X Package

holes (vias) under each device ground lead will reduce the common lead inductance to an acceptable level.

Soldering the leads to the through-hole vias must be done with care, since a cold solder joint adds resistance to the ground return and will limit device performance. The solder must be allowed to flow all the way to the package body to minimize the lead inductance between the package and the attachment point.

The ratio of microstrip line width to board thickness is constant for a particular transmission line impedance and a particular substrate dielectric constant. The result is that the thinner dielectric material required for high-frequency operation will require a narrower line to achieve the required impedance. As an example, the width of a 50 Ω microstrip line on 0.020-inch-thickness Duroid 5880 is 0.060 inches, while with 0.031-inch-thick material of the same dielectric constant, the 50 Ω line width would be 0.093 inch. Choosing a 50 Ω line width of 0.020" will result in a minimum of electrical discontinuity when mating with the 0.020" wide leads of the MGA-64135. Since the device has a characteristic impedance of 50 Ω, the length of the 50 Ω microstripline is not critical. However, keeping the lines as short as possible will minimize resistive losses.

Bias Decoupling
DC bias must be supplied to the MGA-64135 through the RF output lead. This necessitates the use of a bias T arrangement at pin 3 in Figure 3. The bias T is simply a diplexer network which couples DC into the device via a low-pass network, and couples RF out of the device via a high-pass network. The low-pass network consists of an RF choke whose impedance is high at the RF frequency so that signal transfer from the device to the load is not restricted. The high-pass network is simply a chip capacitor which couples RF out, while providing a block to DC. A DC block is required to isolate each MMIC's DC bias network from adjacent stages. Although there is no voltage present at the input terminal, it is suggested that a blocking capacitor be used to protect the input of the first device from the voltage present on the preceding stage's output.

The blocking capacitors must be high-quality ceramic chip capacitors with minimal associated parasitics. For best operation in the 2 to 6 GHz frequency range, a capacitor in the 3 to 30 pF range is optimum. Values

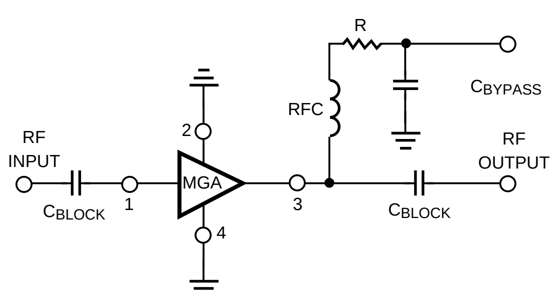

Figure 3. MGA-64135 Typical Biasing Configuration

below 3 pF present too high a series impedance, thereby degrading low frequency performance, while values higher than 30 pF tend to have associated parasitics that cause resonances and “gain suckouts” at frequencies above 2 GHz. 8.2 pF capacitors were used in the single-stage demonstration circuits while 22 pF capacitors were used in the dual-stage amplifiers.

The RF choke at pin 3 should present a high impedance to RF without introducing any in-band spurious responses. The miniature molded RF chokes are generally not low enough in value for the frequency of operation and therefore may have significant resonances in the band of operation. Version 1 of the demonstration circuit uses a 4-turn choke made from #30 AWG wire (0.01-inch nominal diameter) wound with an inner diameter of 0.050 inches. Keep the distance from the edge of the 50 Ω microstripline and the first turn of the RF choke to a minimum. A 33 Ω chip resistor in series with the RF choke will allow operation from a +12 volt power supply.

The 33 Ω series resistor limits the MMIC current to approximately 60 mA. The resistor also decreases the Q of the decoupling network making the circuit less susceptible to inband resonances. The other end of the resistor should be bypassed to ground with a high-quality 1000 pF chip capacitor. When cascading a series of MGA-64135s, use a 0.33 μH miniature molded RF choke between V_{dd} terminals of each stage. This will prevent crosstalk between bias circuits which could cause instabilities. Schematics of both single- and dual-stage amplifiers are shown in Figures 4 and 5.

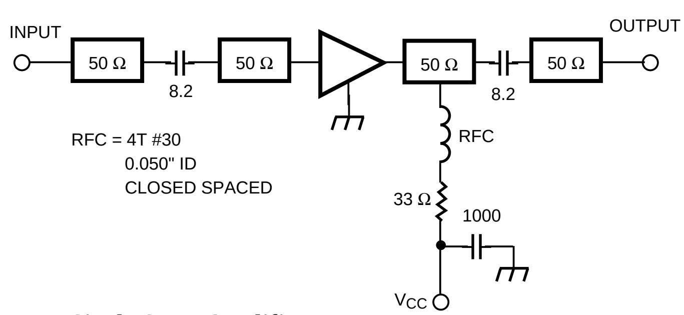

Figure 4. Single Stage Amplifier No. 1

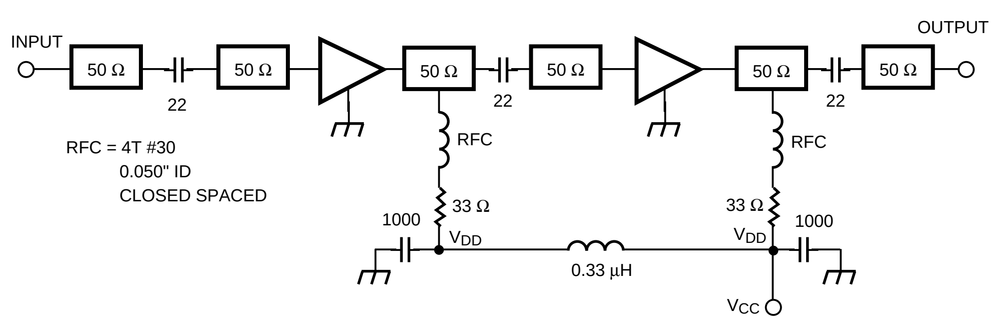

Figure 5. Dual Stage Amplifier

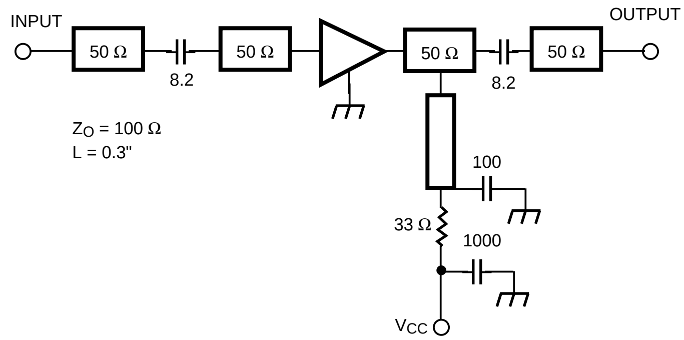

Figure 6. Single Stage Amplifier with Etched Microstripline

A second version of the microstrip board uses an etched microstripline as the series RF choke. A microstripline of 0.020 inches in width and 0.300 inches in length provides acceptable performance in the 2 to 10 GHz frequency range. A schematic of the demonstration amplifier using the etched microstripline is shown in Figure 6.

When the completed circuit board is installed in a housing, cavity-coupling effects can be critical. Although the MGA-64135 is unconditionally stable, it is best to limit the amount of gain appearing in a single normally-designed cavity between 30 to 35 dB. This means that a single cavity should contain two or, at most, three devices in cascade. If more gain is required, then an additional cavity can be used to contain another cascade of devices. As an additional precaution against instabilities, the use of low-profile components will help limit the radiation and pickup of stray RF.

Although not considered especially static-sensitive, handling of the MGA-64135 is done with the same precautions used with other GaAs devices. It is recommended that Electrostatic discharge procedures, as described in Hewlett-Packard Application Note AN-A004R, *Electrostatic Discharge Damage and Control*, be followed for both assembly and test.

Performance

Single-Stage Amplifier With Wound RF Choke

A plot of gain versus frequency for the single-stage amplifier using a wound RF choke is shown in Figures 7a and 7b. Gain of the completed amplifier is greater than 10 dB from 1 GHz to 6.4 GHz, and peaks at 14.0 dB at 3.85 GHz. Input return loss is greater than 9.5 dB from 1 GHz to 10 GHz. Output return loss is greater than 14.5 dB from 1 to 6.8 GHz. The measured noise figure on two demonstration amplifiers varied from 7.7 dB to 8.3 dB from 2 to 6 GHz. Noise figure at 10.4 GHz was still only 8.3 to 8.9 dB. The TOUCHSTONE™ simulation for this amplifier design appears in Tables 1a and 1b.

The measured 1 dB gain compression point showed a 1 dB degradation as temperature was increased from -25°C to +85°C. Through 4 GHz the gain variation over temperature was less than ±0.3 dB, while at 6 GHz the gain varied ±0.6 dB. A plot showing typical 1 dB gain compression and gain data at 4 GHz over temperature is shown in Figure 8.

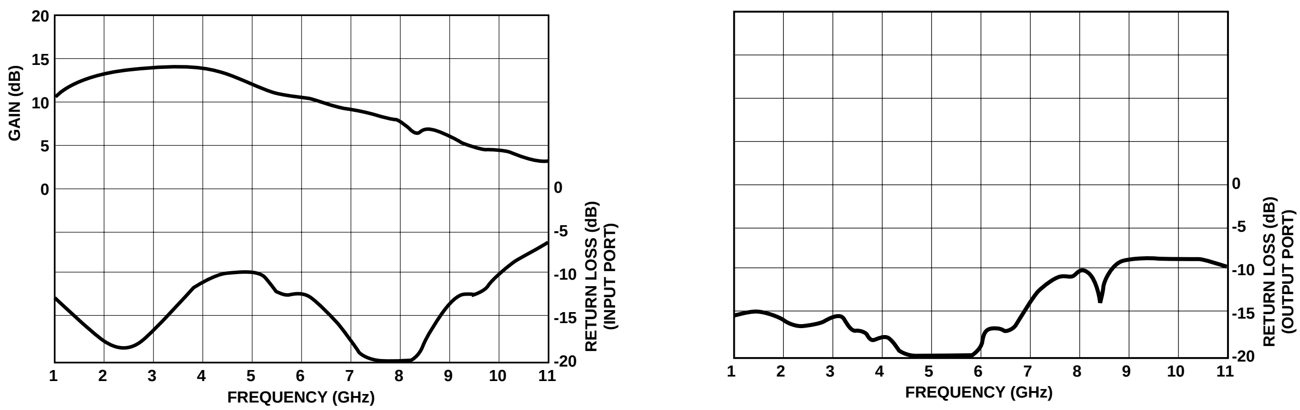

Figure 7a and Figure 7b. MGA-64135 Amplifier #1

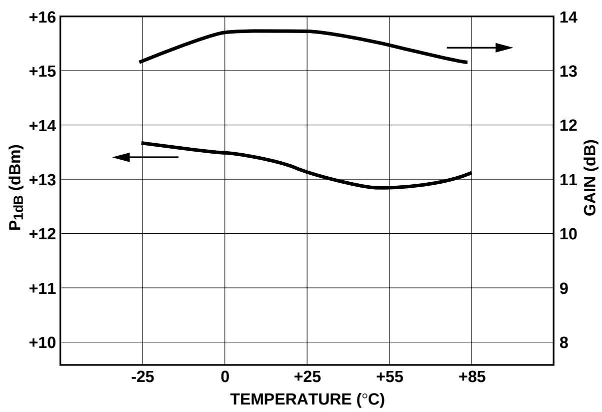

Figure 8. P_{1dB} and Gain vs. Temperature at 4 GHz

Table 1a. Single Stage Amplifier with Wound Inductor (simulation)

FREQ (GHz)	dB[S21]	dB[S12]	dB[S11]	dB[S22]	K	B1
0.10	-12.276	-50.099	-1.104	-0.631	19.264	0.241
0.50	7.512	-34.249	-5.974	-14.327	7.907	1.198
1.00	12.048	-34.418	-10.028	-16.334	5.825	1.067
2.00	14.344	-35.984	-15.421	-22.330	5.867	1.017
3.00	14.761	-38.891	-15.849	-23.897	7.843	1.017
4.00	14.275	-38.938	-12.935	-19.950	8.087	1.034
5.00	13.390	-37.509	-12.243	-19.074	7.518	1.039
6.00	12.415	-36.388	-15.841	-18.435	7.616	1.007
7.00	11.372	-33.485	-28.187	-13.939	6.152	0.955
8.00	10.137	-31.883	-16.074	-11.580	5.630	0.940
9.00	8.651	-27.500	-9.242	-12.274	3.751	1.025
10.0	7.311	-27.327	-5.923	-12.930	3.533	1.193
11.0	5.421	-27.929	-3.639	- 10.291	3.322	1.315

Table 1b.

```
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DIM
         FREQ GHZ
         IND  NH
         CAP  PF
         LNG  IN

VAR
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CKT
         MSUB  ER=2.2  H=.020  T=.0014  RHO=1  RGH=0
         TAND  TAND=.003
         MLIN  1    2   W=.060  L=.22
         SLC   2    3   L=.5  C^C1
         MLIN  3    4   W=.060  L=.25
         MSTEP 4    5   W1=.060  W2=.020
         MLIN  5    6   W=.020  L=.005
         S2PA  6    7   8   C:\S_DATA\GAMMIC\MGA64135.S2P
         MLIN  8   30   W=.020  L=.005
         VIA   30   0   D1=.030  D2=.030  H=.020  T=.001
         MLIN  30  31   W=.060  L=.080
         VIA   31   0   D1=.030  D2=.030  H=.020  T=.001
         MLIN  8   35   W=.020  L=.005
         VIA   35   0   D1=.030  D2=.030  H=.020  T=.001
         MLIN  35  36   W=.060  L=.080
         VIA   36   0   D1=.030  D2=.030  H=.020  T=.001
         IND   12   20   L=15
         SRL   20   21   R=33  L=.5
         MLIN  21   22   W=.2  L=.2
         SLC   22    0   L=1  C=1000
         MLIN  7    10  W=.020  L=.005
         MSTEP 10   11  W1=.020  W2=.060
         MLIN  11   12  W=.060  L=.100
         MLIN  12   13  W=.060  L=.150
         SLC   13   14  L=.5  C^C1
         MLIN  14   15  W=.060  L=.25
         DEF2P 1    15  MGACKT


FREQ
        !SWEEP  .1   1   .1
         STEP   .1
         STEP   .5
         SWEEP  1   11   1
        !SWEEP  1   6  .5

OUT
         MGACKT  DB[S21] GR1
         MGACKT  DB[S12] GR2
         MGACKT  DB[S11]
         MGACKT  DB[S22]
         MGACKT  K
         MGACKT  B1
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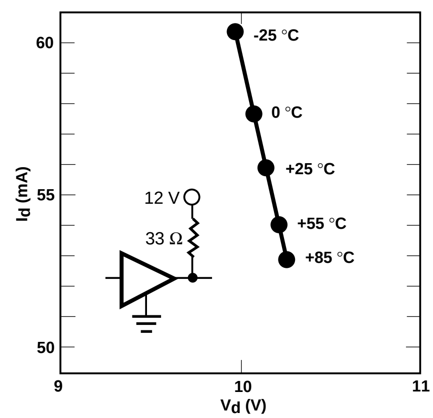


Figure 9. Measured V_d and I_d vs. Temperature

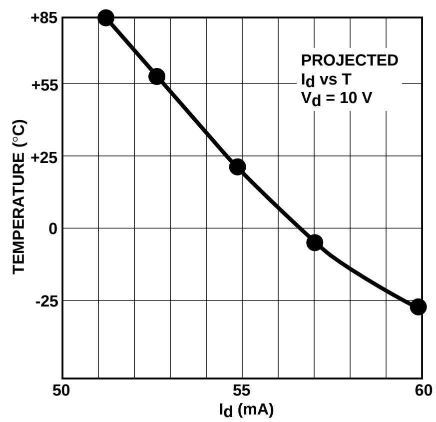
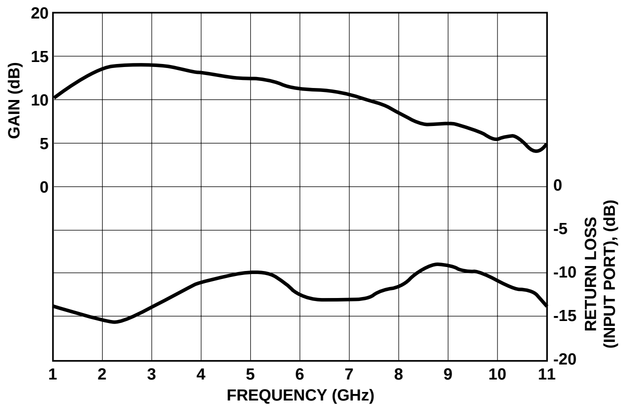


Figure 10.

Each of the demonstration amplifiers incorporates a 33 Ω resistor to allow it to operate from a 12 VDC power source. The graph in Figure 9 shows that the bias current varies only ±4 mA over the range of -25 to +85°C. The projected current variation over temperature if the output terminal were held at 10 volts is shown in Figure 10 to be less than ±4.5 mA.

Single-Stage Amplifier With Etched RF Choke

The performance of the second version of the single-stage amplifier, using an etched microstripline RF choke, is shown in Figures 11a and 11b. In the 2 to 6 GHz frequency range, the performance of the amplifier using the etched RF choke amplifier is comparable to the version using the wound choke. The microstripline RF choke does provide superior performance at frequencies above 6 GHz, while the wound RF choke offers a slight improvement at frequencies below 2 GHz. A TOUCHSTONE™ simulation for this amplifier design appears in Tables 2a and 2b.



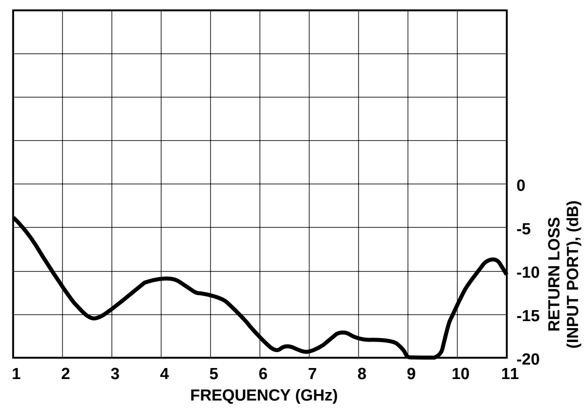


Figure 11a and Figure 11b. MGA-64135 Amplifier with Etched Inductor

Table 2a. Single Stage Amplifier with Etched RF Choke (simulation)

FREQ (GHz)	dB[S21]	dB[S12]	dB[S11]	dB[S22]	K	B1
0.10	-20.689	-58.512	-1.015	-0.115	25.542	0.047
0.50	-3.205	-44.966	-6.270	-0.267	5.793	0.074
1.00	9.624	-36.842	-11.770	-2.919	5.083	0.536
2.00	13.916	-36.412	-15.773	-9.431	5.768	0.906
3.00	14.548	-39.104	-16.052	-12.541	7.810	0.964
4.00	14.158	-39.055	-12.980	-14.223	8.076	1.005
5.00	13.394	-37.505	-12.207	-18.499	7.497	1.038
6.00	12.199	-36.684	-16.077	-15.973	8.067	0.996
7.00	10.906	-33-952	-29.770	-11.325	6.608	0.922
8.00	9.547	-32.474	-15.914	-8.713	5.999	0.874
9.00	7.879	-28.272	-9.695	-8.067	4.033	0.917
10.0	6.037	-28.602	-6.544	-6.549	3.898	0.977
11.0	2.814	-30.537	-3.507	-3.911	3.877	0.869

Table 2b.

```
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              64135B.CKT    Wed Aug 01 13:39:13 1990

DIM
        FREQ GHZ
        IND  NH
        CAP  PF
        LNG  IN

VAR
        C1=8.2

CKT
        MSUB  ER=2.2  H=.020  T=.0014  RHO=1  RGH=0
        TAND  TAND=.003
        MLIN  1   2   W=.060  L=.22
        SLC   2   3   L=.5  C^C1
        MLIN  3   4   W=.060  L=.25
        MSTEP 4   5   W1=.060  W2=.020
        MLIN  5   6   W=.020  L=.005
        S2PA  6   7   8   C:\S_DATA\GAMMIC\MGA64135.S2P
        MLIN  8   30  W=.020  L=.005
        VIA   30  0   D1=.030  D2=.030  H=.020  T=.001
        MLIN  30  31  W=.060  L=.080
        VIA   31  0   D1=.030  D2=.030  H=.020  T=.001
        MLIN  8   35  W=.020  L=.005
        VIA   35  0   D1=.030  D2=.030  H=.020  T=.001
        MLIN  35  36  W=.060  L=.080
        VIA   36  0   D1=.030  D2=.030  H=.020  T=.001
        MLIN  12  20   W=.020  L=.3
        SLC   20   0   L=.5  C=100
        SRL   20  21   R=33  L=.5
        MLIN  21  22   W=.2  L=.2
        SLC   22   0   L=1  C=1000
        MLIN  7   10  W=.020  L=.005
        MSTEP 10  11  W1=.020  W2=.060
        MLIN  11  12  W=.060  L=.100
        MLIN  12  13  W=.060  L=.150
        SLC   13  14  L=.5  C^C1
        MLIN  14  15  W=.060  L=.25
        DEF2P 1   15  MGACKT

FREQ
       !SWEEP  .1   1   .1
        STEP  .1
        STEP  .5
        SWEEP  1   11   1

OUT
        MGACKT  DB[S21]
        MGACKT  DB[S12]
        MGACKT  DB[S11]
        MGACKT  DB[S22]
        MGACKT  K
        MGACKT  B1
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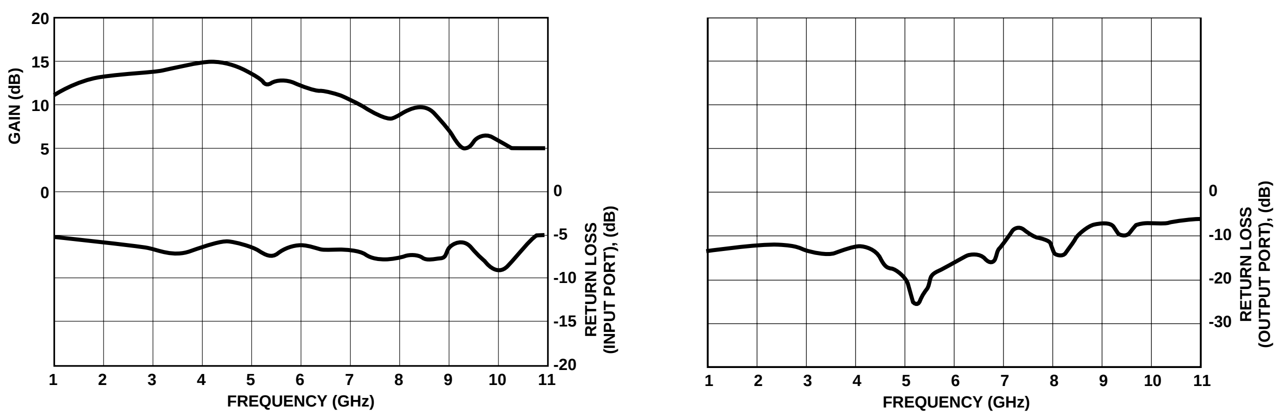


Figure 12a and Figure 12b. Dual-Stage MGA-64135 Amplifier

Dual-Stage Amplifier

The performance of the two-stage amplifier shows the “cascadability” of the MGA-64135. A high-performance broadband amplifier with unconditional stability can be built with only a few components. A plot of gain versus frequency is shown in Figures 12a and 12b. In the curve, gain peaks at 29 dB at 4 GHz. Input and output return loss is greater than -11 dB from 1 to 7 GHz. Noise figure of the cascade measured 8.0 dB at 2 GHz, 8.65 dB at 3.5 GHz and 7.3 dB at 6 GHz. Somewhat lower noise figure, i.e. 0.5 dB lower, can be obtained at slightly lower device voltage. At the lower voltage, however, gain will be about 1 dB lower.

Narrow-band Optimization

In the frequency range of 2 to 6 GHz little improvement in gain can be expected by using a matching network external to the device. As shown in the S parameters, the worst case S11 is only 0.2, which corresponds to a mismatch loss of about 0.18 dB. Providing an external match on both the input and output would result in an increase in small signal gain of only 0.36 dB. However, at 10 GHz, matching both the input and output could provide a gain improvement of 0.9 dB.

Effect of Common-lead Grounding

The requirement for a low-inductance common-lead path to ground has already been addressed, but its effect cannot be overemphasized. The simulated swept frequency plots shown in Figures 13 and 14 show the effect of inductance on both gain and reverse isolation for the single-stage amplifier using a wound RF choke. The plots were generated by varying the value of inductance in each device lead. Note that 0.1 nH of lead inductance in each lead can increase passband ripple over the 2 to 6 GHz frequency range from ±1 dB to ±1.5 dB. As Figure 14 shows, excessive common-lead inductance will decrease reverse isolation, which will result in an amplifier that is only conditionally stable. The plot in Figure 15 compares the gain of the MGA-64135 device by itself to the gain of the completed amplifier, including the bias decoupling networks and the effect of two plated through holes connecting each common lead to the bottom groundplane.

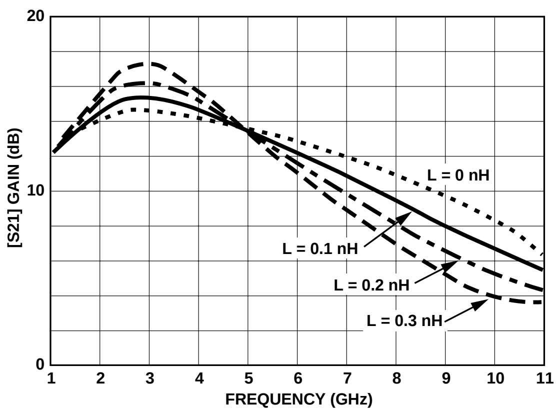


Figure 13. MGA-64135 Amplifier Gain vs. Common Lead Inductance

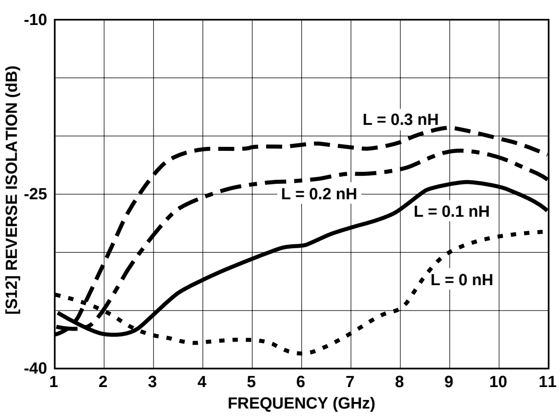


Figure 14. MGA-64135 Amplifier Reverse Isolation vs. Common Lead Inductance

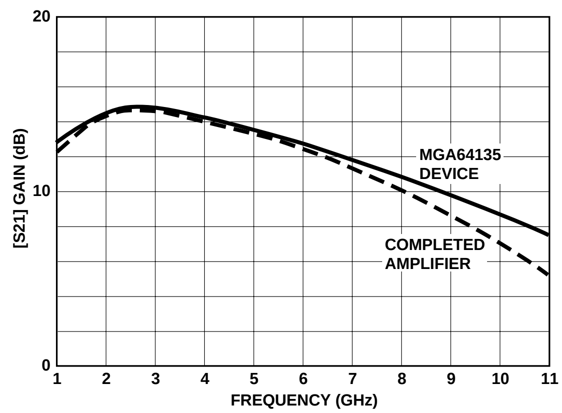


Figure 15. MGA-64135 Device Compared to Completed Amplifier

Other Applications

Limiting Amplifier

Driving the MGA-64135 into saturation indicates the possibility of several nonlinear applications, including use as a limiting amplifier or as a harmonic generator.

At 2 GHz, the MGA-64135 amplifier saturates at an input level of about +10 dBm. Saturated power output is typically +16 dBm. Increasing the input level to the suggested maximum CW RF input level of +13 dBm causes no further increase in output power, making the device practical for limiting amplifier applications. At an input power level of +13 dBm, the second harmonic output is -16 dBc. The complete spectral display of the harmonic output is shown in Figure16.

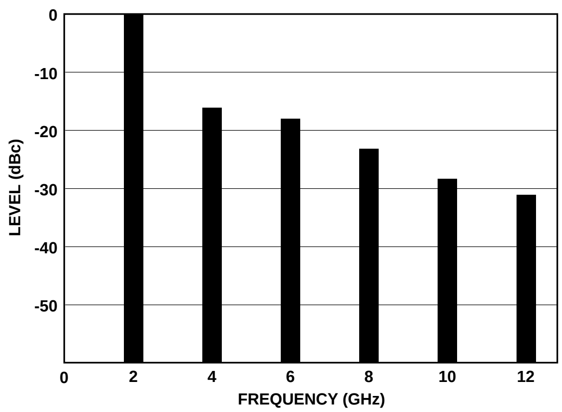


Figure 16. Spectral Output from MGA-64135 Amplifier when driven at 2 GHz at an input power level = +13 dBm, I_d = 55.8 mA, T_A = +25°C

Frequency Multiplier

When terminated in 50 Ω, the MGA-64135 has been shown to exhibit excellent harmonic rejection when driven into saturation. Using the MMIC as a multiplier is accomplished by terminating the output of the MMIC in a bandpass filter. An appropriate bandpass filter will pass the desired harmonic, and reflect all other undesired harmonics, including the fundamental frequency, back into the MMIC at the proper phase angle to accent the desired harmonic. The electrical length between the MMIC and filter is very important for proper multiplier operation.

To evaluate the MGA-64135 as a multiplier, the simple setup shown in Figure 17 was constructed. Conversion loss as a times-2 multiplier from 3 to 6 GHz measured 2.0 dB at an input power level of +10 dBm. Increasing the input level to +13 dBm increased the second harmonic level from +8 dBm to +10.6 dBm. The measured power output levels were corrected for the measured loss of the bandpass filter. The results of using the MGA-64135 as a times-3 multiplier were not as good, displaying an 11.8 dB conversion loss in multiplying from 2 to 6 GHz.

The results are sensitive to the phasing between the MMIC and bandpass filter, and could be improved by use of a line stretcher

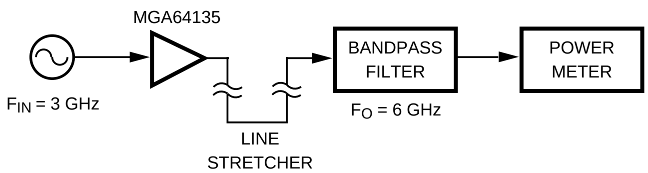


Figure 17. Multiplier Test Setup

between the MMIC and the bandpass filter. The amount of improvement depends on the RF drive level and the frequency of the desired harmonic. Useful upper frequency range is usually limited to the frequency at which the gain has dropped 3 dB from midband or approximately 7 to 8 GHz.

Frequency Converter

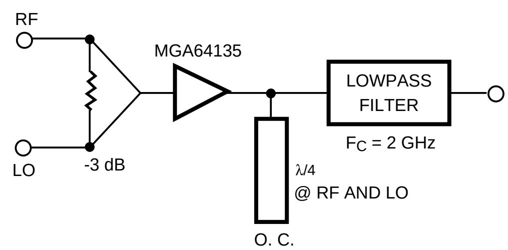
Another nonlinear property of the MGA-64135 is its ability to operate as a frequency converter. When driven by a fairly strong local oscillator signal (i.e., +6 dBm), the MGA-64135 functions as a mixer, providing either up-conversion or down-conversion depending on the application.

The MGA-64135 was tested as a single-ended down-converter, with both the LO and RF signals injected into the input port via a broadband power combiner. The IF is taken off the output port. A simple test setup is shown in Figure 18. RF is at 6 GHz, LO at 5 GHz at a level of +6 dBm measured at the input to the mixer.

Measurements indicate that a device voltage of 8 volts was optimum for lowest noise figure. A quarterwave open-circuited stub on the microstrip board at the output of the device provides a virtual short to both the RF and LO at the output of the device. The result is a 1 dB improvement in conversion gain.

It would also appear to be desirable to place a short at the IF frequency at the input of the device to enhance conversion gain. This was, however, not attempted with the demonstration mixer. Without any further tuning, 0 dB conversion gain was obtained with an SSB noise figure of 15.8 dB. Somewhat improved conversion gain is expected at higher IFs, (i.e., 2 GHz), since device gain is about 2 dB higher. The expected improvement is similar to the increase in gain. The device should work well for up-conversion at frequencies as high as 6 to 7 GHz.

The MGA-64135 has other potential applications such as oscillators, self oscillating mixers, and frequency dividers. Bias current and drive levels can be optimized for a particular application.



RF	6 GHz
LO	5 GHz @ +6 dBm @ MIXER INPUT
IF	1 GHz
V_{CC}	8 V
I_{CC}	48 mA
C_G	0.0 TO 0.5 dB FOR MIXER
NF_{SSB}	15.8 dB @ MIXER INPUT

Figure 18. Mixer Test Setup

Conclusion

The MGA-64135 should find many uses in telecommunications systems and test equipment. It will provide good gain and medium power output in the 1 to 8 GHz frequency range in a low cost microwave package. The information presented in the Other Applications section of this note indicates that performance as a limiting amplifier, frequency multiplier or frequency converter is also promising.

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