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Designing with HMMC-5021, -5022, -5026 and -5027 GaAs MMIC Amplifiers

Application Note # 1053, Rev A

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1.0 Introduction

This application note gives a technical overview of the HMMC-5021, HMMC-5022, HMMC-5026, and HMMC-5027 GaAs MMIC Traveling Wave Amplifiers (TWA). As a group, these amplifiers cover 2 to 26.5 GHz with small signal gains of 8.5 dB, P_{1dB} compression up to 22 dBm at 20 GHz, and 19 dBm at 26.5 GHz. The HMMC-5021/22/26 models represent three different RF screening levels of the same GaAs MMIC amplifier. The HMMC-5021 has typical RF specifications, the HMMC-5022 has guaranteed RF specifications up to 22 GHz, and the HMMC-5026 is guaranteed up to 26.5 GHz. Also discussed in this application note is the HMMC-5027 GaAs MMIC amplifier, which is a high power version of the HMMC-5026.

These MMIC amplifiers also have two very useful design features: variable gain control and a low end frequency response that can be extended down into the kHz range using external components. A detailed discussion of these topics and how to properly bond and bias the amplifiers will be covered in this application note.

2.0 Device Schematic and Topology

The device topology and schematic for the HMMC-5026 and HMMC-5027 are shown in Figures 1 and 2, respectively. The HMMC-5021, HMMC-5022, and HMMC-5026 are all structurally the same and the bonding and biasing techniques that apply to HMMC-5026 also apply to the other two. Each GaAs MMIC amplifier is a cascade of seven cascode stages. The cascode amplifiers in the HMMC-5026 use two 124 µm gate-width FETs and the HMMC-5027 uses two 248 µm gate-width FETs. The larger gate periphery on the HMMC-5027 provides about 2.5 dB more output power (19 dBm typical) and slightly less gain than the HMMC-5026 (7.5 dB vs. 9.3 dB) at 26.5 GHz.

Refer to the HMMC-5026 schematic in Figure 1 for the following discussion. The RF input drives the lower FET of each stage of the MMIC amplifier from a series of transmission lines known as the “gate line.” The gate line is terminated in 50Ω to ground through a 10.8 pF capacitor and includes a resistor network through which the gate bias (V_{GG}) is fed into the amplifier. This resistor network also includes an additional bonding pad (labeled Auxiliary Gate) that can be used with an eternal capacitor to extend the lower frequency range of the amplifier. This topic will be covered in detail later.

The RF output is connected, via the “drain line,” to the drains of the upper FETs of each stage and is terminated in a 50Ω resistor. In this case, the terminated end of the 50Ω resistor utilizes a special network that includes a shunt 1.0 pF capacitor connected to another shunt 8.1 pF capacitor through a 15Ω resistor. The drain line termination also incorporates a resistive divider network which is used to set the operating bias point for the top row of FETs. This resistor network also includes an additional bonding pad (labeled Auxiliary Drain) that can be used with an external capacitor to extend the lower frequency range of the amplifier.

The schematic of the HMMC-5027 is similar to that of the HMMC-5026 with the exception of the gate line configuration. The HMMC-5027

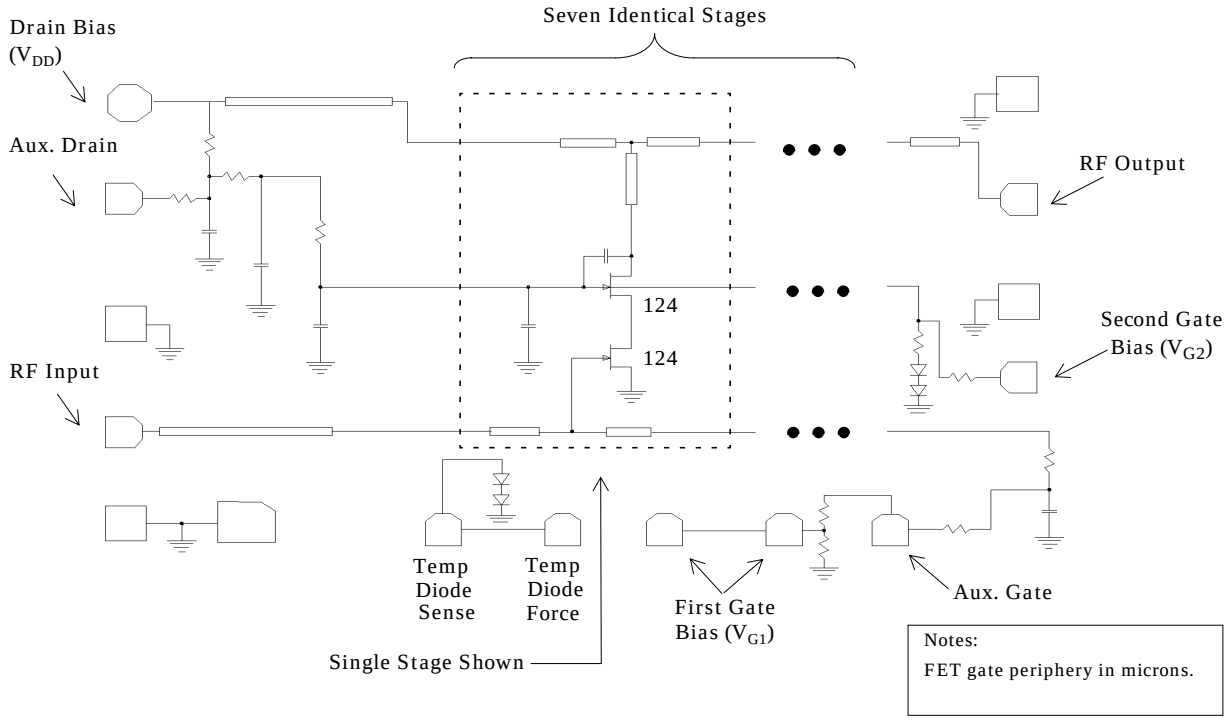
incorporates two gate lines. The first is an RF path which drives the lower FET of each stage and is terminated in 50Ω. A bias gate line is used to feed DC bias to each FET through 15KΩ resistors and is terminated in 30 KΩ to ground.

The bonding pads for the HMMC-5026 and HMMC-5027 are also shown in Figures 1 and 2. The size of the DC bias pads is slightly larger than the RF pads to facilitate bonding. Adjacent to the RF input and output pads are additional ground pads which are only used during initial device testing. No bonds to these pads are required for normal operation since RF and DC ground is provided on chip by conductive vias. Each device has a unique chip I.D. which can be used to track a given device and provide a reference for the device location on the wafer.

Using the simplest form of bonding, the HMMC-5026 are HMMC-50027 amplifiers will provide excellent RF performance over the full 2 to 26.5 GHz frequency range. The next sections describe how to properly bond and bias the amplifiers to get optimum performance.

3.0 Bonding the TWA

Only two RF and two DC bonds are needed for normal operation of the amplifiers. The RF bonds should be made with 500 line/inch gold mesh[1] to both the RF input and output pads on



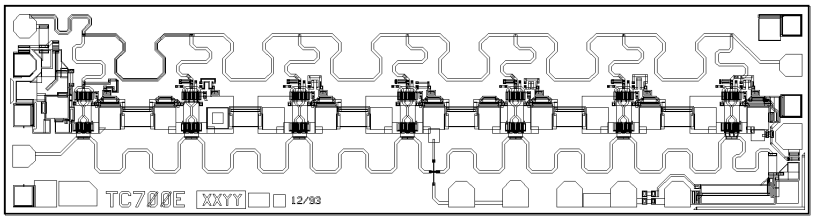
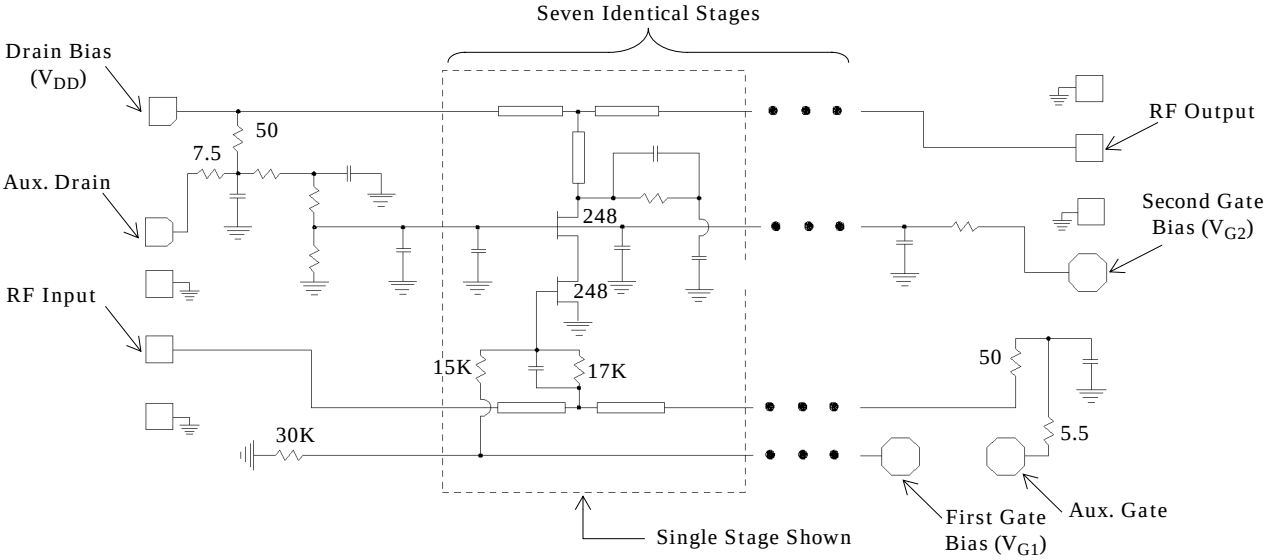


Figure 1. HMMC-5021/22/26 TWA Schematic and Topology.

the TWA. These bonds should be kept as short as possible to reduce the RF lead inductance. Single 0.7 mil diameter gold wire may be used in place of the RF mesh bond, however, high frequency performance (>20 GHz) will degrade slightly due to the increased inductance. Specifically, gain will decrease and input/output return loss will degrade slightly.

The two DC bonds required include the GATE BIAS (V_{GG}) and DRAIN BIAS (V_{DD}) bonds (Figure 1). The gate bias is used to control the drain current (I_{DD}) of the device. The length of the gate bond wire is not critical because an on-chip decoupling circuit isolates the cascode stages of the MMIC amplifier from the external gate bias network. The gate bond wire is normally made short to insure mechanical rigidity. In cases where the bond wire must span great distances, small bonding islands can be used to split the length into shorter loops. Gate bias should only be applied using the GATE BIAS (V_{GG}) bond pad as shown in Figure 1. Although gate bias can be fed into the device through the AUX GATE or RF INPUT pads, doing so will circumvent the on-chip protection circuit, designed to prevent

1. Buckbee-Mears Co., St. Paul, MN, (612-228-6400)



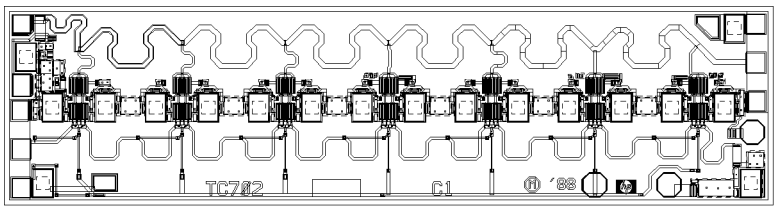


Figure 2. HMMC-5027 TWA Schematic and Topology.

excessive gate current under saturating RF drive levels, and therefore is not recommended.

On the HMMC-5026, this circuit consists of a series 550Ω and a shunt 550Ω resistor. On the HMMC-5027 the combination protection/decoupling circuit consists of series 15KΩ resistors between the gate bias line and the gates of each FET, and a shunt 30KΩ resistor which terminates the gate bias line. The length of the drain bias bond wire will affect the RF performance of the TWAs and is discussed in detail in the section entitled, "Drain Inductance." Drain bias should be applied to the amplifier using **only** the DRAIN Bias paid (V_{DD}). The transmission line between the drain bias pad and the first two stages has been reinforced with thicker gold to prevent electromigration due to DC current. Although it is possible to apply the drain voltage (V_{DD}) to the amplifier through the RF OUTPUT pad, this would bypass the protection against electromigration that is designed on the MMIC amplifier. Bonding to this pad is especially important on the HMMC-5027 which operates at a high bias current (typically 250 mA). No bonds are required to any other pads for 2 to 26.5 GHz performance.

A typical bonding configuration for 2 to 26.5 GHz operation is shown in Figure 3. The device is die-attached to a gold-plated molybdenum shim using a fluxless solder process. The suggested thin film circuits include 50 pF capacitors in series with the 50 Ω line. The lengths of the thin film circuits should be kept as short as possible for best return loss performance. All DC bonds may be made using 0.7 mil diameter gold wire with the exception of the drain bias bond on the HMMC-5027. The current drawn by the HMMC-5027 (typically 250 mA) would stress and possibly fuse a long length of 0.7 mil diameter gold wire. The fusing current for pure gold bond wire is inversely proportional to the length of the bond. Table 1 lists the fusing current for various

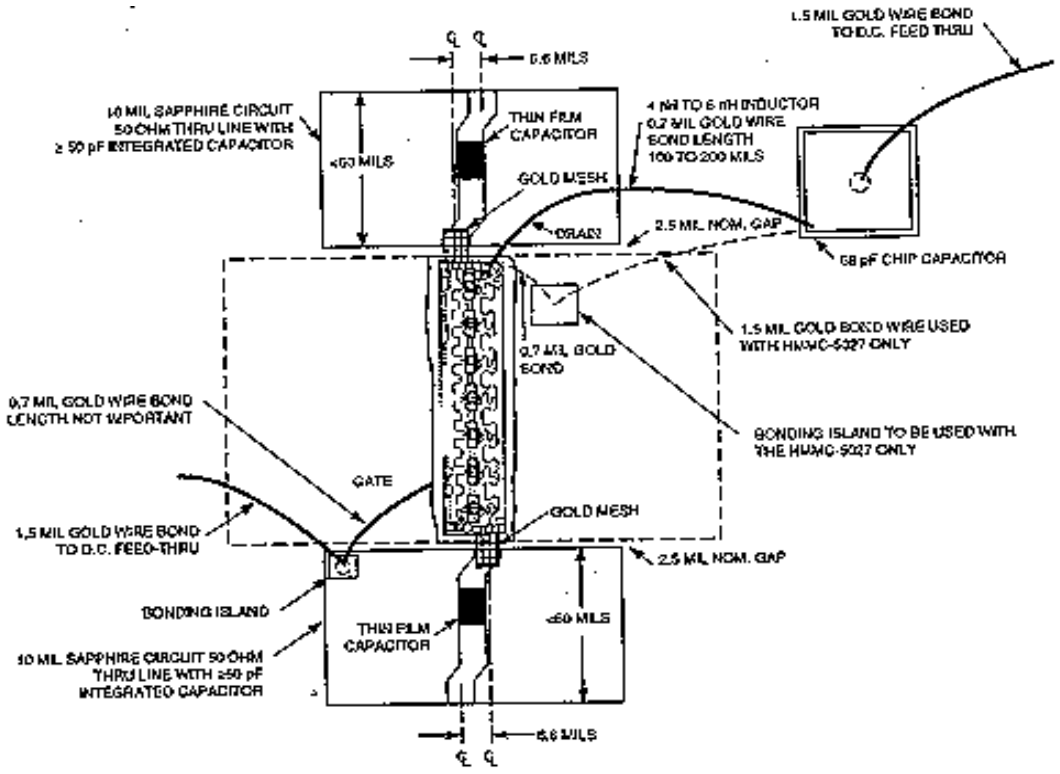


Figure 3. Typical Bonding Configuration for 2 to 26.5 GHz Operation.

pure gold bond wire diameters as a function of the bond wire length.

Table 1: Fusing Currents for Pure Gold Bond Wire.

Fusing Current (mA)			
Length (mils)	Wire Diameter		
	0.7 mil	1.0 mil	1.5 mil
50	800	1800	4700
100	450	1200	3300
200	250	750	2500
300	170	580	2100

Table 1 shows that a 1.5 mil diameter wire will easily handle the current of the HMMC-5027, but the drain bond pad is too small to directly bond a 2.5 mil wire onto it. A different bonding scheme is required to accommodate the larger diameter bond wire. When assembling a HMMC-5027, a low capacitance fused silica or alumina bonding island should be epoxied as close as possible to the drain bias pad of the HMMC-5027. Then a short 0.7 mil diameter gold wire bond can be added between the bias pad and the bonding island. Due to the short length of the bond it will not fuse open. A long 1.5 mil bond may then be added between this island and the chip capacitor. The long length of this bond provides enough inductance to guarantee a good match to frequencies below at least 2 GHz. A more general discussion of die-attach, bonding, and handling of GaAs MMICs can be found in application note 999, “GaAs MMIC Assembly and Handling Guidelines.”

4.0 Biasing the TWA

The proper DC biasing technique for the TWA is similar to that of a discrete FET. A negative voltage is required for the gate bias and a positive voltage is required for the drain bias.

Table 2 shows the recommended continuous operating bias values for both the HMMC-5026 and HMMC-5027. The simplest method for providing the bias to the TWA is to use two separate supplies; one positive and one negative. The positive supply must be able to supply enough current to meet the operating conditions specified in Table 2. Figure 4 shows a simple biasing setup which allows convenient monitoring of voltages and currents for the gate and drain.

Table 2: Recommended Operating Bias Conditions

Parameter	HMMC-5026	HMMC-5027	Units
V_{DD}	7.0	8.0	volts
I_{DD}	150	250	mA
V_{GG}	~-0.25	~-0.4	volts
I_{DSS}	200	350	mA

The recommended technique for applying bias to the GaAs MMIC amplifiers is outlined below. It assumes that the amplifier is assembled into an evaluation package with bonds connecting the device to external DC feedthru pins.

1. Connect the amplifier ground to the power supply commons before connecting the gate and drain leads. Be sure the voltages on both supplies are set to ZERO and any RF input signal is removed.
2. Connect the gate lead and then the drain lead to the package bias pins.
3. Slowly increase the negative gate voltage (V_{GG}) to about -2 volts. This should be enough negative potential to insure the device is in pinch-off.
4. Increase the drain voltage (V_{DD}) to +7 volts for the HMMC-5026, or +8 volts for the HMMC-5027.
5. Decrease the gate voltage (i.e., less negative voltage) until the drain current (I_{DD}) is 150 mA for the HMMC-5026, or 250 mA for the HMMC-5027.

5.0 Extended Low Frequency Performance

The TWAs can operate down to frequencies as low as a few hundred kilohertzs with a few simple modifications to the standard assembly of Figure 3.

The low frequency performance of the TWA can be extended by doing the following:

A. Add external capacitors to the Auxiliary Gate (Aux Gate) and Auxiliary Drain (Aux Drain) bonding pads.

B. Increase the capacitance of the DC blocking capacitors (C_{DC}) at the RF input and output ports.

C. Increase the inductance of the drain inductor (L_D).

All three factors are equally important since any one can limit the low frequency performance. The following sections discuss how to select these components for low frequency response.

6.0 Auxiliary Drain and Gate Bypass Capacitors

The ability to extend the low frequency of the HMMC-5026 and HMMC-5027 is largely possible due to two features designed into the TWAs: access to both the drain and gate on-chip bypass capacitors using the AUX GATE and AUX DRAIN bond pads. Several low frequency performance characteristics are affected by the addition of external circuitry to these pads and only the most significant characteristics are described here. Specifically, gain peaking around 1 to 1.5 GHz and improvement in the input/output return loss and gain at frequencies below 2 GHz are discussed.

The drain and gate lines on the HMMC-5026 and HMMC-5027 are terminated with a on-chip 50Ω resistor to ground through on-chip capacitors ranging in value from 1 pF to 10 pF. Below about 2 GHz, these small capacitors are poor RF shorts. Input and output return loss degrades as the drain and gate line loads deviate from 50Ω. The loads can be restored to about 50Ω, and RF performance improved, by adding large external capacitors (C_{AUX}) in parallel with the on-chip capacitors as shown in Figure 5. The capacitors must be attached from the AUX GATE bonding pad to ground and from the AUX DRAIN bonding pad to ground.

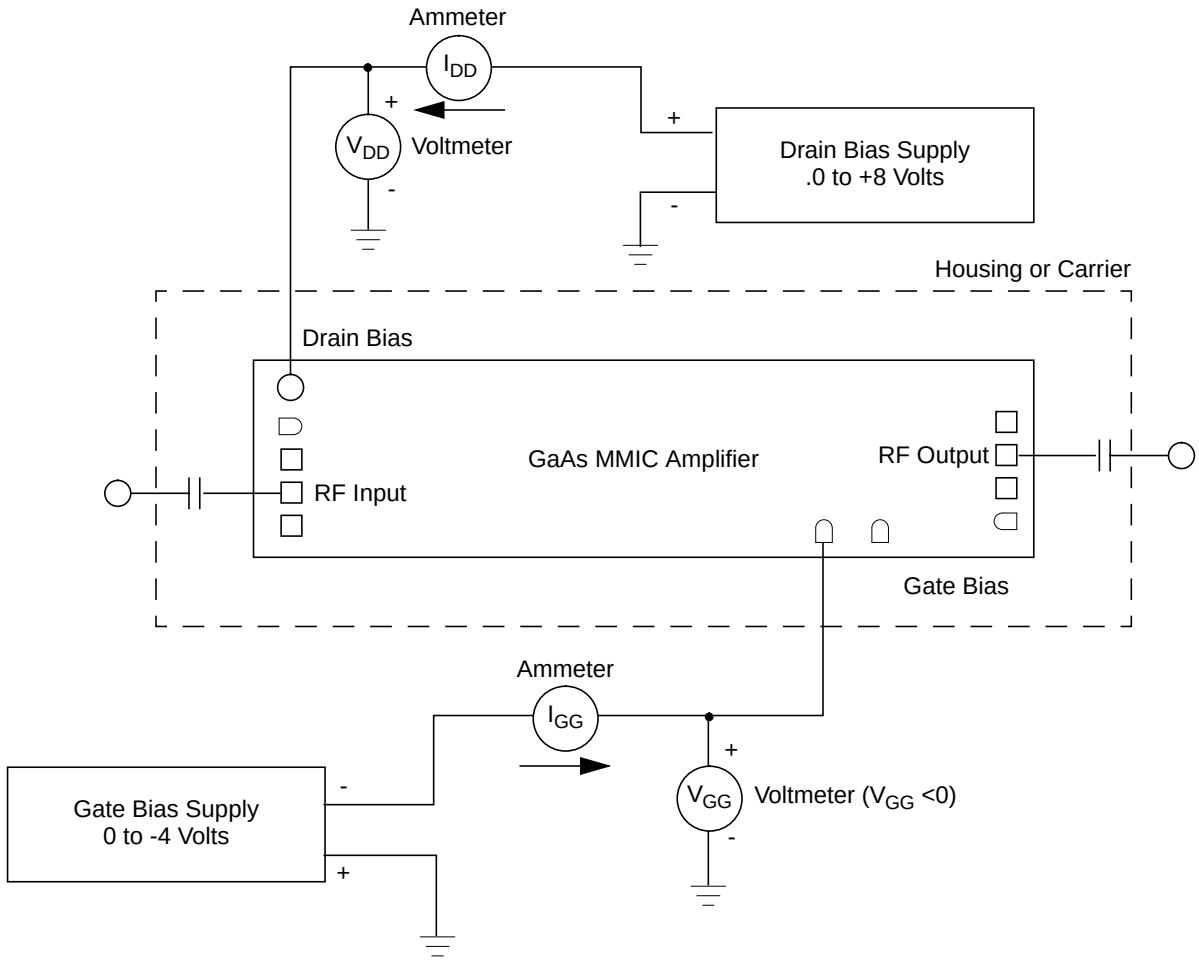
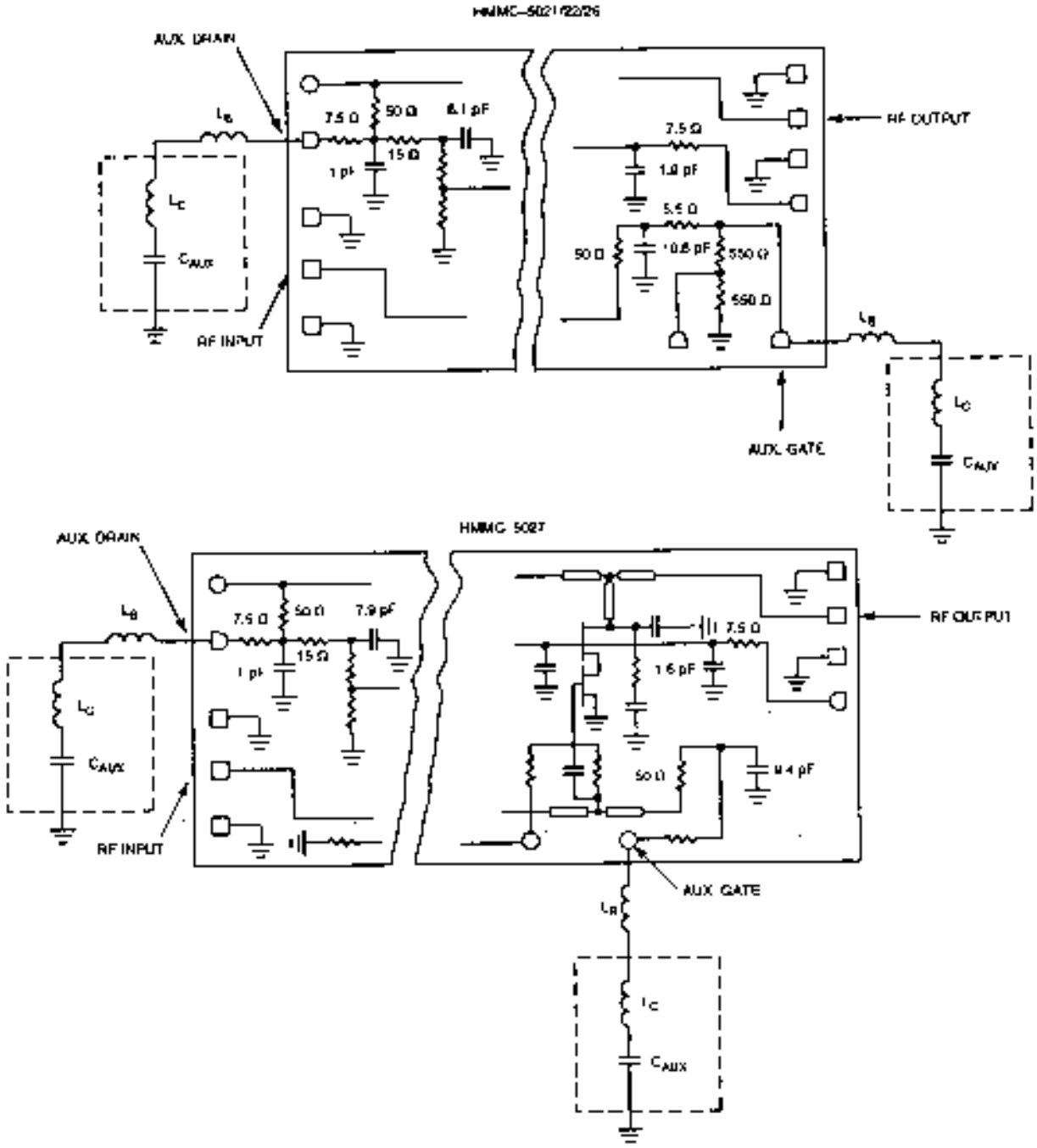


Figure 4. Simple Power Supply Configuration for Applying Bias to the TWA.



L_B is the inductance of the bond wire between C_{AUX} and the Auxiliary bond pad.

L_C is the parasitic inductance of C_{AUX}.

Figure 5. Low Frequency Extension Using Capacitors (C_{AUX}) on the Auxiliary Drain and Auxiliary Gate Bond Pads

When bypass capacitors are connected to the AUX pads, the low frequency limit is extended down to the point where the bypass capacitor (C_{AUX}) series resonates with the on-chip 50Ω load and small de-Q'ing resistor. The low frequently limit can be approximated from the following equation:

$$f_{C_{AUX}} = \frac{1}{2\pi(R_o + r_{DE\text{-}Q})\, C_{AUX}} \text{ (Hz)}$$

where,

R_o is the 50Ω gate or drain line termination resistor.

$R_{DE\text{-}Q}$ is the small 7.5Ω or 5.5Ω de-Q'ing resistor,

and,

C_{AUX} is the capacitance of the bypass capacitor connected to the AUX DRAIN or AUX GATE pad in farads.

With the external bypass capacitors (C_{AUX}) connected to the AUX GATE and AUX DRAIN pads, gain will show a slight increase between 1.0 and 1.5 GHz. This is due to a series resonance between the parasitic inductance of the bypass capacitor (L_C), the inductance of the bond wire (L_D) and the on-chip capacitance. The increase in gain is strongly affected by the total series inductance, therefore the bond wire from the Aux pads to the bypass capacitors should be made as short as possible. The small 5.5 and 7.5Ω resistors are included on-chip next to the GATE AUX and DRAIN AUX bond pads to de-Q the resonance and limit the amount of peaking in gain.

In a typical assembly, the bypass capacitors are usually monoblock capacitors on the order of 0.01 or 0.047 µF depending on the desired low frequency operating point. These monoblocks have series parasitic inductance (L_C) of ~0.8 and ~1.3 nH for 0.01 and 0.047 µF capacitors, respectively.

Using the preceding formula, the required bypass capacitor value can be calculated for various desired corner frequencies. Since this equation does not take into account TWA transmission line impedances and on-chip resistive networks, a more accurate capacitance value may be obtained by modeling the TWA with a linear simulation program and an accurate small-signal model for the TWA. These results are summarized in Tables 3 and 4.

Table 3: Maximum bypass capacitance connected to AUX GATE for extended low frequency performance.

Frequency (MHz)	Min Capacitance, (C_{AUX}) for f=	
	f_{CAUX}	$f\|S_{11}\|$=10dB
0.1	28 nF	45 nF
1.0	2.8 nF	4.5 nF
10	280 pF	450 pF
100	28 pF	35 pF
1000	2.8 pF	NR

Table 4: Minimum bypass capacitance connected to AUX Drain for extended low frequency performance.

Frequency (MHz)	Min Capacitance, (C_{AUX}) for f=	
	f_{CAUX}	$f\|S_{22}\|$=10dB
0.1	29 nF	35 nF
1.0	2.9 nF	3.5 nF
10	290 pF	350 pF
100	29 pF	25 pF
1000	2.9 pF	NR

Notes:

- The modelled results listed include a total series inductance ($L_C + L_B$) of 1.5 nH.
- $f|S_{11,22}|$=10dB is the lowest frequency at which the input/output return loss is still ≤ -10 dB. The values of C_{AUX} listed in this column are modelled values.
- NR indicates that an external bypass capacitor is NOT REQUIRED to achieve this performance.

7.0 DC Blocking Capacitance

A series DC blocking capacitor is required at the RF input and output of the amplifiers as shown in Figure 6. The value of this capacitor directly affects the low frequency performance of the TWA. It must be large enough to appear as a RF short circuit at the lowest desired operating frequency. A capacitor with low loss and low parasitic inductance is necessary for good high frequency performance. A beamlead capacitor or planar capacitor fits these requirements.

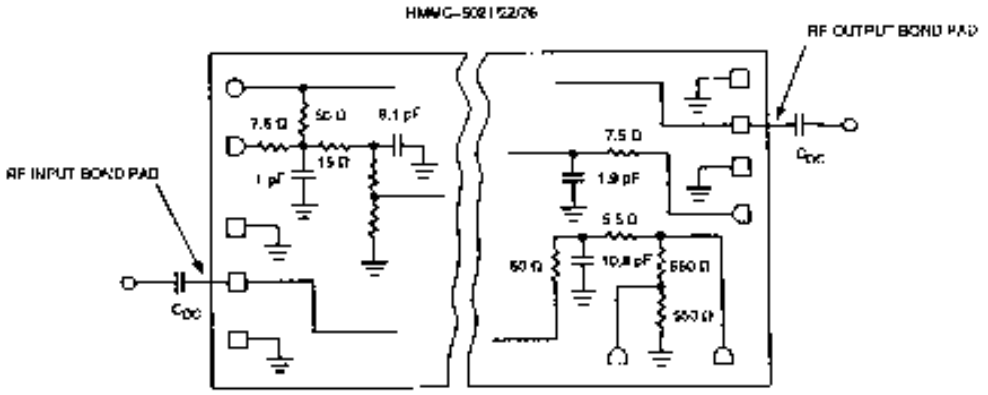


Figure 6. Location of DC Blocking Capacitors at the TWA RF Input and Output.

The lower frequency limit (f_{CDC}) due to the DC blocking capacitor can be calculated, to first order, by the following equation:

$$f_{C_{DC}} = \frac{1}{2\pi(R_o \times C_{DC})} \text{ (Hz)}$$

where,

R_o is the RF input/output terminating resistance (50Ω).

C_{DC} is the DC blocking capacitance in farads.

Using this equation, C_{DC} can be calculated for different desired corner frequencies. The equation is an approximation, because it does not take into account other factors, such as transmission line impedances and TWA termination networks. A more accurate C_{DC} value may be obtained by modeling the TWA and optimizing C_{DC} to yield the desired corner frequency. The calculated and modeled results are shown in Table 5.

Table 5: Minimum DC blocking capacitance for various low frequency limits.

Freq. (MHz)	Minimum Capacitance, (C_{DC}) for f=		
	f_{CDC}	$f\|S_{21}\|$-3dB	$f\|S_{11,22}\|$=-10dB
0.1	32 nF	24 nF	48 nF
1.0	3.2 nF	2.4 nF	4.8 nF
10	320 pF	240 pF	480 pF
100	32 pF	24 pF	48 pF
1000	3.2 pF	2.4 pF	4.8 pF

Notes:

- $f|S_{21}|$-3dB is the lowest frequency at which the maximum low frequency gain has decreased by 3 dB. The values of C_{DC} listed in this column are modelled values.
- $f|S_{11,22}|$=-10dB is the lowest frequency at which the input/output return loss is still ≤ -10 dB. The values of C_{DC} listed in this column are modelled values.

8.0 Drain Inductance

The drain bias pad is RF “hot” and must be isolated from the drain DC supply. Figure 7 shows a typical method of applying drain bias. This bias circuit passes DC to the drain line of the TWA while preventing the RF signal present on the drain line from appearing in the external DC biasing circuit. The series inductance of the bond wire (L_D) and the shunt capacitance of the bypass capacitor (C_D) form an RF choke circuit. The corner frequency (low frequency roll-off) is determined by the parallel combination of the drain bond wire inductance, L_D, and the on-chip 50Ω resistor.

If the length of the drain bond wire is too long, the bond may droop mid-span and short to the package floor causing a DC and RF electrical short. In some assemblies, this long bond may act as a high impedance transmission line and may transform an open circuit appearing λ/4 from the drain to a short circuit at the drain bias pad. This results in a gain “suck-out” and a corresponding peak in the output return loss at the λ/4 frequency.

The recommended length for the drain bond is between 100 to 200 mils, for 2-26.5 GHz opera-

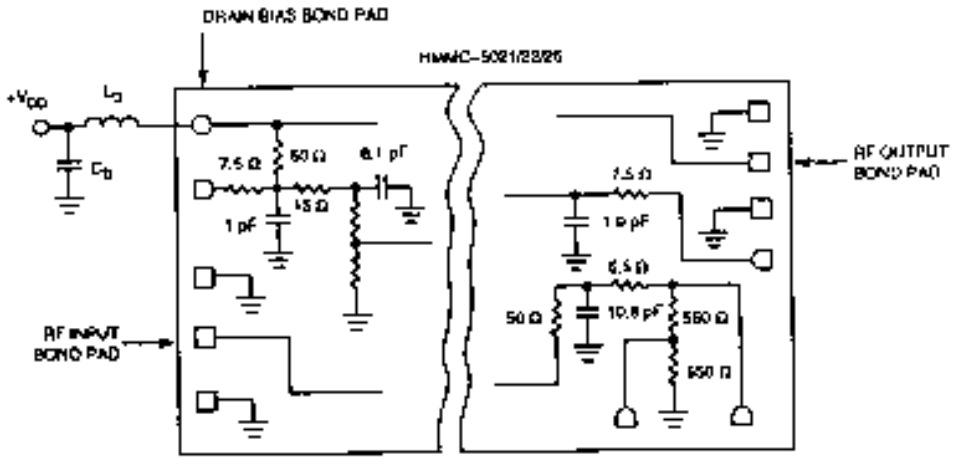


Figure 7. RF Choke Circuit Used to Isolate the Drain Voltage Supply from the RF 'Hot' Drain Bias Pad.

tion, and should be bypassed in at least 50 pF to provide a good RF ground. Typically, a chip capacitor is used to provide this capacitance and act as a bonding island between the drain bias pad and the feedthrough capacitor. Due to the length of this bond, radiative coupling between the bond and the package floor or between drain bonds of adjacent stages may cause excessive ripple in the gain response. This may also degrade the output match slightly at higher frequencies. To limit the gain ripple, non-conductive polyiron may be placed around the drain bond to reduce the radiative coupling. A 200 mil long bond wire has sufficient inductance to isolate the drain line from the power supply for frequencies down to about 1 GHz.

The bypass capacitor (C_D) can be either a chip capacitor, feedthrough capacitor or a combination of the two. Its value must be large enough to insure that the series resonance of C_D and L_D is lower in frequency than that of the a parallel combination of L_D and 50Ω. As a general rule, DC should be greater than or equal to the DC blocking capacitance described earlier.

GaAs MMIC TWAs have a tendency to "bias oscillate" at frequencies between 1 kHz and 1 MHz. This is due to insufficient RF bypassing at the microcircuit or module connections. Typically, capacitive feedthroughs are employed to help suppress higher frequency oscillations. However, to prevent the low frequency bias oscillations, additional bypass capacitance (~0.1 to 0.5μF) is required.

The lower frequency limit (f_{LD}) due to the drain bond wire inductance can be calculated using the following equation:

$$f_{L_D} = \frac{R_0}{(2\pi L_D)} \text{ (Hz)}$$

where,

R_0 is the RF input/output 50Ω terminating resistance, and L_D is the inductance associated with the off-chip drain bias circuit.

This equation can be used to calculate the minimum values of L_D required for various desired corner frequencies. Modeling the drain bond as a lumped inductor yields slightly different results than this equation due to the termination and transmission line impedances which exist on-chip. The calculated and modelled results are shown in Table 6.

As a practical application of the preceding discussion, a single-stage HMMC-5026 amplifier was assembled. The amplifier was built to demonstrate the assembly techniques and performance calculations presented. The amplifier utilized 0.01μF monoblock bypass capacitors connected to the AUX GATE and AUX DRAIN contacts, 150 pF integrated DC blocking capacitors at the RF input and output, and a 5μH wirewound polyiron core inductor connected to the DRAIN BIAS pad.

As indicated by the preceding formula, the low frequency limit, in this case, is dominated by the 150 pF DC blocking capacitors. The bypass capacitors and drain inductor used are sufficiently large enough to guarantee a low-end limit much lower in frequency. The -3dB roll-off in gain is 21.2 MHz and 15 MHz, for the calculated and modelled predictions, respectively. Modelled results also predicted the frequency at which the input and output return loss approached -10 dB to be about 30 MHz. The calculated and modelled results agree quite well with the measured results of the assembled amplifier. The low frequency roll-off (where gain is down by 3 dB) was measured on the amplifier to be 14.4 MHz. The input and output return loss were measured at less than -10 dB for f ≥29 MHz.

In conclusion, proper application on the preceding assembly and design techniques to the HMMC-5026 or HMMC-5027 can result in exceptional broadband performance. In this case, a 10 octave, single-stage amplifier with greater than 8 dB gain and less than -10 dB return loss was demonstrated over the full 30 MHz to 30 GHz frequency range.

Table 6: Minimum drain bond inductance for various corner frequencies.

Freq. (MHz)	Minimum Inductance, (L_D) for f =		
	fL_D	$f\|S_{21}\|$=-3dB	$f\|S_{11,22}\|$=-10dB
0.1	80 µH	40 µH	120 µH
1.0	8 µH	4 µH	12 µH
10	800 µH	400 nH	1200 nH
100	80 nH	35 nH	115 nH
1000	8.0 nH	3.0 nh	10 nH

Notes:

- The calculated and modelled results assume a terminating capacitance, C_D, large enough to guarantee that the series resonance between C_D and L_D will be below the parallel resonance. If a fixed capacitance on the order of 1 to 20 nF is used, the minimum inductance required for operation down to 100 kHz or 1 MHz must be larger.

9.0 Gain Control Using The Auxiliary Second Gate

Another feature designed into the HMMC-5026 and HMMC-2027 is the ability to control the gain of the amplifier via the auxiliary second gate bond pad. This allows the device to be used in a wide variety of applications where variable gain over a broad bandwidth is required. Such applications include automatic gain control (AGC) circuits, input signal modulation, leveled output power for improved source match and pulse modulation circuits.

The SECOND GATE BIAS (V_{GSB}) bond pad is connected to the gates of the upper FETs in every cascode stage by a small 7.5Ω de-Q'ing resistor. The other end of the second gate line is terminated in an on-chip resistive divider network which allows the second gate to self-bias to about 37% of V_{DD} for the HMMC-5026, and about 27% of V_{DD} for the HMMC-5027. Under normal operating conditions, this pad is left open circuited and therefore the drain current is set by the gate bias voltage applied to the lower FET in each stage. The nominal open-circuit voltage appearing at the SECOND GATE BIAS pad is about +2.5 and +2.0 volts for the HMMC-5026 and HMMC-5027, respectively. Under this operating condition, maximum gain and power are achieved from the TWA.

By applying an external voltage to the SECOND GATE BIAS pad (less than the open-circuit potential), the drain voltage on the lower FET can be decreased to a point where the lower FET enters the linear operating region. This will reduce the current drawn by each cascode stage and result in a decrease in gain. Second gate voltages (V_{GSB}) ranging form +2.5 down to about +0.5 volts will reduce the gain of the TWA about 2 to 3 dB. Decreasing V_{GSB} further will reduce the drain voltage on the lower FET towards zero while pinching off the upper FET in each stage. At large negative values of V_{GSB}, between 0.0 and -2.5 volts, the gain of the TWA will decrease significantly. This is illustrated in Figure 8, which shows the small-signal gain and output return loss (of a HMMC-5026 assembled in a small evaluation package) as a function of the voltage applied to the second gate.

Since the input and output return loss of the TWA is dominated by the gate and drain line terminations, varying the second gate voltage has minimal effect on the input/output match. This allows the user to adjust the gain of the TWA over wide dynamic range while maintaining good input/out return loss. At large negative voltages, between -1.5 and -2.5 volts, gain at lower frequencies begins to decrease more rapidly than that at higher frequencies causing significant positive gain slope. The minimum

dynamic range is about 50 dB at lower frequencies and reduces to about 40 dB at high frequencies.

10.0 Conclusion

Applying simple assembly and bonding techniques to the HMMC-5021/22/6 and HMMC-5027 TWAs will provide excellent RF performance across the full 2 to 26.5 GHz frequency range. The low frequency performance can be extended through the use of special bonding techniques and external circuitry. Another feature designed into the device is the ability to control the gain of the device via the auxiliary second gate bonding pad while maintaining a good input and output match. The performance enhancements described in this application note allow the user maximum flexibility to use the TWA in a wide variety of applications.