DC-50 GHz Variable Attenuator: Switching Speed Limitations

Application Note # 45

MWTC Semiconductor Marketing

HMMC-1002

1.0 Introduction

The HMMC-1002 is a voltage variable attenuator that operates from DC to 50 GHz. This application note highlights the switching speed limitations of the HMMC-1002, including temperature effects on switching speed.

2.0 Switching Speed Limitations

There is a well known GaAs anomaly called "slow tails" or "gate lag." The effect of this anomaly is that the drain current (and therefore, the channel resistance) does not have the same switching profile as the signal that was applied to the gate. The difference in the two profiles is seen in the settling time where there may be a time constant in the rise or fall time. Gate lag is believed to be due to surface states that exist near the edges of the gate. Since these surface states are not completely controlled, the occurrence of gate lag is also not controlled. Worse case conditions for gate lag occur when the gate is switched from beyond pinchoff to the ON state. On a single FET, the magnitude of the gate lag is dependent on how far beyond pinchoff the initial gate voltage is and how far ON the second voltage is switched to. The wider the swing across pinchoff, the higher the gate lag can be. Temperature can also affect the amount of gate lag. The colder the temperature, the higher the gate lag will be.

For FET attenuators, gate lag causes slow responses in channel resistance and when the channel resistance is slow to change, so is the

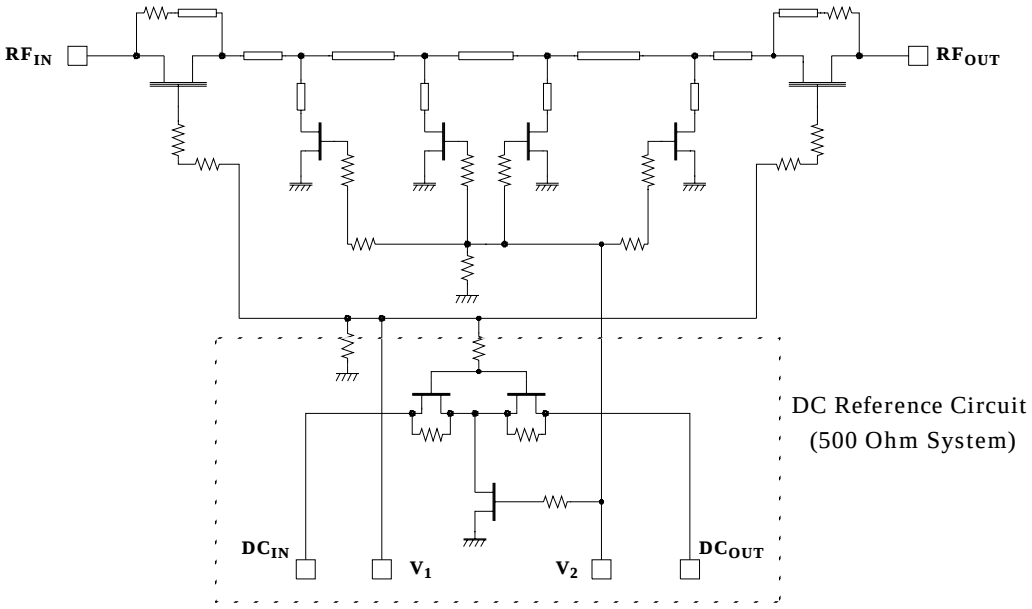

Figure 1. HMMC-1002 Schematic

attenuation level. For the HMMC-1002, this limitation is evident when switching from minimum attenuation to other attenuation levels (see Figures 2 and 3). Not all attenuation levels were tested, but the data suggests that all levels are affected. No gate lag was observed when switching from maximum attenuation to minimum, or when switching from other attenuation levels to minimum.This suggests that the shunt FET is the main cause of gate lag in the HMMC-1002. The theory suggests that gate lag may exist when switching from maximum to minimum due to the fact that the series FETs are being switched from -4 volts on the gate to 0 volts on the gate. However, any gate lag generated by the series FETs is expected to be very small due to the presence of the 50 ohm shunt resistors that are across each series FET. This resistor causes the equivalent series resistance to be buffered from changes in resistance that occur in the FET. Also, for a "T" attenuator, the attenuation level is more sensitive to shunt resistance changes than for series resistance changes. This explains why the HMMC-1002 only shows gate lag effects when going from lower attenuations to higher attenuations.

The switching speed is also affected by temperature. The colder the temperature the greater the effect. Data has shown that for some devices, gate lag will only be evident at temperatures below room temperature.

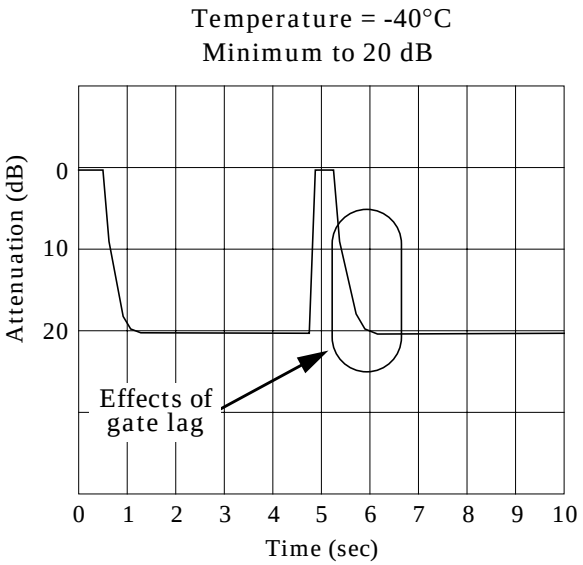

Figure 2. HMMC-1002 Switching Speed Minimum to 20 dB Level

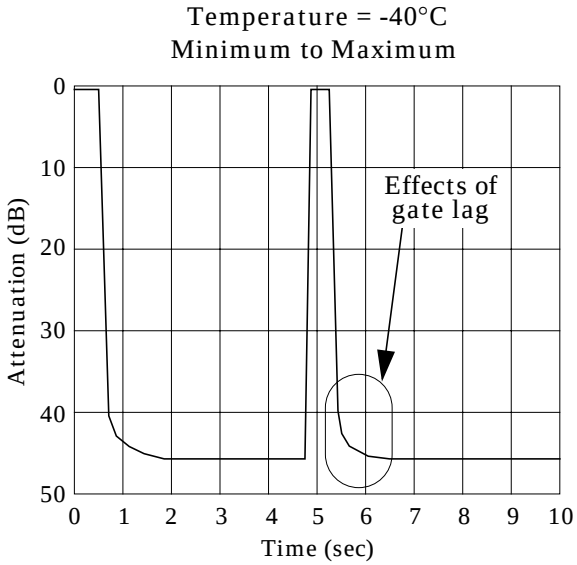

Figure 3. HMMC-1002 Switching Speed Minimum to Maximum Level