HEWLETT PACKARD

Measuring chip capacitors with the HP 8510C Network Analyzers and Inter-Continental Microwave test fixtures

Product Note 8510-17

Introduction

The increasing use of chip capacitors in RF and microwave designs requires a knowledge of their behavior beyond that available in current manufacturer data sheets. The HP 8510C network analyzer and Inter-Continental Microwave[1] in-line test fixtures compose the complete solution for the measurement of chip capacitors. The solution offers complete compatibility with the HP Microwave Design System (HP MDS).

Knowledge of chip capacitor properties are essential for designing circuits such as filters, impedance matching circuits, RF and DC blocking and digital pulse circuits. There are two reasons to perform measurements of a chip capacitor: 1) to see its behavior in its intended application, 2) to use the measurement data to create two-port black box networks and to derive equivalent models for use in a microwave circuit simulator.

This note includes a discussion of the HP 8510C and Inter-Continental Microwave (ICM) test fixtures, chip capacitor terminology, including equivalent circuit models, and an example of a chip capacitor measurement.

Measurement system and fixtures

The ICM universal test fixture, TF-3001, along with an appropriate ICM TRL calibration kit, is used for all measurements. The test fixture accommodates a wide range of insertable midsections covering most packaged two-port devices. Capacitor midsections are available for a variety of chip capacitor sizes, providing flexibility in measurement and design. All midsections provide easy mounting and are non-destructive to the capacitor which reduces valuable measurement set-up time. Capacitor fixtures come in series-thru, shunt-thru, and shunt-to-ground configurations that allow horizontal and vertical mounting, providing easy and convenient measurements. Capacitor orientations (horizontal or vertical mounting) effect the sequence of resonances. This knowledge can be used to extend a capacitor's useful bandwidth. Capacitor measurements performed in their intended configurations, series-thru, shunt-thru, or shunt-to-ground as shown in Figure 1 give good approximations for quick analysis.

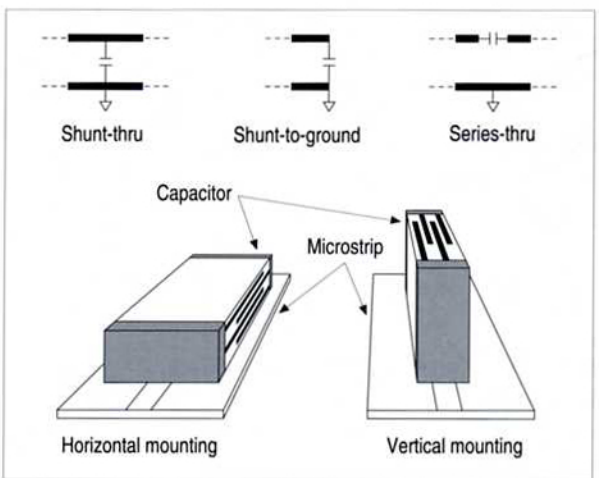

Figure 1. Capacitor configurations and orientations.

[1]Inter-Continental Microwave
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The core of the measurement system is the HP 8510C network analyzer. The HP 8510C is known as the premier network analyzer system for microwave measurements from 45 MHz to 50 GHz. The HP 8510C provides one of the widest bandwidths covering all of today's chip capacitor applications, and has thru-reflect-line (TRL) capability which is essential for in-fixture measurements. The TRL calibration technique allows devices to be measured in a non-coaxial environment with a high degree of convenience and accuracy. For more information and a description of TRL theory, see the REFERENCES section at the end of this note.

The use of HP MDS gives a sharp focus to the complete solution. HP MDS can be used to model two-port networks from measured data and can optimize an equivalent chip capacitor model for more accurate results in circuit design.

Chip capacitor terminology and models

Realizable chip capacitors contain parasitics that are generally negligible at DC and low frequencies. However, in the RF and microwave spectrum they become important. Capacitors can be modeled with equivalent circuit elements that account for these parasitics. Two equivalent circuits are used to represent chip capacitors: 1) the folded transmission line, and 2) the lumped element model. The folded transmission line represents the chip capacitor accurately over a wide bandwidth and accounts for the many series and parallel resonances that occur at higher frequencies. The lumped capacitor model is simpler than the folded transmission line and is a good model up to the first parallel resonant frequency. The lumped capacitor model, shown in Figure 2, is the model used throughout this note because of its simplicity.

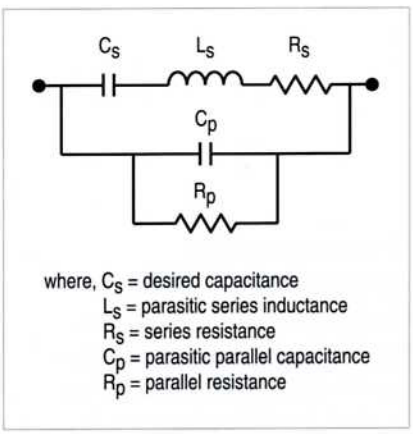

Figure 2. Equivalent lumped element model.

Figure 3 shows a typical plot of insertion loss for the lumped element model. The points of series and parallel resonances are created by L_S in series with C_S and L_S in parallel with C_p. The resistances, R_p and R_S, account for parallel and series resistive losses. Another parasitic resistor in parallel with C_S is of concern only at DC and low frequencies and is not shown in the above model.

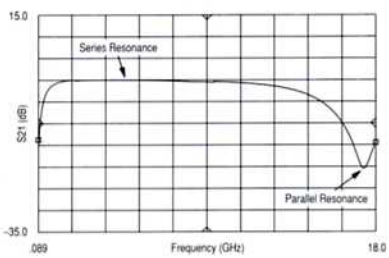

Figure 3. Lumped element insertion loss.

The frequency at which the desired capacitance C_S is measured can be found in manufacturer data sheets. This frequency is usually 1 MHz where the effects of R_S, L_S, C_p, and R_p become negligible. The impedance magnitude of an ideal capacitor varies from infinite at DC to zero at infinite frequency. Realizable capacitors are non-ideal and contain parasitics that effect their impedance response. Figure 7 shows a Smith chart plot of a 3 pF capacitor. At its series resonance the capacitor appears as a small resistor, while at its parallel resonance it appears as a large resistor. Between DC and its series resonance it acts as a capacitor, while between its series and parallel resonances, it acts as an inductor. The deviation of its series resonance impedance from zero indicates series resistive losses and the deviation of its parallel resonance impedance from infinity indicates parallel resistive losses. The spectra of series and parallel resonances of a measured capacitor are clearly visible in the insertion plot in Figure 4.

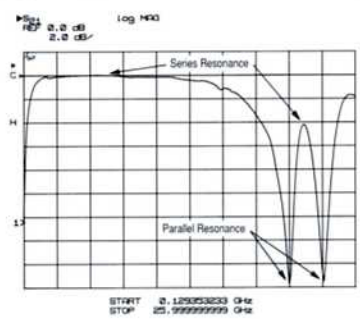

Figure 4. Insertion loss for a typical capacitor.

Two general parameters, equivalent series resistance (ESR) and dissipation factor (DF), characterize the performance of capacitors. The ESR combines all losses, both series and parallel, into a single resistance at a given frequency. The ESR varies with frequency.

The dissipative factor is the percentage power input that turns to heat. It is often confused with the power factor. Figure 5 indicates their relationship. In an ideal capacitor the current leads the voltage by 90 degrees. In realizable capacitors the current leads the voltage by the phase angle, θ. The tangent of the phase angle complement, termed the loss angle, is the dissipation factor (DF) and the cosine of the phase angle is the power factor (PF). The reciprocal of the DF is the quality factor, Q. The DF varies nonlinearly with frequency and is related to the ESR by:

$DF = 2\pi C_S \cdot (ESR)$

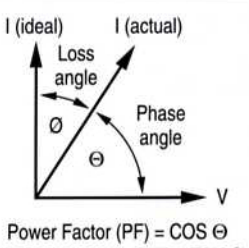

Figure 5. Power factor vs. dissipation factor.

Measurement example

The example below derives an equivalent lumped circuit model from measurement data obtained from the HP 8510C and ICM test fixture with a series horizontally oriented 3 pF capacitor. The example illustrates the approximation of the equivalent lumped circuit model components in Figure 2 and optimization using HP MDS.

Measurement procedure

The measurement of any chip capacitor follows a simple measurement sequence composed of the following steps:

1. Set up instrument
Define the measurement by setting the basic measurement parameters. These include sweep type, start/stop frequencies, sweep time, number of points, RF power level, and the parameter to be measured. Other functions such as smoothing, scaling, or trace math are post-processing functions and can be set after a measurement has been performed.

2. Calibrate
Calibration is essential to ensure that measurement data accurately represents the device under test (DUT). TRL calibration is used to calibrate the in-line test fixture and should be performed with the appropriate TRL calibration kit. Refer to the ICM operating manual for procedures.

3. Connect DUT
The midsection and DUT should be inserted into the fixture. The fixture holding pads may need to be adjusted to accommodate the DUT.

4. Perform measurement
Once the device has been connected, store the measured frequency response within the instrument. This can be done with a single sweep or multiple sweeps for averaging.

5. Post processing
Post processing functions such as trace statistics and marker searches can be used during this step. Any function that effects the data after error correction is classified as a post-processing function.

Results

The insertion loss, shown in Figure 6, clearly defines series and parallel resonant frequencies. Using the HP 8510C marker functions the series and parallel resonances were determined from the return loss plot in Figure 7 to be 5.6 and 16.5 GHz. This capacitor is well suited for a matching network ranging from 2 to 8 GHz since it has 0 dB insertion loss over this band. It would not, however, be a good choice for digital pulse circuitry since the variation in the insertion-loss angle is large with respect to frequency, and would result in an unacceptably large pulse distortion.

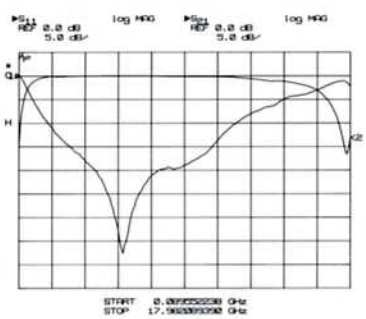

Figure 6. 3 pF capacitor (S_{21} & S_{11})

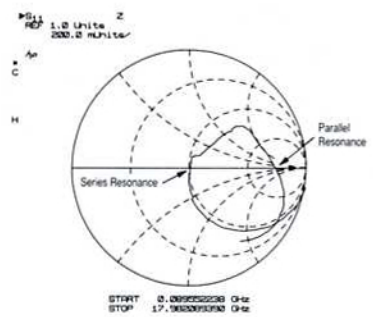

Figure 7. 3 pF capacitor (Smith chart)

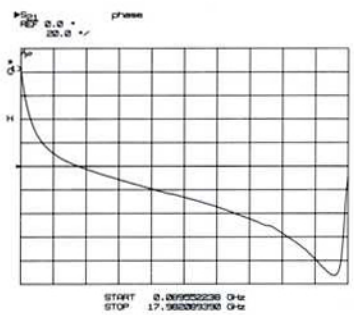

Figure 8. 3 pF capacitor ($\angle S_{21}$)

From the return loss measurement, an impedance versus frequency plot was constructed in Figure 9.

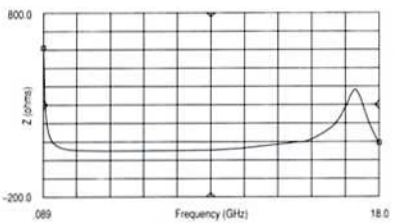

Figure 9. Impedance for 3 pF capacitor

Using this data, the equivalent circuit values were calculated:

Resistance, R_s
At the series resonant frequency, the capacitor appears as a small resistor whose value is approximated by the series resistance, R_S, in the equivalent circuit model. R_S was determined to be 0.2 ohms by setting a marker at 5.6 GHz.

Capacitance, C_s
The capacitance C_S is the capacitance specified in manufacturer data sheets and is usually measured at 1 MHz. If the impedance was known at 1 MHz, the capacitance could be calculated from:

$$C_S = \frac{1}{\omega \bullet |Z_{1\ MHz}|}$$

However the impedance at 1 MHz is not known. Therefore, for a first order approximation, C_S is assumed to be the value specified by the manufacturer, 3 pF.

Series Inductance, L_s
The inductance L_S in series with C_S creates a series resonance of 5.6 GHz. Therefore,

$$\frac{1}{\sqrt{L_S \bullet C_S}} = 2\pi f_{series}$$

and,

$$L_S = \frac{1}{(2\pi f_{series})^2 \bullet C_S} = 0.3\ nH$$

Parallel Capacitance, C_p
The capacitance C_p in parallel with Ls creates a parallel resonance of 16.5 GHz. Therefore,

$$\frac{1}{\sqrt{L_S \bullet C_p}} = 2\pi f_{parallel}$$

and,

$$C_p = \frac{1}{(2\pi f_{parallel})^2 \bullet L_S} = 0.3\ pF$$

Resistance, R_p
At the parallel resonant frequency, the capacitor appears as a large resistor. This resistance is approximated by R_p in the equivalent circuit model. R_p was determined to be 400 ohms by setting a marker at 16.5 GHz.

Once the component values had been approximated, HP MDS was used to optimize individual components within the model. The results of the optimization are compared with the measured data in Figure 10 and Figure 11 shows the optimized lumped circuit model. The optimized capacitance was 3.54 pF which was within specified tolerances. The optimized model is a good equivalent to the measured capacitor.

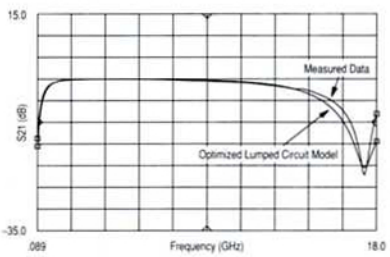

Figure 10. Comparison of optimized lumped circuit model and measured data (S_{21}).

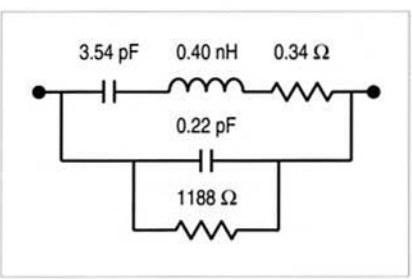

Figure 11. Optimized model

The ESR can be determined from the dissipative loss, DL, by:

$$ESR = \frac{R_{ref}(1-\sqrt{DL})}{(1+\sqrt{DL})}$$

where,

$$DL = \frac{(1-|S_{11}|^2)}{(|S_{21}|^2)}$$

and,

R_{ref} refers to the reference impedance

Figure 12 shows a smoothed ESR curve. Its minimum occurs at the series resonance and its value increases as frequency approaches the parallel resonance.

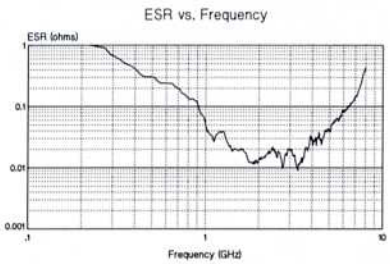

Figure 12. ESR vs. frequency (smoothed)

The Q factor in Figure 13 is related to the ESR through the dissipation factor:

$$Q = \frac{1}{DF}$$

where,

$$DF = 2\pi f C_s \bullet (ESR)$$

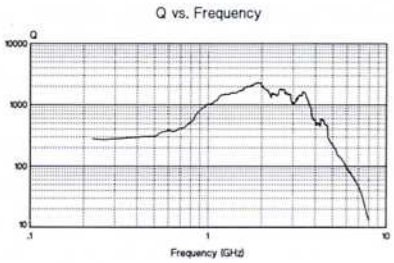

Figure 13. Q vs. frequency (smoothed)

Extremely good calibration is required to measure both ESR and Q. Calibration standards must be clean of any foreign particles and carefully handled. Visual inspection should be done every time a standard is used. The contact between calibration standards and the ICM fixture RF-pins is critical to calibration. For proper TRL calibration techniques, see the REFERENCES section at the end of this note.

This example has illustrated the path from the measurement of a chip capacitor to its equivalent lumped circuit model using the HP 8510C, ICM test fixture and HP MDS.

References

Hewlett-Packard Product Note 8510-8A, *"Network Analysis: Applying the HP 8510 TRL calibration for non-coaxial measurements"*, 1992.

Inter-Continental Microwave Application Note 111, *"Mainframe/TRL Calibration Trouble Shooting"*, 1991.

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