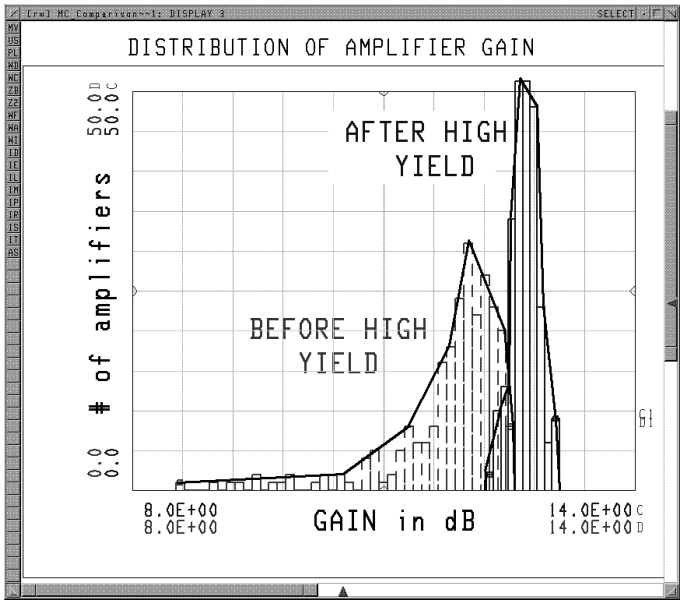
HEWLETT PACKARD

Using the High Yield Software Package to Create Robust Designs

Product Note 85150-5



Using High-Frequency Design Software from HP-EEsof

Introduction

The HP 85149A/AN High Yield Software Package utilizes the Design of Experiments (DOE) statistical analysis technique to help designers create robust designs that have high yields in manufacturing. DOE is a proven technique that has been used to make manufacturing processes less sensitive to component variations. Now DOE has been added to circuit simulation software to allow designers to use this powerful technique to analyze their designs and make them more robust. The HP 85149A/AN High Yield Software Package is used with Release 6.0 (or later revisions) of the HP Microwave and RF Design Systems[1].

Intended Audience for this Product Note

This product note was written for design and manufacturing engineers, assuming no prior knowledge of DOE. The product note covers the benefits of DOE, and shows its application in the design of an RF amplifier. Appendix B covers basic DOE theory. Readers with even minimal experience using the HP Microwave Design System (MDS) and RF Design System (RFDS) should be able to begin using DOE on their circuits immediately. Readers who have never used HP MDS and RFDS, should be able to understand the benefits of DOE and how it may be applied.

[1]DOE is also available in Series IV, Version 5.0.

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One Designer's Experience

As a design engineer, you know you must include margin in your design for variations seen in a production environment. In your last design, you used first order analysis to make sure the design would work. You did a prototype run of ten. With minor tweaks, you were able to get all ten units working. You passed the design to production. In the first production run, new variations were seen and production had to stop shipments. You spent many overtime hours, with your boss looking over your shoulder, getting the circuits working again. Eventually you had to loosen the specifications, over the objections of marketing, but you told them there was no other solution. Three months later your design has a low turn-on yield and requires much rework and production engineering support. You want to get onto your next big project, but you are spending all your time supporting production.

Now let's use Design of Experiments. Using the topology you had, you ran a DOE simulation and discovered that if you changed the nominal component values, you could reduce the circuit's sensitivity to component variations. In fact, you were able to make marketing happy by achieving the original specification. Your production engineer was pleased when you showed him the simulation results (see the figure on page 1), which indicated that the yield would increase with less variation, without the need for tighter-tolerance parts.

Benefits of DOE

A designer's main tasks are to determine a topology, set parameter values (such as bias voltages and resistor values), and to determine how tightly component tolerances must be set to meet performance objectives. Perhaps the longest part of this process is determining the best nominal values for the many parameters in a circuit. Often this process is not done methodically and a designer may not be sure that the best solution has been found. DOE provides a methodical, efficient method of finding the best nominal parameter values in a circuit and a way to set their tolerances.

DOE is an organized way of setting up a series of simulations ("experiments"), and keeping track of the results to reveal which parameters and parameter interactions[2] are important. Designers then use this information to set parameter values and their tolerances to optimize circuit characteristics and minimize variations.

"I have parameter tuning, performance optimization, and sensitivity analysis. Why do I need DOE?"

Many designers use more simple design techniques, such as tuning, in which they vary only one parameter at a time. These techniques have some limitations, in that they do not reveal parameter interactions, and can be slow and cumbersome. Performance optimization is an improvement, but this technique provides less insight, and may find a solution that is too sensitive to parameter variations. Also, it is often necessary to make trade-offs among circuit characteristics, and performance optimization does not provide information enabling a designer to make such trade-offs. DOE takes performance optimization a step further, by allowing a designer to investigate a circuit's performance variation due to component tolerances, and to choose among different solutions. Performance optimization will produce different solutions depending on the goals of the optimization and the weighting given to each goal. Often a designer must make trade-offs among various circuit performance characteristics. Sensitivity analysis is another approach that can be used, but it is not particularly helpful in finding the best nominal values, and does not reveal the effects of parameter interactions. DOE overcomes many of the limitations of both performance optimization and sensitivity analysis.

[2]See Appendix A—What are parameter interactions?

How Design of Experiments is Applied

The objective of DOE analysis is to optimize a circuit's characteristics by finding the best nominal parameter values and their tolerances. A DOE analysis is carried out by varying parameter values in a circuit, and seeing how the circuit's characteristics change. Of course, this is the kind of thing that designers do often, when attempting to improve their designs. The big contribution of DOE is that it enables a designer to investigate the effects of many parameters on a circuit's characteristics simultaneously. DOE also displays the results using tables and plots that clearly indicate what must be done to improve the circuit, including trade-offs that might be necessary.

For example, in an amplifier circuit, the characteristics to be optimized might be gain, stability factor, output match, etc. DOE may also be used to find parameter values and tolerances that minimize variations in these characteristics. This will be described in the "Using a Nested DOE Simulation to Find an Optimal Solution (Taguchi Analysis)" section. In DOE terminology, these characteristics are called **response variables**. The parameters to be varied might include bias resistor values, stability resistor and inductor values, or matching network element values. In DOE terminology, these are called **factors**.

In a DOE analysis, the parameters (factors) are varied and multiple simulations are run. The DOE outputs show how the circuit characteristics (response variables) depend on the parameters. The simulator uses two levels for the factors, the nominal value plus a percentage or absolute value, and the nominal value minus a percentage or absolute value. As a simple example, if a designer were investigating how to set the nominal values of two resistors in an amplifier circuit to optimize the gain, a DOE simulation would be set up as follows:

Run #	Resistor A	Resistor B	Gain	Point in Figure 1
1	900	450	9 dB	r1
2	1100	450	10 dB	r2
3	900	550	9.5 dB	r3
4	1100	550	12 dB	r4

This experiment is depicted graphically in Figure 1.

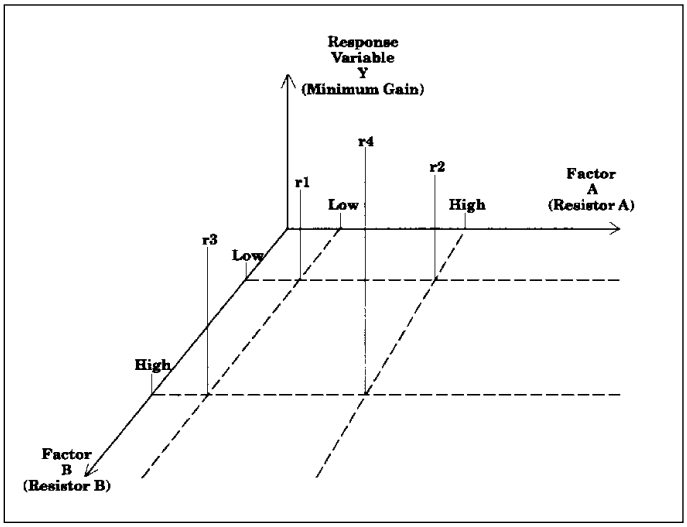

Figure 1. A graphical depiction of a simple DOE simulation. Four simulations are run, each with a different possible combination of the factor values. The relationship between the gain and the two resistors is actually a surface, and the DOE simulation finds four points on this surface.

The nominal value of resistor A is 1000 ohms, and the nominal value of resistor B is 500 ohms. Each one is set to its nominal value plus or minus 10% (may be any percentage) during the simulation runs. Note that all possible combinations of resistor values are simulated, and that there are two levels for the factors during the simulations. Experiments of this type are called **two-level full factorial**.

The outputs from a DOE simulation such as this are a Pareto chart that shows which factors and interactions dominate the response variable(s) (gain, in this example), main effects plots and interaction plots which show how the factor values should be set for best performance, and an ANOVA (ANalysis Of VAriances) table which provides additional statistical information about the experiment. This experiment is so simple that the designer is able to choose the best parameter values from the table above. However, in more complex DOE simulations with many factors and two response variables, examining the DOE outputs would be necessary to choose the best factor values.

Definition of Common Terms

Multiple Analysis Capabilities

Sensitivities—A sensitivity analysis is used as a screening step to determine which factors dominate a circuit's response. (A factor is a component or parameter value that is varied during the DOE simulation.) All factors are held at their nominal values except for one, which is set to the high and low values defined by the user. This is repeated for each factor. Note that this is not the same as a traditional sensitivity analysis, which calculates mathematical derivatives, because the difference between the high and low values of each factor can be arbitrarily large.

Two-Level Full Factorial—This type of experiment provides the most information, because all combinations of the factors are included.

Two-Level Fractional Factorial—This type of experiment is useful when the number of factors is greater than about four. It reduces the total simulation time by eliminating the simulations used to compute higher-order interactions.

Response Variables

A response variable can be anything definable by an equation, such as the minimum value of a stability factor, gain, DC power consumption, power-added efficiency, harmonic levels, or worst-case return loss. DOE can be used with all analyses, such as DC, AC, S-parameter, harmonic balance, and others. This flexibility allows the designer to analyze many different characteristics. DOE outputs (Pareto chart, ANOVA table, main effect plots, etc.) may be generated for one or two response variables at a time. DOE outputs for other response variables may be generated easily, without resimulating the circuit. Note that an arbitrarily large number of response variables may be displayed simultaneously in table form, with each response variable being a column. This can be useful when making trade-offs among circuit characteristics.

Factors

Up to twelve factors may be defined for full and fractional factorial experiments, and up to twenty-six factors may be defined for sensitivity analyses. The high and low values may be defined by either plus and minus a percentage or plus and minus an absolute value.

DOE Outputs

Design Matrix and Response Variable Table—shows the values of the factors for each simulation and the corresponding response variables.

ANOVA Table—indicates numerically which factors and interactions have the largest effects on the response variables, and gives other statistical information about the experiment. ANOVA stands for "ANalysis Of VAriance."

Pareto Chart—displays the ANOVA table information in a histogram, allowing a designer to easily see which factors and interactions dominate.

Main Effects Plots—display the main effects of all of the factors on the response variables. The designer uses these to determine the best nominal values for each of the factors.

Interaction Plots—display how interactions affect the response variables. The designer uses these to determine factor values when interactions are significant.

The use of these DOE outputs will be described in the "Applying DOE–A Design Example" section, which begins on the next page.

Applying DOE to Your Designs

Using DOE for performance optimization

How DOE is applied depends on where a circuit is in the design process. If acceptable nominal performance has not been achieved yet, then DOE may be used as an optimizer. This is described in Steps 1–6 of the "Applying DOE–A Design Example" section.

Using DOE to evaluate variability in circuit performance and to set specifications

If an acceptable solution already exists, either from performance optimization or manual design techniques, then DOE may be used to investigate the variability of the circuit's responses. This is described in Step 7 of the "Applying DOE–A Design Example" section. This step is particularly useful when determining whether a circuit will meet its specifications or when setting specifications.

Using DOE to optimize circuit performance and minimize variability simultaneously

DOE may be used to optimize circuit performance and minimize variability simultaneously, using a nested technique described below. This method is also known as the "Taguchi method." It allows a designer to consider both the mean value of a circuit response and the variation in the response simultaneously.

Using DOE with surface-mount components

DOE may be used with circuits that have surface-mount (SMT) components. In this case, it may be easier to find a good nominal solution using lumped elements, rather than starting with SMT library components. This is because SMT library components include not only the main component (such as a resistor, capacitor, or inductor), but also various parasitic components. Assuming the parasitics change with the nominal value of the main component, a large change in the main component's value without changing the parasitics would lead to an inaccurate simulation. After finding a good solution with lumped elements, the lumped element components are replaced with SMT components, and the DOE techniques described in the "Using DOE with SMT Library Parts" section on page 25 could be used to analyze the variability of the circuit responses.

Using DOE to improve circuits that are difficult to manufacture

For circuits that are currently difficult to manufacture, or sometimes fail to meet specifications, DOE may be used to determine which parameters contribute the most to variations in circuit responses. This type of analysis would lead the designer to tighten the tolerances on the critical component(s), or use a nested DOE analysis or the other techniques described in this product note to find a better set of nominal parameter values.

Applying DOE–A Design Example[3]

To show how DOE may be used to design circuits, a simple amplifier example will be shown. The circuit was originally designed to be a low-noise 1 GHz amplifier. The original circuit was designed considering bias, stability, noise figure, and output match, all independently, and is shown in Figure 2.

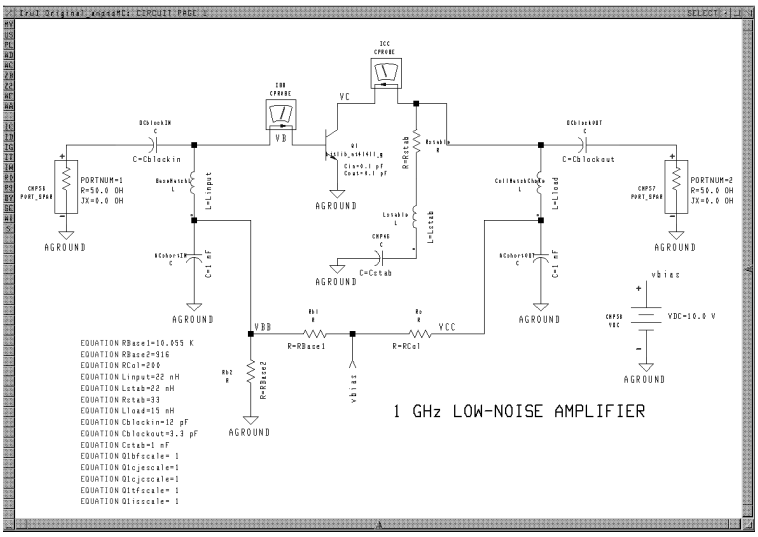

Figure 2. Schematic of amplifier to be analyzed using DOE.

DOE will be used to improve the amplifier's performance (primarily gain and stability) in the 1-2 GHz band. Here is an outline of one design method, using DOE:

1. Choose a topology and initial component values.
2. Run a simulation to check the circuit's initial characteristics.
3. Decide objectives for DOE simulations, and choose circuit parameters (factors) to vary.
4. Set up a screening experiment to determine which factors are important.
5. Run the screening experiment, present the results, and remove insignificant factors.
6. Run a fractional factorial or full factorial experiment and choose a best set of factor values (this step may require iterations).
7. Evaluate variability in circuit responses due to parameter tolerances.

Step 1. Choose a topology and initial component values

The initial step was to choose bias resistor values to provide a 10 mA collector current. The next step was to insert a shunt resistor and inductor at the collector of the device to stabilize it. Then an LC network was added at the input, to improve the noise figure. Finally, an LC network was added at the output to improve the output match.

[3]The screen views in this example are from the workbench, "DOE_analysis_of_BJT_LNA," which is in the example file, "amplifiers," included with HP MDS and RFDS Release 6.0.

Step 2. Run a simulation to check the circuit's initial characteristics (this list could vary, depending on what is important to the designer) such as:

- Edwards/Sinsky stability factor, MU[4]
- minimum gain
- gain delta (maximum gain—minimum gain)
- input and output match
- DC collector current

Figure 3 shows the simulation control blocks.

The results of this simulation are shown in Figure 4, in which only the worst-case values are shown. The stability factor is computed as shown in Figure 6.

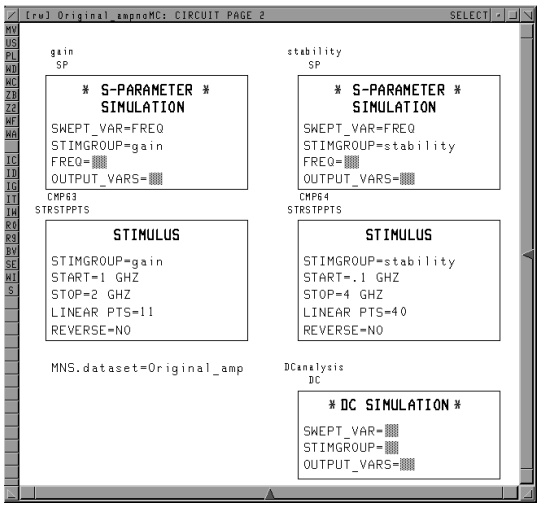

Figure 3. Simulation control blocks. The S-parameters are computed over two different frequency ranges, the band of interest, 1-2 GHz, and a wider range, 0.1-4 GHz, to check stability.

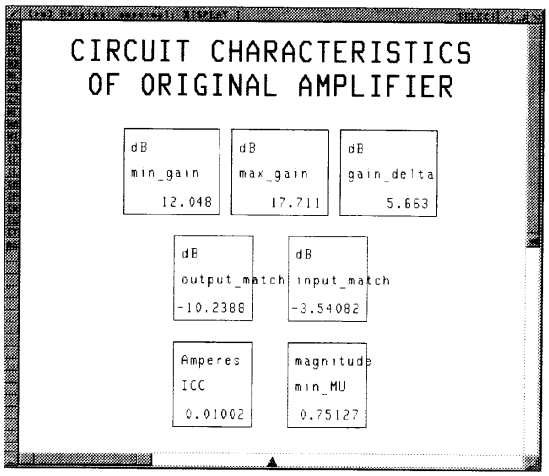

Figure 4. Original amplifier circuit simulation results.

Note that the amplifier is no longer unconditionally stable, because MU is now less than one, over some part of the 0.1-4 GHz range. The stability factor is simulated over a wider range than the gain, to verify that there will not be an out-of-band oscillation.

If the amplifier's performance is satisfactory, the designer should skip to Step 7 to evaluate the variability of the circuit due to parameter variations. Steps 3–6 describe using DOE to choose the best nominal component values.

[4]M.L. Edwards and J.H. Sinsky, "A Single Stability Factor for Linear 2-port Circuits," 1992 *IEEE MTT-S International Microwave Symposium Digest*, Vol. 2, pp. 885-888, June 1992.

Step 3. Decide objectives for DOE simulations, and choose circuit parameters (factors) to vary

It is desirable to increase the minimum value of MU (min_MU in Figure 4). Also, the minimum gain (min_gain) is important, and it is necessary to see how changes that improve MU degrade the gain. Gain variation (maximum gain–minimum gain), input and output match, and collector current are other characteristics that may need to be checked as circuit changes are made. The circuit parameters (factors) to be varied must also be chosen. Because improving stability is the primary objective, circuit parameters that are expected to have an effect on stability should be chosen. These include the stability resistor and inductor, Rstable and Lstable, and also the bias resistors Rbase1, Rbase2, and RCol. Additional parameters such as output match inductor (CollMatchChoke) and input match inductor (BaseMatchL), and various capacitors might be included as DOE factors. While these parameters are not expected to have any effect on the stability, they are included in the initial analysis, just to be sure. Deciding on the objectives and choosing circuit parameters (factors) relies on the designer's intuition and knowledge.

Step 4. Set up a screening experiment, to determine which factors are important

DOE full factorial experiments, in which the circuit is simulated with all possible combinations of factor values, reveal the most information. However, they also take the most time. If there are eight factors, for example, then a full factorial experiment would require 2^8=256 simulations. For this reason, it is desirable to run a simpler screening experiment to eliminate factors that don't have an effect on the circuit characteristics of interest.

There are two types of screening experiments. One is a **sensitivity** analysis, in which all circuit parameters (factors) are held at their nominal values, except one, which is set to its high value for one simulation, and its low value for another. These pairs of simulations are repeated for each of the factors. This type of analysis will not reveal any parameter interactions, but it will show the main effect of each of the factors. A **fractional factorial** experiment, in which only part (one-half, one-quarter, or less) of a full factorial experiment is run, may also be used to screen factors. Fractional factorial experiments reveal less information than full factorial ones, but they are much faster, and reveal enough information to eliminate unimportant factors.

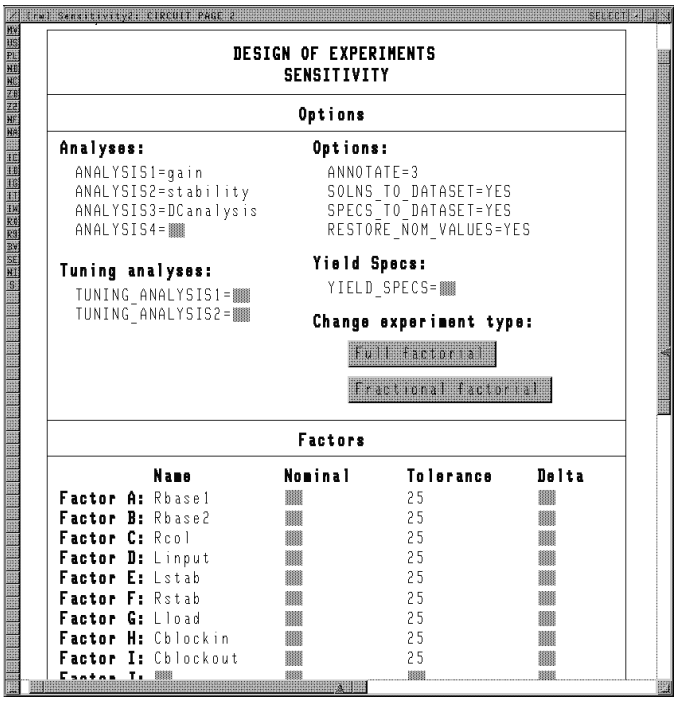

Figure 5. DOE form with parameter names entered as factors.

Figure 5 shows the variables and the percentage above and below the nominal value that defines the high and low values of each factor during the experiment. These are entered into a DOE form, which was inserted onto the circuit page via the menu pick INSERT/MDS CONTROL/STATISTICS/DESIGN OF EXPERIMENTS. The variables could also be defined without equations, using notation such as “Rstable.r”, where “Rstable” is the name of one the resistors. This form has two sections: the Options section for choosing the analyses, changing the experiment type (sensitivity was chosen, as indicated below the title of the form), and the Factors section for specifying the factors and defining the high and low values for each factor. It is not necessary to specify the nominal value here, if it is defined in an equation elsewhere, or if the factors are entered in the “Rstable.r” notation. The high value for each factor is the nominal value plus the percentage in the “Delta %” column or plus the number (absolute value) in the “Delta, abs” column. The low value for each factor is defined similarly. There are three simulations run for each set of factor values, and the names, gain, stability, and DCanalysis, refer to the simulation control blocks in as shown in Figure 3.

Before starting the simulation, if the designer selects the View Design Matrix button at the bottom of the DOE form (not visible in Figure 5), the simulator will show how many simulation runs will be made. This DOE sensitivity analysis requires 18 simulations.

Step 5. Run the screening simulation, present the results, and remove insignificant factors

Run the simulation by selecting the DOE form, and selecting the menu pick PERFORM /MNS /LOCAL. The simulation requires less than 4 seconds. The simulation results are all stored in a dataset specified by the designer. The next step is to present the results, by inserting a presentations page and inserting equations to define response variables that will be used in the DOE analysis. Figure 6 shows the computation of the minimum gain of the amplifier in the 1-2 GHz range, min_gain, and the minimum value of the stability factor, min_MU, for each of the 18 DOE runs. The variable, min_gain, is computed from the equation:

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min_gain=min(dB(S_21gain),2)
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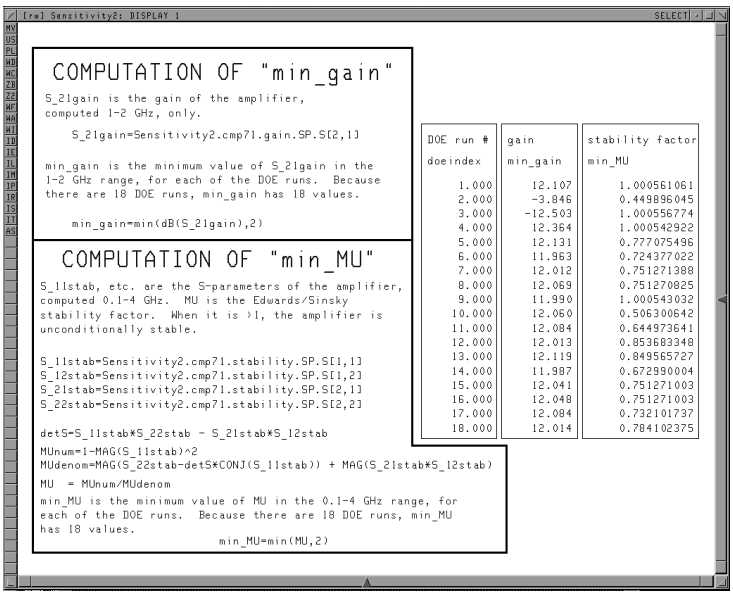


Figure 6. Computation of the response variables, min_gain and min_MU is the first step in presenting the results of a DOE simulation.

S_21 gain is actually a two-dimensional array, the first being the DOE simulation index, and the second being the frequency, which varies from 1 to 2 GHz. The notation in the equation causes the minimum value of dB(S_21gain) to be found, by searching the second dimension of the array. i.e., for each DOE simulation index, which corresponds to a different S-parameter simulation with a different set of factor values, the minimum gain in the 1-2 GHz range is found.

Several DOE presentations (design matrix and responses, ANOVA table, Pareto chart, main effects plots, and interaction plots) are generated automatically, when the user selects the presentations page menu pick INSERT /DOE RESULTS, and enters the response variables, as shown in Figure 7.

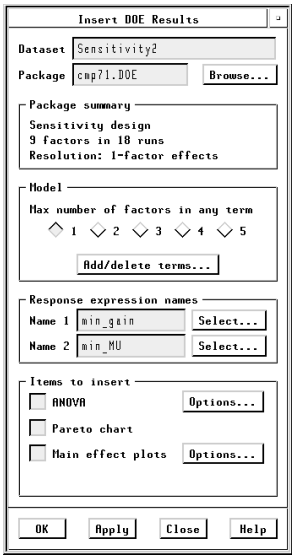


Figure 7. Palette for inserting response variables. When the OK button is selected, the DOE presentations are generated automatically.

Since the objective of the screening experiment is to remove insignificant factors from the experiment, attention should be focused on the Pareto chart, as shown in Figure 8.

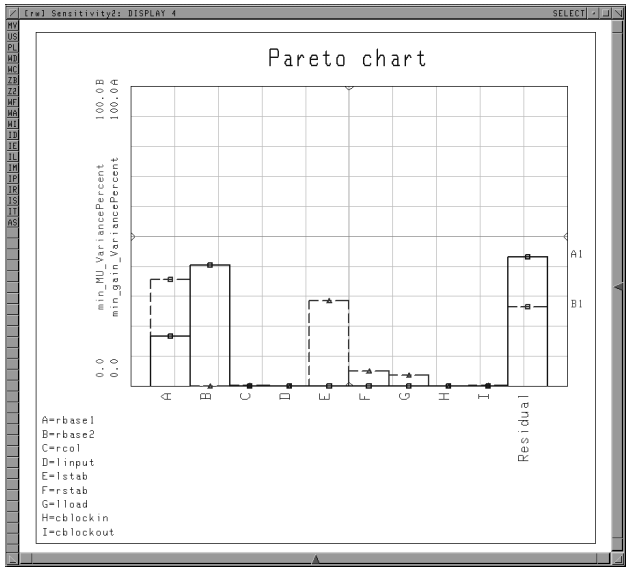


Figure 8. The Pareto chart indicates which factors have the greatest effect on the response variables.

This chart indicates which factors dominate variations in the response variables, min_gain and min_MU. The chart indicates, for example, that varying factor B (resistor rbase2) has a strong effect on min_gain, but almost no effect on min_MU. Similarly, the chart indicates that varying Factors C, D, H, or I has no effect on either min_gain or min_MU. This indicates that these factors could be removed from the experiment.

The designer should remember that sensitivity analyses only reveal main effects. Factors C, D, H, and I could have interactions with some of the other factors, and the high residual present indicates that there may be interactions present. As described in Appendix B, DOE analysis computes the coefficients of a polynomial that expresses the response variables in terms of each of the factors and interactions among factors. The residual is a measure of how accurate this equation is. If the residual is high, then a more complex DOE analysis should be done, such as a fractional factorial or a full factorial.

Step 6. Run a fractional factorial or full factorial experiment and choose a best set of factor values

This step may require several iterations. Figure 9 indicates the modified DOE form, after removing 4 factors and switching from a sensitivity experiment to a fractional factorial experiment.

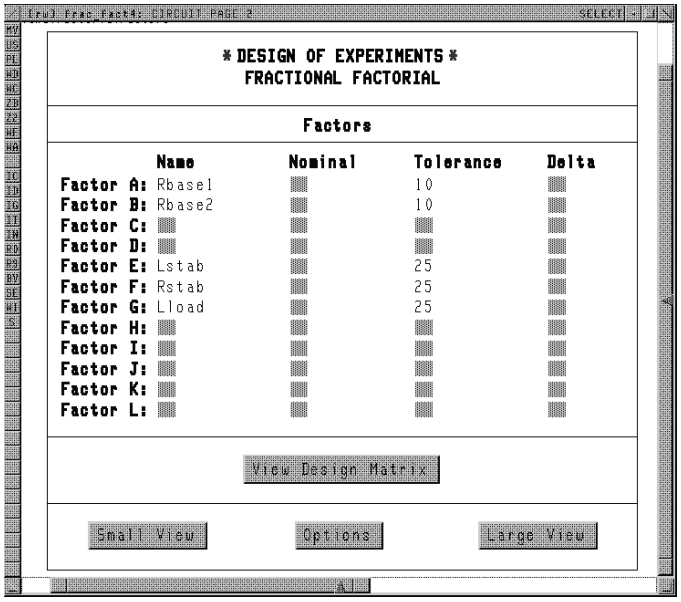


Figure 9. The DOE form, after removing 4 factors and switching to a fractional factorial experiment. This is the simplified version of the form that only displays the factors.

This is done by selecting the “Fractional Factorial” button in the “Options” section of the DOE form on the circuit page. This version of the DOE form displays only the factors. Also, note that the percentage change on resistors Rbase1 and Rbase2 has been reduced to 10%, because with the tolerance at 25%, the device would be biased incorrectly for some of the DOE runs. With only 5 factors, the designer could run a full factorial experiment, which would require 32 simulations, but a fractional factorial experiment, requiring only 16 simulations, was chosen as a compromise between simulation time and information obtained.

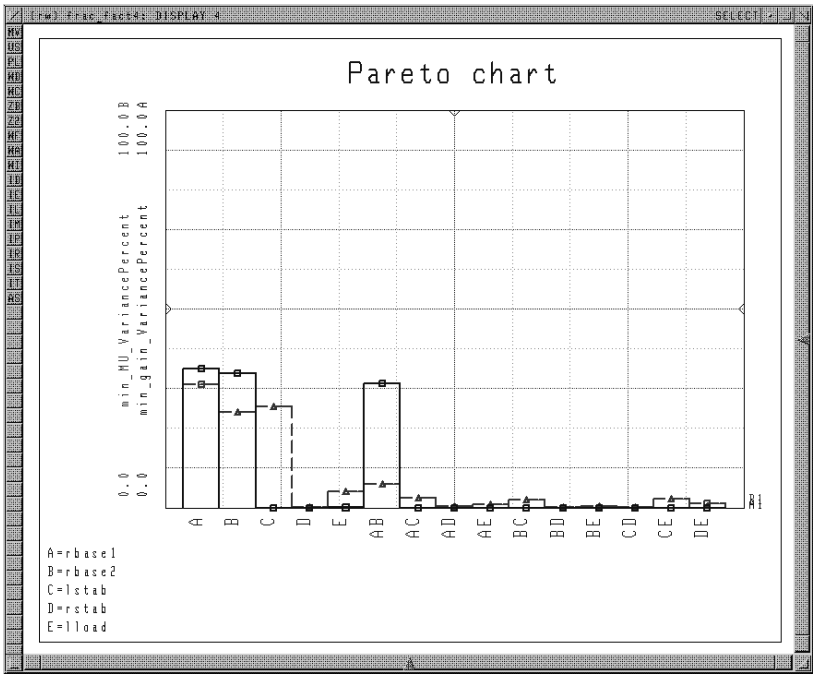


Figure 10. The Pareto chart indicates that Factors A, B, and C influence the stability factor, MU, and that Factors A and B and the AB interaction affect the gain.

The resulting Pareto chart in Figure 10 reveals interesting information. It shows that the stability factor, MU, is dominated by bias resistors, Rbase1 and Rbase2, and stabilizing inductor, Lstab, but that varying the stability resistor, Rstab, has virtually no effect on MU. The designer should be aware that the effect of the stability resistor is probably greater when the nominal values of the other parameters in the circuit are significantly different. Such dependencies are present in many circuits.

The Pareto chart tells the designer which main effects plots and which interaction plots to examine to determine which direction to change the various circuit parameters. Figure 10 shows that Factors A and B (rbase1 and rbase2), and the AB interaction influence the amplifier's gain. Also, Factors A, B, and E (lstab) influence the stability factor. Because Factors A and B influence both the gain and the stability factor, the designer may need to make a trade-off.

The Pareto chart indicates which factors and interactions are important, but not how to set the factor values. For this information, the designer must examine the main effect and interaction plots. Figure 11 shows the main effect plots for each of the factors.

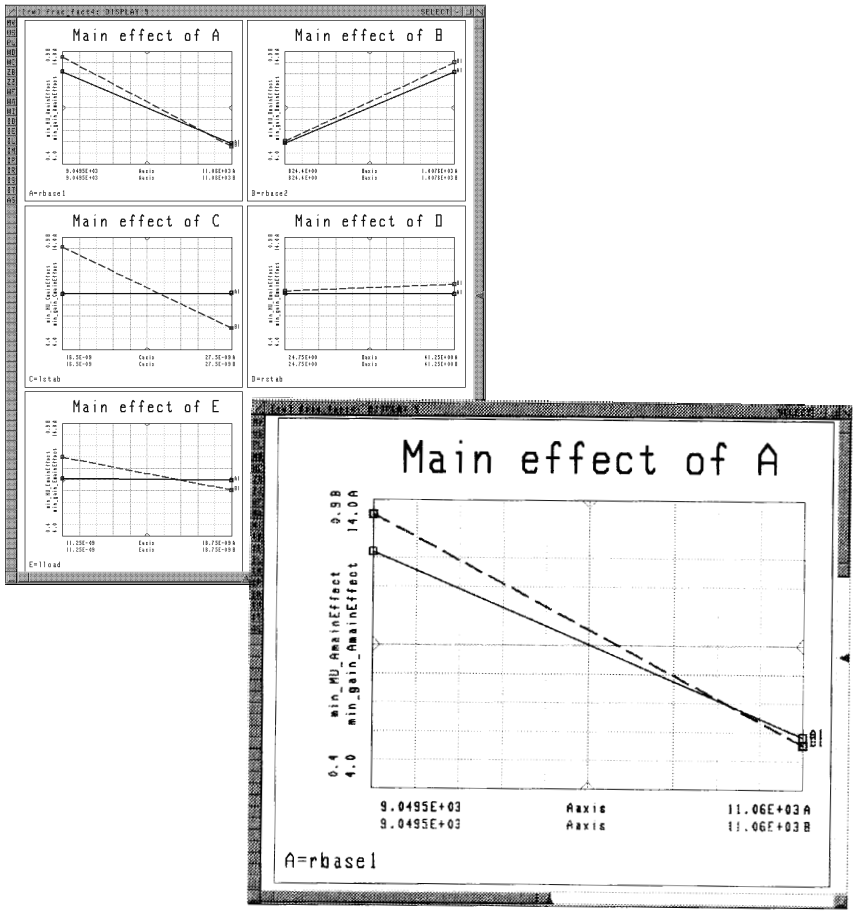


Figure 11. The main effect plots indicate how the circuit parameter values may be adjusted to improve the circuit responses.

The plot above labeled *Main effect of A* shows the average value of the response variables, min_gain and min_MU, when factor A (Rbase1) is set to its low value (9.0495 Kohms) and its high value (11.06 Kohms). The plot indicates that both min_gain and min_MU are higher (which is good) when rbase1 is set to its low value. Studying the other main effect plots indicates that Factor B (Rbase2) should be set to its high value, Factor E (Lstab) should be set to its low value, and Factor G (Lload) should be set to its low value. The main effect plots in this example are somewhat unusual in that no trade-offs have to be made, i.e., gain does not have to be sacrificed to attain better stability or vice-versa.

After examining the main effect plots, it is necessary to examine the interaction plots. Because the Pareto chart indicated that only the AB interaction was significant, only that interaction plot should be examined. Figure 12 indicates that highest gain and stability factor is obtained when factor B (Rbase2) is high and factor A (Rbase1) is low.

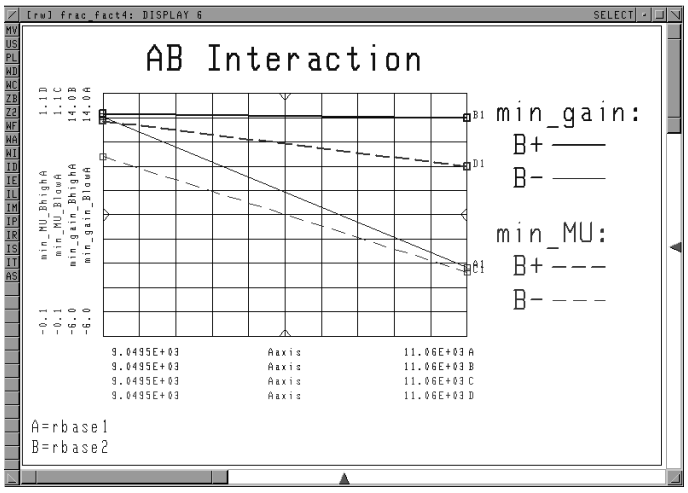
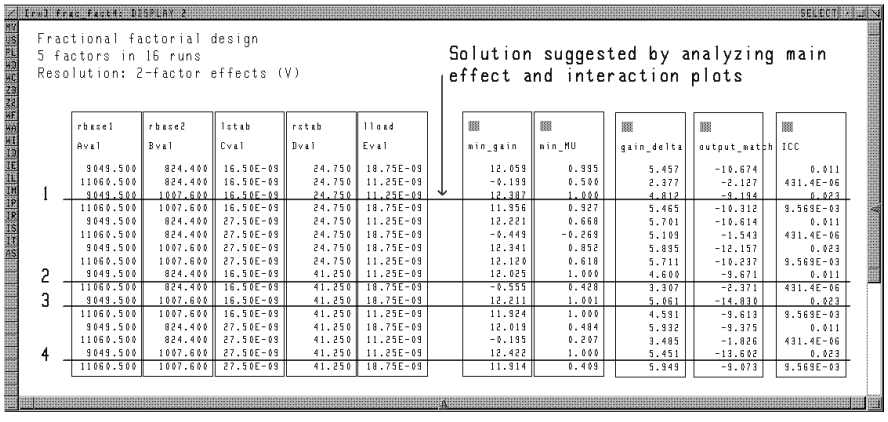


Figure 12. This interaction plot indicates that Factor B (Rbase2) should be set to its high value and Factor A (Rbase1) should be set to its low value.

Often, the interaction plots will indicate that the factors should be set in a way that conflicts with what the main effect plots show. If this occurs, the designer should refer to the design matrix and responses table (described next) to choose the best factor values.

Figure 13 shows the design matrix and responses table (which is also automatically generated by the INSERT/DOE RESULTS menu pick and will be on a different presentations page).



	rbase1 Aval	rbase2 Bval	lstab Cval	rstab Dval	lload Eval	min_gain	min_MU	gain_delta	output_match	ICC
	9049.500	824.400	16.50E-09	24.750	18.75E-09	12.059	0.995	5.457	-10.674	0.011
	11060.500	824.400	16.50E-09	24.750	11.25E-09	-0.199	0.500	2.377	-2.127	431.4E-06
1	9049.500	1007.600	16.50E-09	24.750	11.25E-09	12.387	1.000	4.812	-9.194	0.023
	11060.500	1007.600	16.50E-09	24.750	18.75E-09	11.956	0.327	5.465	-10.312	9.569E-03
	9049.500	824.400	27.50E-09	24.750	11.25E-09	12.221	0.668	5.701	-10.614	0.011
	11060.500	824.400	27.50E-09	24.750	18.75E-09	-0.449	-0.268	5.109	-1.543	431.4E-06
	9049.500	1007.600	27.50E-09	24.750	18.75E-09	12.341	0.852	5.895	-12.157	0.023
	11060.500	1007.600	27.50E-09	24.750	11.25E-09	12.126	0.618	5.711	-10.237	9.569E-03
2	9049.500	824.400	16.50E-09	41.250	11.25E-09	12.025	1.000	4.600	-9.671	0.011
	11060.500	824.400	16.50E-09	41.250	18.75E-09	-0.555	0.428	3.307	-2.371	431.4E-06
3	9049.500	1007.600	16.50E-09	41.250	18.75E-09	12.211	1.001	5.061	-14.830	0.023
	11060.500	1007.600	16.50E-09	41.250	11.25E-09	11.924	1.000	4.591	-9.613	9.569E-03
	9049.500	824.400	27.50E-09	41.250	18.75E-09	12.019	0.484	5.932	-9.375	0.011
	11060.500	824.400	27.50E-09	41.250	11.25E-09	-0.195	0.207	3.485	-1.826	431.4E-06
4	9049.500	1007.600	27.50E-09	41.250	11.25E-09	12.422	1.000	5.451	-13.602	0.023
	11060.500	1007.600	27.50E-09	41.250	18.75E-09	11.914	0.409	5.949	-9.073	9.569E-03

Figure 13. The design matrix and response table shows the values of the factors during each DOE run, as well as the corresponding circuit responses. The listing columns for gain_delta, output_match, and ICC have been added to allow the designer to better choose the factor values.

Each row in the table represents a single simulation, and shows the values to which each factor was set, as well as the corresponding response variable values, min_gain and min_MU. The row labeled 1 corresponds to the factor values that the main effect and interaction plots indicated to be “best.” Note that there are three other sets of factor values, labeled 2, 3, and 4, that produce similar results. To help choose among these four sets of factor values, three additional simulated characteristics of the circuit have been added in listing columns. These are: gain_delta, which is the difference between the minimum gain and the maximum gain of the circuit, output_match, which is the worst-case output return loss, and ICC, which is the collector bias current. The table indicates that solution 2 would be better for minimum gain variation and because it only requires 11 mA of bias current. However, solution 3 would be better if output match were more important and 23 mA of bias current could be tolerated.

Note that the “best” circuit performance may not be with all factors set to the high or low values used in the DOE experiment. It may be possible to achieve better performance by setting some of the factor values outside the range of the experiment or somewhere in between the high and low values. These possibilities can be investigated by carrying-out additional DOE runs.

Second Simulation

Solution 3 described above and shown in Figure 13 was chosen as the new set of nominal factor values, and an additional DOE simulation was made to see if the stability factor MU could be increased further. The same factors, delta percentages, and response variables were kept. The Pareto chart in Figure 14 shows that the AB interaction still has a strong effect on the gain, but that nothing has any significant effect on the stability factor, MU. This indicates that if MU is to be increased, then some other factor must be found to vary.

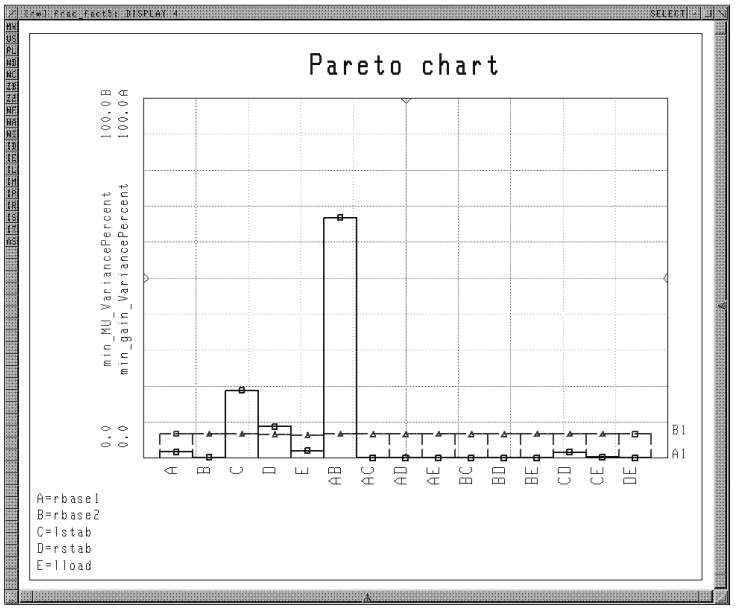


Figure 14. The Pareto chart from the second DOE simulation indicates that none of these factors or interactions influence the stability factor.

Second Sensitivity Run

A quick way to determine which circuit parameters might influence MU is to increase the number of factors and run another sensitivity analysis. Figure 15 shows the list of factors and tolerances entered into a DOE form. Because MU seems to be so insensitive to the parameters in the circuit, the tolerance has been increased to 50% on most of the factors.

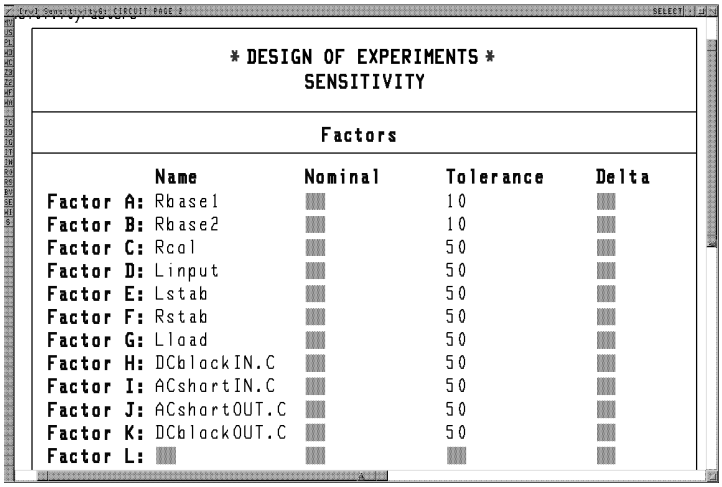


Figure 15. The DOE form used in the second sensitivity run.

The resulting Pareto chart in Figure 16 reveals that MU is influenced primarily by two factors, inductor Lload and the output DC blocking capacitor. Also, the Pareto chart indicates that the gain can be adjusted via the collector bias resistor, Rcol, and the inductor, Lstab.

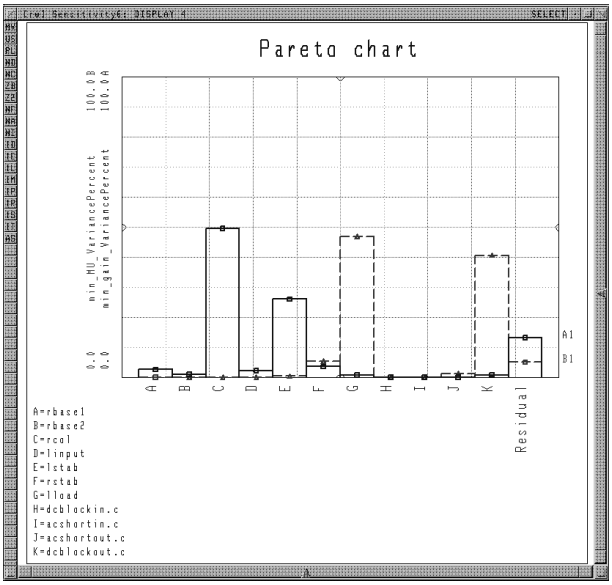


Figure 16. This Pareto chart indicates that Factors G and K have the most influence on the stability factor.

Result

After several more iterations like the ones described previously, a satisfactory set of parameter values was found, giving a minimum gain of 12.7 dB, minimum stability factor, MU, of 1.056, output match of -10.4 dB, and gain variation, gain_delta, of 5.2 dB. The last DOE simulation that was run indicated that inductor, LStab, and resistor, RStab, could be adjusted to improve the gain or stability, but not both simultaneously.

Step 7. Evaluate variability in circuit responses due to parameter tolerances

The next step is another DOE simulation to see whether the circuit's performance is sufficiently intolerant to variations in parameters. The value of each parameter is assumed to have a Gaussian distribution, and the parameter high and low values will be set to the nominal value plus and minus one standard deviation. The results of the DOE simulation runs will vary, and from this variation, a mean value and standard deviation for each performance characteristic of the circuit may be computed. From the mean value and standard deviation, the designer will be able to set the specifications for each performance characteristic, or, if the specifications already exist, determine whether the circuit will meet them or not. If a specification cannot be met, the DOE results (particularly the Pareto chart) can be analyzed, to see which parameters dominate the particular characteristic. The tolerances of these parameters may be tightened until the circuit meets its specifications, and conversely, the parameter tolerances that don't matter may be loosened.

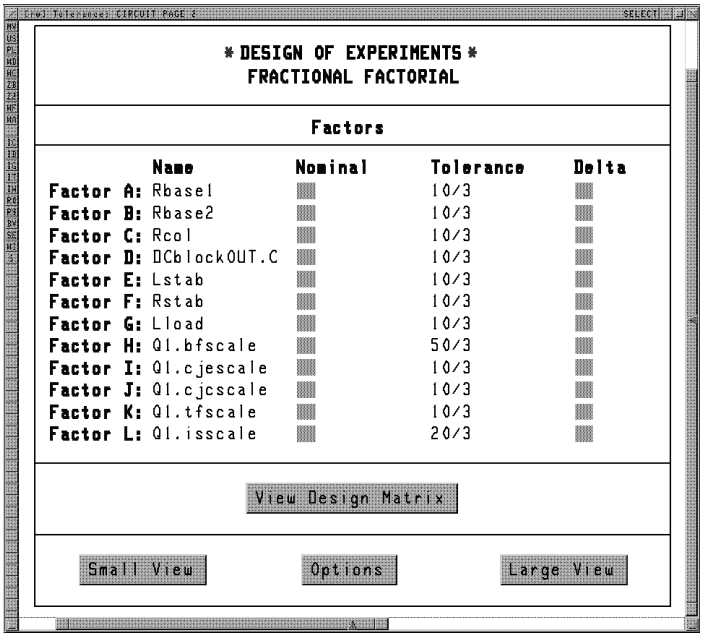


Figure 17. DOE form set up to evaluate the variability of the circuit responses due to parameter tolerances.

Figure 17 shows the DOE form for this analysis. Several transistor model parameters have been added as factors. These include transistor model scaling coefficients which all have a nominal value of 1. Q1.bfscale scales the forward beta of the device, Q1.cjescale scales the base-emitter zero-bias depletion capacitance, Q1.cjcscale scales the base-collector zero-bias depletion capacitance, Q1.tfscale scales the ideal forward transit time, and Q1.isscale scales the saturation current density. These and many other scaling parameters are now in each model of the active device model libraries, and may be used to see the effects of device model variation on circuit performance.

The “Delta %” column in the DOE form is a percentage used to define the high and low values used in the DOE simulation. The high value of each factor during the simulation is the nominal value plus this percentage, and the low value is the nominal value minus this percentage. In this tolerance analysis, high and low values are set to the nominal value plus and minus one standard deviation. In this example, we have assumed that the components have normally distributed parameter values, and that the specified tolerance is equal to three times the standard deviation. In Figure 17, Factor A, Rbase1, is assumed to have a 10% tolerance, and during the DOE simulation, the high and low values are the nominal value plus and minus one standard deviation, or (10/3) %. The transistor model parameter variations are just a guess. Transistor manufacturers typically do not supply this information.

The computed mean value of the minimum gain was 12.7 dB, and the standard deviation was 0.152 dB. The standard deviation of a response variable may be computed using an equation of the form:

standard deviation = sqrt (variance (response variable)) or
= stddev (response variable)

The designer must enter an equation like this to compute the standard deviation of each response variable or performance characteristic. This indicates that the minimum gain specification should not be set higher than 12.24 dB, which is the mean value of the response variable minus three times the standard deviation. (The designer may want to use the more conservative standard of six times the standard deviation when computing the specification limit.) The mean value of the minimum stability factor, MU, was 1.055, and the standard deviation was 0.00332. This indicates that the amplifier should remain stable. The mean value of the output match was -10.3 dB, and the standard deviation was 0.498 dB, which implies that the output match specification could be set near -8.8 dB. The mean value of the collector current was 25 mA, and the standard deviation was 4 mA, which implies that the collector current might vary from 13 to 37 mA in production.

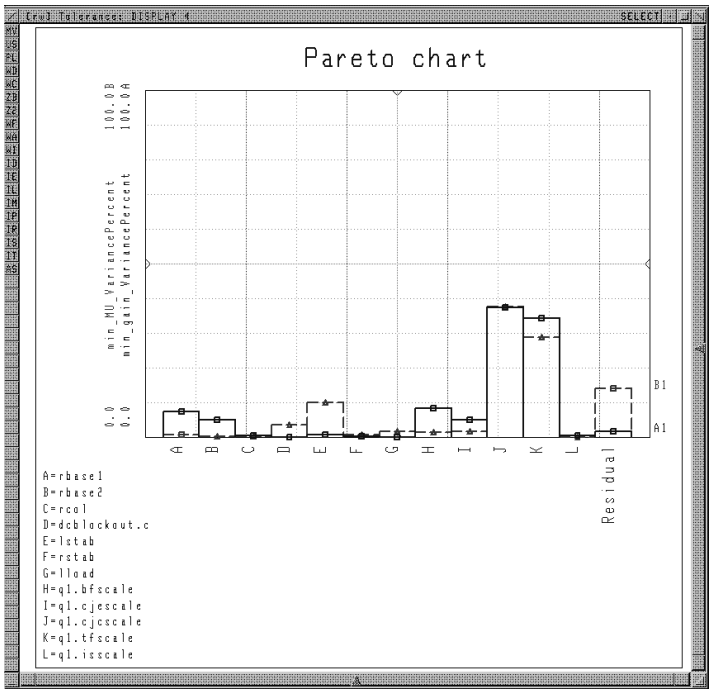
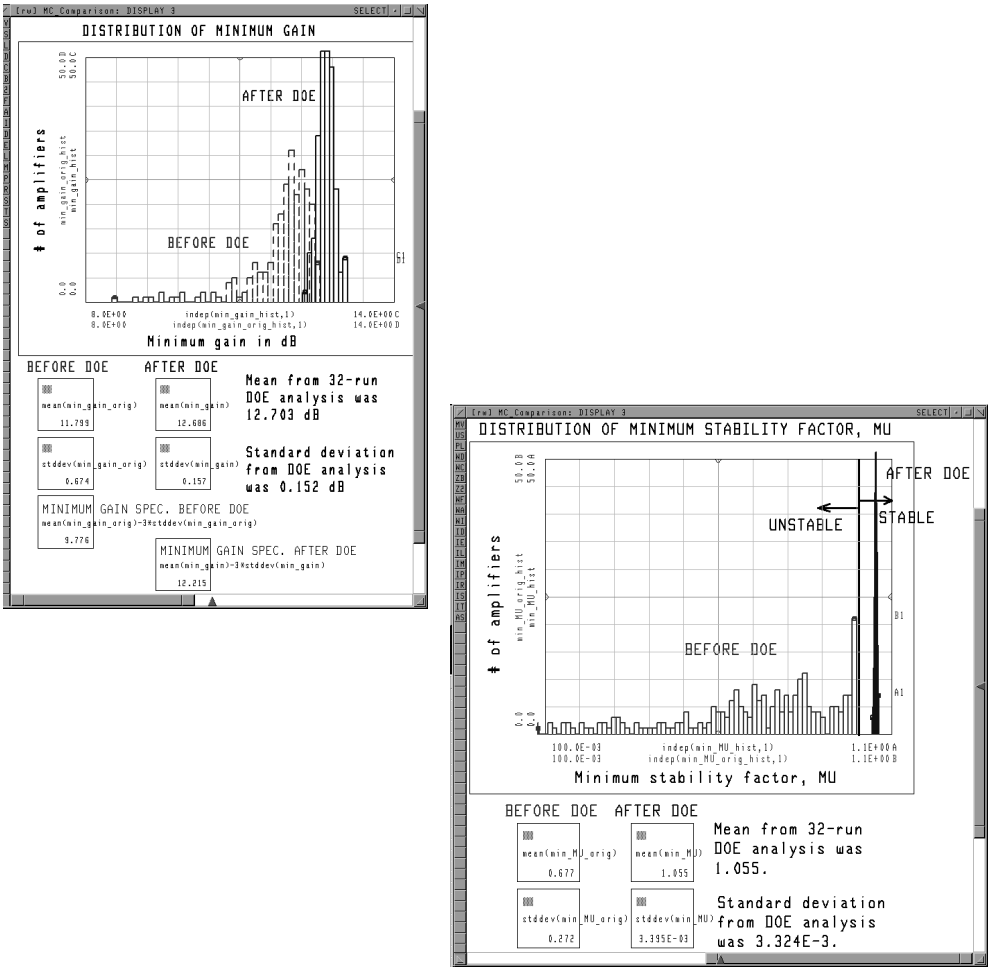


Figure 18. Factors J and K, which model variations in the transistor model's Cjc0, base-collector zero-bias depletion capacitance, and T_F, the ideal forward transit time, contribute the most to variations in gain and stability factor.

The Pareto chart in Figure 18 indicates that the factors Q1.cjcscale and Q1.tfscale, have the greatest influence on both the gain and the stability factor. Note, however, that the 10% assumed variation in each parameter is just a guess. None of the other factors are very significant, which indicates that a 10% tolerance on the design parameters, Factors A through G, should be sufficient.

Figures 19a (minimum gain) and 19b (minimum stability factor) show the results of 250 Monte Carlo simulations of the original circuit and the circuit after applying DOE analysis. Note that even though the mean value of the minimum gain has only improved by 0.9 dB, the standard deviation has been reduced from 0.674 dB to 0.15 dB. Clearly, the DOE-optimized amplifier's gain specification may be set much higher (12.26 dB vs. 9.8 dB, using the mean minus three standard deviations as the specification.) The difference is even larger if the more conservative mean minus six standard deviations are used to set the specification. The results of the DOE analysis agree very closely with the Monte Carlo simulations.



Figures 19a and 19b. Comparison of 250 Monte Carlo simulations of the amplifier before and after applying DOE analysis.

If the large variation in collector current is a concern to the designer, then DOE presentations may be generated with the collector current as the response variable, to determine which factors need to have tighter tolerances to reduce variation in the current. Note that another simulation does **not** have to be run. The DOE presentations may be generated via the menu pick, PERFORM/ UPDATE DOE RESULTS, and entering ICC, the collector current, as the response variable. If the designer wants to keep the original DOE results, then the ICC DOE results could be inserted into a new presentations icon.

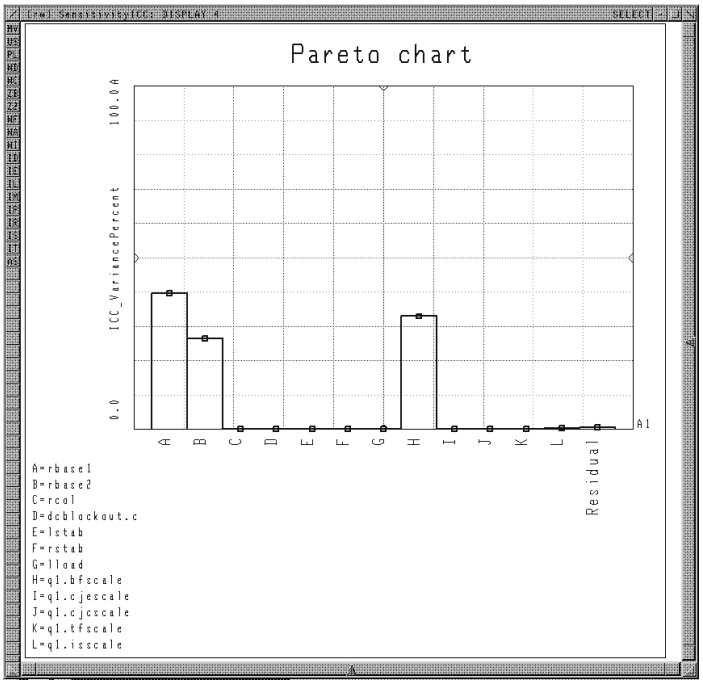


Figure 20. The Pareto chart indicates that variations in Rbase1, Rbase2, and device beta contribute the most to variations in the DC collector current.

Figure 20 indicates that variations in Rbase1, Rbase2, and Q1.bfscale contribute the most to variation in ICC. In order to reduce variation in ICC, the easiest solution would be to tighten the tolerances on Rbase1 and Rbase2, although specifying a tighter tolerance on beta may also be possible. Tightening the tolerances on Rbase1 and Rbase2 to 1% (standard deviation 0.333%) reduces the standard deviation in ICC to 2.4 mA. Now ICC should vary from 18 to 32 mA in production.

Transistor parameters, other than the four included above, could vary and affect the circuit's characteristics. A screening experiment could be run to see which model parameters dominate the characteristics.

Using DOE with Performance Optimization

Steps 3-6 of the application example could be replaced by performance optimization. The parameter values that the optimizer finds depend on the goals of the optimization, and also on the weightings given to each goal. (Refer to the HP MDS/RFDS, Release 6.0 documentation for details on setting up and running performance optimizations.) One of the limitations of using performance optimization on a circuit is that no information concerning a circuit's variability due to process variations is revealed. DOE may be used to evaluate the variability of circuit characteristics due to process and parameter variations, enabling the designer to determine if a solution found by the optimizer is satisfactory, and to better compare solutions found from different optimizations. Also, the nested DOE technique described next can be used to determine whether a better solution can be found near the optimizer's solution.

Depending on the circuit, using performance optimization may be a faster way to find a set of nominal parameter values than DOE, but optimization generally does not provide insight.

Using a Nested DOE Simulation to Find an Optimal Solution

In most circuits, the amount of variation in a circuit's characteristics depend not only on the tolerances of the components, but also on the nominal values of the components. Nested DOE analysis allows a designer to vary the nominal values of many parameters and look for a solution that not only gives circuit characteristics with good mean values but also low variation in the characteristics.

In a nested DOE analysis, the designer chooses "design" parameters, which have nominal values that may be chosen. The designer also specifies process and component tolerances, and typically would choose the high and low values to be one standard deviation above and below the nominal values, as was done in Section 7. A "main" DOE simulation is run, where the design parameters are varied. For each set of factor values in the "main" DOE simulation, a "tolerance" DOE simulation will be run, to see how much the performance characteristics of the circuit vary. From this nested DOE analysis, it is possible to evaluate both the mean values of the circuit performance characteristics and the variability of the performance characteristics, simultaneously.

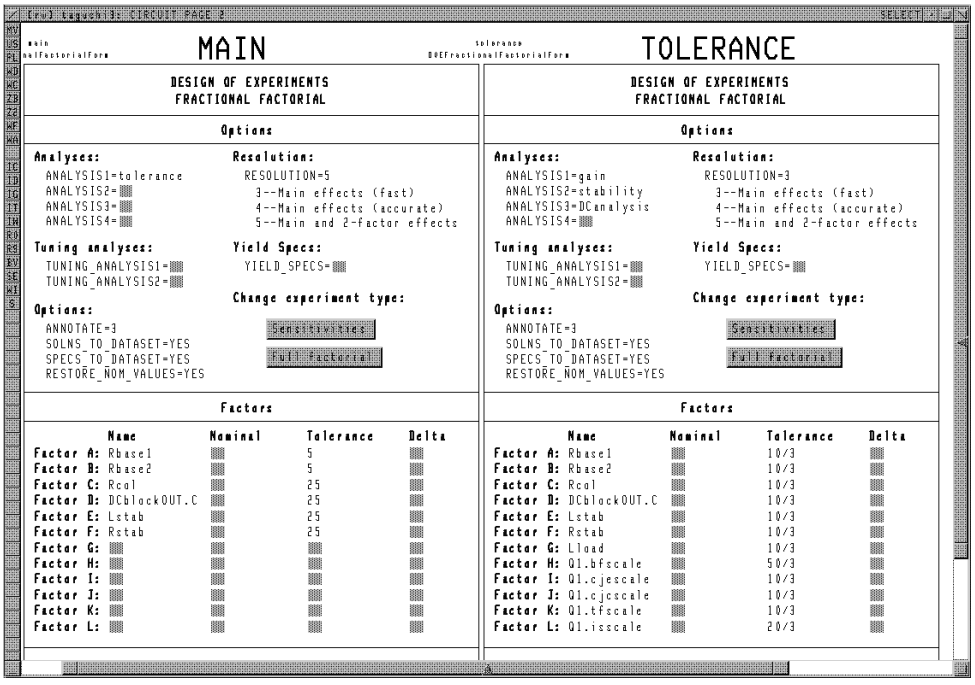
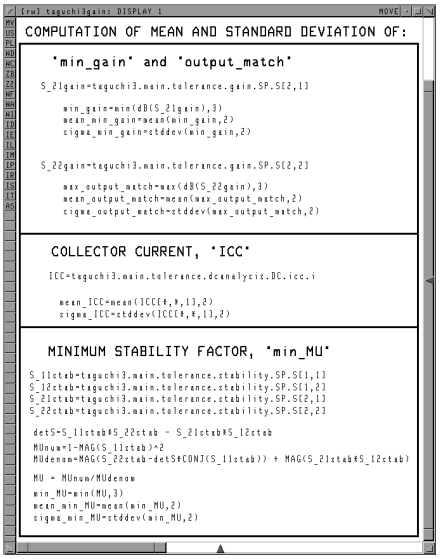


Figure 21. DOE forms for "nested" DOE analysis. Nested DOE analysis allows a designer to vary the nominal values of many parameters and look for a solution that not only gives circuit characteristics with good mean values but also low variation in the characteristics.

Figure 21 shows the configured DOE forms for this analysis. The left DOE form, labeled “main,” lists the “design” parameters, and the right DOE form, labeled, “tolerance,” lists the process and component factors. For each set of factor values in the “main” DOE simulation, the “tolerance” DOE simulation will be run. The “tolerance” DOE simulation will be used to compute the mean value and the standard deviation of each circuit characteristic, for each set of “main” DOE simulation factor values. Figure 22a shows the computations of the mean values and standard deviations of the minimum gain, min_gain, minimum stability factor, min_MU, collector current, ICC, and output match. Figure 22b shows these responses in listing columns. Each row corresponds to a set of factor values in the “main” DOE simulation. Other circuit characteristics could be displayed, also. Each set of factor values in the “main” DOE simulation corresponds to a row in the listing columns.



mean_min_gain	sigma_min_gain	mean_min_MU	sigma_min_MU	mean_ICC	sigma_ICC	mean_output_match	sigma_output_match
12.721	0.160	1.037	2.934E-03	0.026	4.366E-03	-9.924	0.431
12.339	0.249	1.039	3.548E-03	0.018	4.214E-03	-10.652	0.680
12.663	0.147	1.040	3.548E-03	0.032	4.376E-03	-11.944	0.558
12.696	0.164	1.037	2.935E-03	0.025	4.157E-03	-9.851	0.429
12.451	0.153	1.040	3.549E-03	0.025	4.102E-03	-11.866	0.662
12.384	0.229	1.037	2.938E-03	0.018	4.041E-03	-9.532	0.542
12.621	0.142	1.037	2.933E-03	0.031	4.050E-03	-10.554	0.478
12.433	0.157	1.040	3.550E-03	0.024	3.920E-03	-11.718	0.664
12.553	0.163	1.074	4.695E-03	0.026	4.366E-03	-10.413	0.390
12.437	0.246	1.063	4.806E-03	0.018	4.214E-03	-8.278	0.417
12.759	0.145	1.060	4.019E-03	0.032	4.376E-03	-8.972	0.347
12.527	0.167	1.074	4.722E-03	0.025	4.157E-03	-10.349	0.388
12.548	0.151	1.064	4.169E-03	0.025	4.102E-03	-8.953	0.395
12.213	0.234	1.079	5.200E-03	0.018	4.041E-03	-10.084	0.487
12.458	0.144	1.077	4.743E-03	0.031	4.050E-03	-10.978	0.425
12.531	0.155	1.064	4.172E-03	0.024	3.920E-03	-8.873	0.391
12.829	0.159	1.033	2.985E-03	0.026	4.366E-03	-10.652	0.585
12.637	0.242	0.945	0.063	0.018	4.214E-03	-9.550	0.657
12.956	0.144	1.029	2.400E-03	0.032	4.376E-03	-10.843	0.556
12.803	0.163	1.033	2.983E-03	0.025	4.157E-03	-10.529	0.579
12.741	0.149	1.023	0.010	0.025	4.102E-03	-10.728	0.651
12.489	0.227	1.028	0.013	0.018	4.041E-03	-9.992	0.737
12.724	0.141	1.033	2.995E-03	0.031	4.050E-03	-11.628	0.681
12.725	0.152	1.017	0.017	0.024	3.920E-03	-10.579	0.638
12.867	0.158	1.036	0.013	0.026	4.366E-03	-9.371	0.485
12.569	0.243	1.043	0.016	0.018	4.214E-03	-9.438	0.609
12.889	0.144	1.050	3.631E-03	0.032	4.376E-03	-10.563	0.497
12.842	0.162	1.029	0.018	0.025	4.157E-03	-9.274	0.483
12.676	0.149	1.054	3.758E-03	0.025	4.102E-03	-10.479	0.582
12.530	0.225	0.948	0.062	0.018	4.041E-03	-8.813	0.639
12.764	0.140	1.049	3.963E-03	0.031	4.050E-03	-10.134	0.549
12.659	0.153	1.054	3.760E-03	0.024	3.920E-03	-10.351	0.574

Figures 22a and 22b. Results of “nested” DOE analysis. This analysis allows a designer to consider both the mean value of a response and its standard deviation simultaneously.

Generally, designers must consider several different circuit characteristics and make trade-offs when choosing circuit parameter values. In this example, it is desirable to maximize the gain and the stability factor, and minimize the collector current and output match. It is also desirable to minimize the variability of all circuit characteristics. It is easier to analyze the data and make trade-offs, when it is displayed all at once, as in Figures 22a and 22b. DOE presentations may be generated for two response variables at a time, enabling the designer to better make trade-offs.

Using DOE with SMT Library Parts

Many designers may want to use DOE to design circuits with surface mount technology (SMT) parts. The easiest way to do this is to use DOE or performance optimization on a circuit with lumped-element components, until a satisfactory set of nominal factor values has been found. Then, convert the components to the SMT models that have the closest nominal values. The circuit should be resimulated to see whether its performance is still satisfactory or not, as there may be some degradation due to parasitics. If the performance is no longer satisfactory, a performance optimization or DOE analysis should be run, as described earlier. An SMT component and the equivalent circuit it represents are shown in Figure 23.

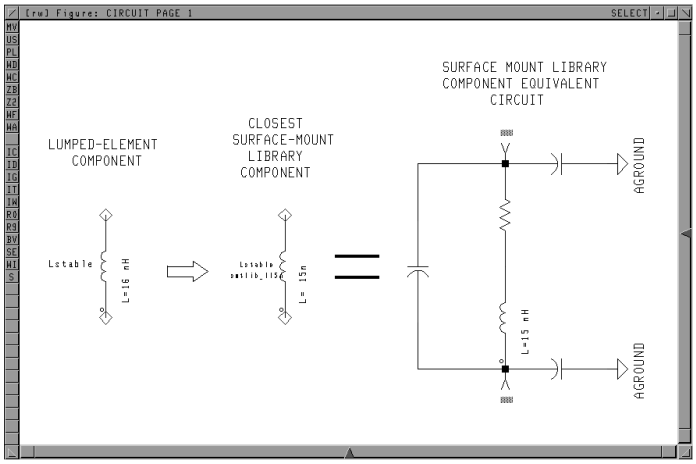


Figure 23. An SMT library component and the equivalent circuit it represents.

The amplifier with SMT library components is shown in Figure 24. The DOE analysis form used for analyzing the variation in the characteristics of this circuit, is shown in Figure 25. The factor, Rb1.rscale, scales the nominal value of resistor, Rb1. When rscale=1, the resistor has its nominal value. When rscale=0.9, the resistor is 10% below its nominal value.

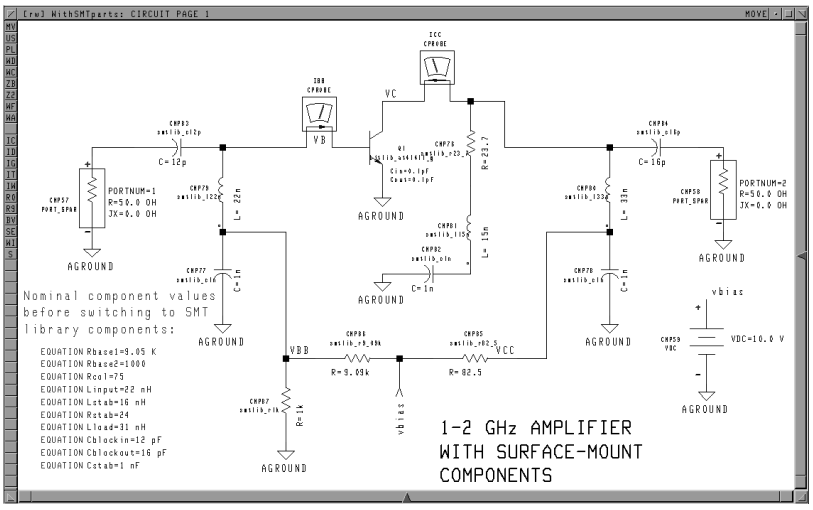


Figure 24. Amplifier with SMT library components.

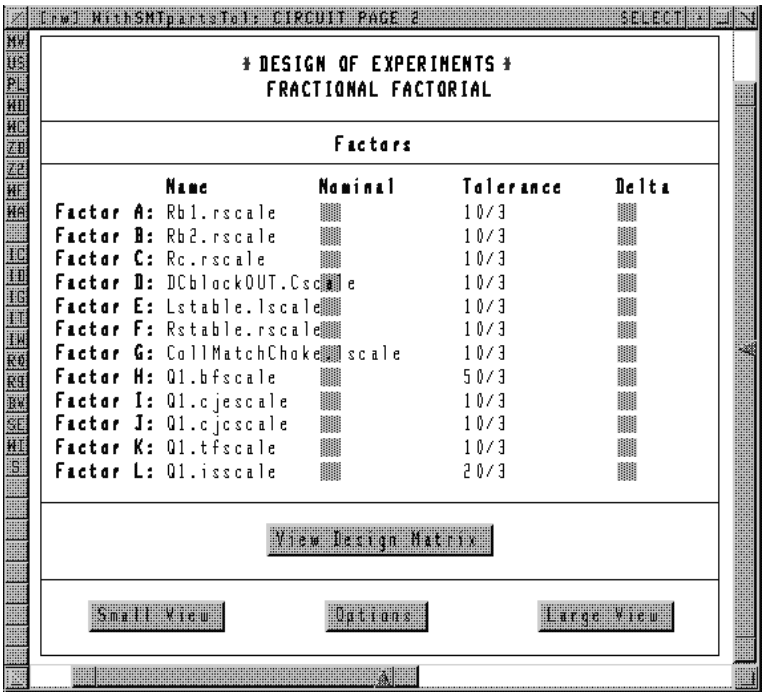


Figure 25. DOE analysis form filled in to analyze the variations of the circuit in Figure 24.

Summary and Conclusion

This product note describes the benefits of the Design of Experiments (DOE) analysis technique, shows how DOE works, and covers in detail the application of DOE to a design. In the amplifier design example, DOE reveals what parameters to vary to improve the circuit. In particular, it shows that in the original amplifier, varying the stability resistor does not affect the stability! It also shows what parameters do affect the stability and how to vary them. DOE shows that the original output DC-blocking capacitor is too small, making the circuit potentially unstable. After finding a good nominal solution, the effect of component (including the transistor) variations is investigated, also using DOE analysis. A comparison with a Monte Carlo simulation shows that the DOE simulation predicts the same response mean values and very similar standard deviations. The DOE simulation also shows that variation in circuit gain is primarily due to transistor variation, which means that tightening tolerances on other components in the circuit would lead to little improvement.

Nested DOE analysis was also described, which enables a designer to take parameter variations into account when looking for an optimum solution. For example, a designer may use DOE to modify circuit parameters to both improve the gain of an amplifier and minimize the variance of the gain. Using DOE with performance optimization and with surface mount components is also described. The appendices cover basic DOE concepts.

DOE is a powerful analysis tool that quickly shows a designer whether a circuit will perform as required, including the variability seen in manufacturing. If the circuit will not perform as desired, DOE can reveal what changes should be made, as well as any trade-offs that might be necessary.

Appendix A: What are Parameter Interactions?

A parameter interaction is present when the change in a circuit's response due to changing parameter A depends on the value of parameter B. For example, suppose that parameters A and B are resistors in an amplifier circuit, and the DOE experiment below is run.

Run #	Resistor A	Resistor B	Gain
1	900	450	9dB
2	1100	450	10dB
3	900	550	9.5dB
4	1100	550	12dB

There is an interaction present between resistors A and B, because the effect on the gain due to increasing Resistor A from 900 to 1100 ohms is only +1 dB when resistor B is 450 ohms, but the effect on the gain is +2.5 dB when resistor B is 550 ohms.

In the interaction plot of Figure 12 on page 15, the lines for the response variable, min_gain, are not parallel, which means that there is an interaction occurring between Factors A and B. In other words, the effect on min_gain due to changing Factor A depends strongly on the value of Factor B.

Appendix B: DOE Basic Theory

DOE uses the results of an experiment (in this case, the experiment is a set of simulations) to compute the coefficients of a polynomial equation that approximates each response variable in terms of factors and interactions among the factors. The results of these computations are displayed in the DOE outputs described above. For a simple, two-level full factorial experiment[5], depicted in Figure A, the polynomial equation for the response variable, Y, is:

$Y=c_0 + c_A*A + c_B*B + c_{AB}*AB$

In the equation for the response variable, A and B are "coded" variables. For example, if Factor A is a 1 Kohm resistor, and its low value in the DOE experiment is 900 ohms and its high value is 1100 ohms, then setting the resistor value to 900 ohms would correspond to setting A equal to -1 in the equation, and setting the resistor value to 1100 ohms would correspond to setting A equal to +1. AB is the product of the two coded variables A and B.

The full factorial design matrix for the experiment is:

Run Number	FactorA	FactorB	Circuit Responses
1	-1	-1	r1
2	+1	-1	r2
3	-1	+1	r3
4	+1	+1	r4

c_0 is the mean value of the response variable, or (r1+r2+r3+r4)/4.

c_A is the half effect of Factor A, and is computed as one-half the difference between the mean value of the response when A is +1 and the mean value of the response when A is -1, or {(r4+r2)/2 - (r3+r1)/2}/2.

c_B is the half effect of Factor B, and is computed as one half the difference between the mean value of the response when B is +1 and the mean value of the response when B is -1, or {(r4+r3)/2 - (r2+r1)/2}/2.

c_{AB} is the half interaction of Factors A and B, and is computed as one half of the difference between the half effect of Factor A when Factor B is high, and the half effect of Factor A when Factor B is low, or {(r4-r3)/2 - (r2-r1)/2}/2.

The design matrix is interpreted as follows: for run number 1, Factors A and B are set to their low values, and the simulation is run, with "r1" being the computed value of the response variable. For run number 2, Factor A is set to its high value and Factor B is set to its low value, and the simulation is run, with "r2" being the computed value of the response variable. The experiment continues until the response variable has been computed for all four possible combinations of the factor values.

The ANOVA table displays these computed coefficients (although what it calls "effects" are really the "half effects" described above), the mean value of the response, the relative contributions of each factor and interaction to the variance of the response variable(s), and other information. The relative contributions of each factor and interaction to the variance of the response variable(s) is also displayed in the Pareto chart. If the relative contribution of Factor A is much larger than that of Factor B, then Factor A should be changed to shift the response variable in the desired direction.

[5]A full factorial experiment is one in which there is a simulation for each and every combination of factor values.

The equation for the response variable may be used to extrapolate responses for other factor values outside the range used during the DOE simulation. The more linear the relationship between the response variable and the factors, the more accurate such an extrapolation is. However, caution should be used if the response is assumed to be highly non-linear and the extrapolation is large.

When a fractional factorial experiment is run, fewer sets of factor values (runs) are used, so the experiment is shorter. The trade-off is that less information is obtained from the experiment, because aliasing (also called "confounding") occurs. For example, if a third factor were added to the experiment above, but the designer did not want to increase the number of simulations, then the design matrix might look like this:

Run number	Factor A	Factor B	Factor C	Circuit Responses
1	-1	-1	+1	r1
2	+1	-1	-1	r2
3	-1	+1	-1	r3
4	+1	+1	+1	r4

Also, the equation for the response variable would have additional terms including the effect of Factor C and interactions of Factor C with Factors A and B:

$Y=c_0 + c_A*A + c_B*B + c_C*C + c_{AB}*AB + c_{AC}*AC + c_{BC}*BC + c_{ABC}*ABC$

In order to compute all of the coefficients in this equation, it would be necessary to run a full factorial experiment. Fractional factorial experiments are designed to compute the most significant information with the highest accuracy. The most significant information is always assumed to be the mean value of the response variable and the main effects of the factors (main effects are directly proportional to the coefficients, c_A, c_B, and c_C). The main effects may be computed from the above experiment, but the interactions cannot be distinguished from the main effects. This is because, for example, the computation of the main effect of Factor C is the same as the computation of the AB interaction. (To understand why this is true requires knowledge of orthogonal arrays which are covered in Reference 2.) The same is true for the other interactions. Aliasing is this inability to distinguish main effects from interactions (and also the inability to distinguish low-order interactions from higher-order interactions). In most circuits, third- and higher-order interactions are usually insignificant, so main effects of factors are aliased with these, first.

When a fractional factorial experiment is chosen, the designer may choose the "resolution" of the experiment. ("Resolution" is also covered in Reference 2.) The higher the resolution, the less the aliasing, but the greater the number of simulations that must be run. The designer may view the design matrix and see what effects and aliases occur by selecting the "View Design Matrix" button on the Design of Experiments form. This form and its use are described in the application example, above.

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