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GLOBAL BUSINESS IDEAS AND INFORMATION FOR MANAGERS AND TEST ENGINEERS



WLAN PROMISES MOBILITY IN THIS FAST-PACED WORLD

By eliminating the physical constraints and installation of wires—which can be expensive, time-consuming, and often disruptive—WLANs offer a variety of benefits, including ease of installation, flexibility, cost-savings and mobility.

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Agilent Technologies

A view from Asia: Riding the innovation wave

By Bharat Kulkarni, managing editor



Bharat Kulkarni is Asia-Pacific marketing manager, based in Hong Kong, for Agilent's Automated Test Group.

By now you have been bombarded with news about the demise of the dot-coms, the global economic slowdown, and how deep and broad this semiconductor downturn is turning out to be. Looking past this grim reality, I see an interesting paradigm shift occurring in the Asian semiconductor industry. The leaders of tomorrow will not be governed by how strong or intelligent companies are, but by their ability to innovate and respond to change. Innovation is the economic growth engine that will pull us out of this downturn and help companies create a competitive advantage.

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Historically, Asian technology companies have provided a low-cost manufacturing value proposition to their U.S. and European counterparts. The tide, however, is changing dramatically as Asia develops its own intellectual property (IP), and as open standards help distribute hi-tech knowledge globally.

Taiwan has been traditionally recognized for its cost-effective electronic manufacturing process. In recent years, TSMC and UMC have pioneered the "dedicated foundry" concept that supports fabless semiconductor companies. Today, developing the manufacturing process is no longer the differentiator between chipmakers that it once was. IP and system knowledge are now the true battlegrounds. These leaders are innovating with new value propositions for their customers, e.g., by offering leading-edge process technologies and proven IP to fabless companies and Integrated Device Manufacturers (IDMs).

Innovation is also driving increased design activity with fledgling design communities across Asia that are mushrooming at a rapid pace. Design houses in Taiwan like Faraday (leading supplier of silicon-proven IP and SOC design services) and VIA (leading supplier of PC chipsets and microprocessors) are a product of this evolution. I expect Taiwan's semiconductor business to go through a metamorphosis, where the existing manufacturing base will be complemented with a focus on high value-added design services.

China today is heavily dependent on imported microelectronic products, as it only produces 10 percent of its needs. Chinese subsides on producing "local-content," which are attracting semiconductor companies from around the world looking to establish a foothold in China. Leading test houses, e.g., Amkor, ASET and ChipPac, recognizing potential opportunities, have established a presence in China. Shanghai and Beijing have been endorsed recently by the central Chinese government to build national microelectronic industrial centers. Semiconductor Manufacturing International Corp. (SMIC) and Grace Semiconductor Manufacturing Corp. (GSMC) are two up-and-coming foundries in Shanghai. A third foundry that is under development is Huaxia Semiconductor Manufacturing in Beijing. Hong Kong and Taiwan will become the springboard for business communities into the largely untapped Chinese market. This will be further facilitated with China's imminent entry into the WTO.

Singapore, which traditionally had an IT focus, has evolved in recent years by joining the foundry frenzy.

Continued on page 19

DID YOU ? KNOW

Silicon Valley jargon

Text message injury (TMI)

Repetitive stress injury caused by excessive use of the thumbs to type messages into a mobile phone or pager.

Community mobility

A shared neighborhood transportation system of various vehicles (from bikes to electric cars and minivans) created out of concern for the environment.

Apology bonus

Cash paid by technology companies to students they promised to hire but can no longer afford to put on the payroll.

Passface

In biometric security system, a face scan, used instead of a password.

Source: Wired *magazine*

The virtues of a standard test platform

A strategy that was initiated several years ago to make testing as simple as possible across both manufacturing and development facilities—the standard test platform—has now become a reality for the Semiconductor Products Group (SPG).

SPG is an internal Agilent group that essentially is a "customer" to Agilent's Automatic Test Group, which manufactures the Agilent 93000 test system.

At the core of the strategy is this common tester platform that allows the user to choose a tester configuration and capability depending on exactly what is to be tested, at what speed and at what coverage. The single platform offers a wide range of capability. As additional capability becomes available, the pin cards that are used for testing can easily be swapped out directly on the test floor.

An engineer employing this common tester platform can choose whatever kind of pins desired—analog, mixed signal, communications, and digital embedded memory. All may be used in the same platform, and new pins can be added as needed. Scalable architecture allows for pay-per-use speed, memory upgrades, higher utilization, increased reliability, smaller footprint, and increased longevity and stability.

This Agilent 93000 common test platform "is the new standard," said Agilent's Atul Goel, R&D manager for the Intelligent Test Solutions division. "Flexibility enables the Agilent 93000 to excel in situations where unpredictability and high channel mix predominate," he said, adding that other Agilent test systems are now being merged into this 93000 system.

"Agilent's architecture in this common test platform is unique," said Goel. "Each of our pins on a package (per-pin-architecture) allows us to pull out one set of pins and put in another, thus enabling us to test a different type of chip as the product mix changes. Also, since this flexible architecture allows one to mix any type of test capability, and the testing resources are distributed per pin, the entire chip can be tested concurrently as opposed to the typical sequential approach. And since the tests can be run concurrently, the platform allows for much more rapid testing—up to 50 percent faster," Goel said.

The result is a tester that is both scalable and reconfigurable.

Agilent's ability to test 32 to 64 parts of a chip at the same time is unique in the industry, delivering faster throughput and lower cost.

Standardizing on one platform for immediate and future test needs will go a long way toward helping fabless designers and IDMs meet their cost and time-to-market goals, Goel said. Standardization considerably lowers training and development costs while maximizing software and hardware development.

"The Agilent 93000 SOC Series provides customers with the flexibility to test a broad range of applications. This results in higher system utilization and reduces the number of test systems required on the manufacturing floor. It also minimizes the number of platforms that require support, thereby lowering cost of ownership," Goel said. ◆

DID YOU ? KNOW



Why do women's blouses have the buttons on the left?

Men's shirts have the buttons on the right, but women's blouses have the buttons on the left. This is more than just a way to tell whether a shirt is for men or women. There is a historical reason for it.

During the Victorian period, buttons were quite expensive, and were mostly worn by rich people. Since proper, well-to-do ladies were dressed by their servants, and most people are right-handed, their buttons were placed on the servant's right, which is the wearer's left side. However, most gentlemen dressed themselves, so their buttons were placed on the wearer's right side.

Those who could not afford servants copied the style of the wealthy, and women's buttons thereafter remained on the left.

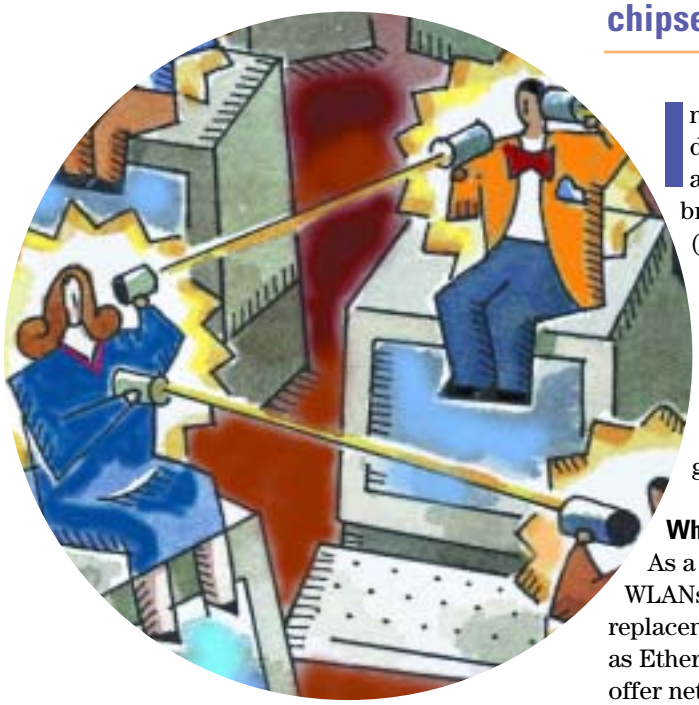
A success story

The standardized test platform has been seen as a great success story. Over a five-year period:

- Utilization rates have improved from -60 percent to more than 95 percent
- The test rate/hour was reduced by more than two times.
- Cycle times are decreased by about two weeks in the sort and final test

WLAN promises mobility in this fast-paced world

The residential market is the fastest growing segment of the wireless LAN business, with residential WLAN chipsets accounting for 47 percent of all WLAN chipset sales



The constraints of a wired world

Interoperability, increased data rates, and lower cost are all working together to bring Wireless LANs (WLANs) and their promises of mobility, flexibility, and scalability to both enterprise and home users. Despite a world-wide economic slowdown, WLAN continues to be a high growth application.

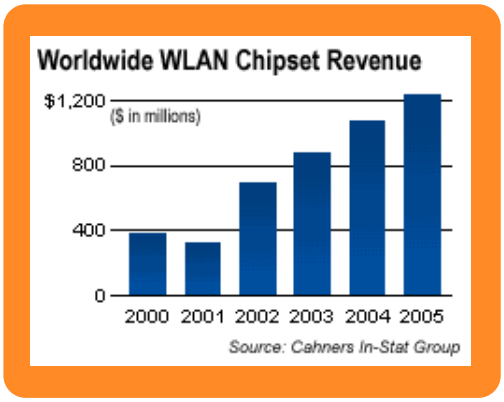
What is WLAN?

As a simple explanation, WLANs are an extension to or a replacement for wired LANs, such as Ethernet or IEEE 802.3, that offer network access anywhere, anytime. To be specific, WLAN is a high bandwidth, two-way data communication network. WLAN operates over a limited distance, up to approximately 300 feet, and uses radio as the transmission medium rather than copper cable or optical fiber.

By eliminating the physical constraints and installation of wires—which can be expensive, time-consuming, and often disruptive—WLANs offer a variety of benefits:

- Ease of installation
- Flexibility
- Scalability
- Cost savings
- Mobility

Installing a WLAN network is as simple as connecting an access point to a wired network and plugging network interface cards (NICs) into all PCs, laptops, PDAs, printers and other devices that require access to the network. No new network cables need to be installed in walls, floors, and/or ceilings to connect the different devices, saving on labor and minimizing disruptions. Furthermore, changing the location of network devices—or adding devices such as additional printers—is quick and easy. Those users with WLAN-equipped portable computers can roam around the building, and will have continuous access as they are handed off from one access point to another.



A Wireless LAN success story

One major attraction of WLAN is cost savings, as the University of Michigan Business School has discovered. The school spent just $50,000 to set up its seven buildings. “Doing the same with cables would have cost seven figures,” says Edward Adams, director of computing services.

Conventional networking means bringing cables in underground, then stringing them through walls and ceilings to every desk or cube where a personal computer sits. “One estimate for wiring a 170-seat classroom in an older building ran $200,000,” says Adam.

Source: Business2.com

The future of WLAN

WLAN chipsets are expected to have a high growth rate, with 31 percent CAGR from 2001 to 2005. A key driver for the growth will be applications for the home user. According to Cahners' *In-Stat*, the residential market is the fastest growing segment of the wireless LAN business, with residential WLAN chipsets accounting for 47 percent of all WLAN chipset sales by 2005, a total of more than 21 million units.

As WLAN grows in popularity, many different public facilities are installing access points to provide Internet services in a variety of locations outside of the home. Whether you're waiting at the airport or train station—or getting coffee on a Monday morning—you can pull the latest information you need from the Internet. Even Starbucks and other commercial establishments are becoming WLAN-equipped—ensuring you have network access anytime, anywhere.

Multitude of WLAN standards

The numerous standards for WLAN have gone through many changes in specifications and requirements. As can be seen in the table on the right, there are basically 2.4 GHz and 5 GHz standards. Today, IEEE 802.11b is the most popular.

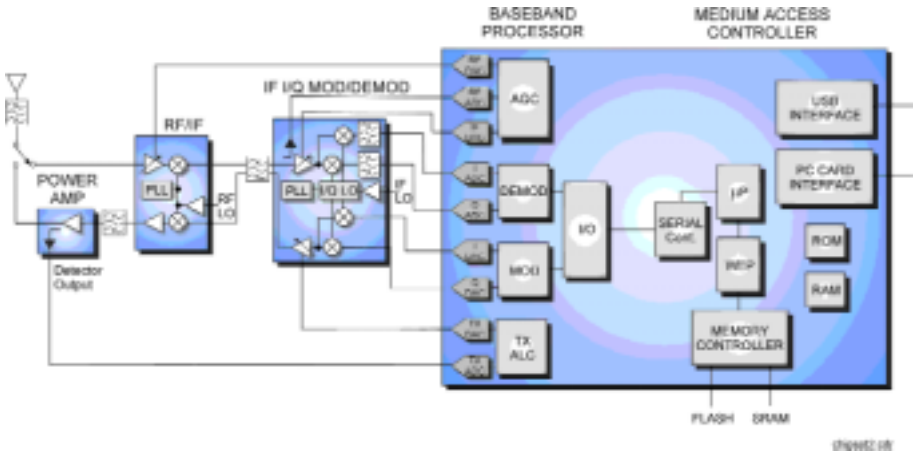
"We expect that 802.11b will be the predominant wireless home networking protocol over the next few years," says Navin Sabharwal, ABI vice president of Residential and Networking Technologies. Five GHz standards, such as IEEE 802.11a, with higher data rates and a less crowded spectrum, are rapidly gaining popularity. IEEE 802.11a devices will be available in the next year and are expected to surpass sales of 2.4 GHz devices in 2005.

WLAN chipset

A typical chipset partitioning today for a WLAN module is shown below. As with all other wireless markets, integration levels continue to increase. The chipset has already been reduced from five chips to four with the integration of the baseband processor and medium access controller onto a single chip. In the future, some WLAN chip manufacturers will use direct conversion technology to combine the RF/IF and Modulator/Demodulator chips into one, reducing the number of chips even further. But it does not stop there—more integration is expected. A single chip solution (excluding the power amplifier) is anticipated by the industry. Also, support for multiple modes—such as 802.11a and 802.11b—in a single chipset will be offered. In fact, such chipsets are available today—ensuring the ultimate in coverage. Increasing functionality on fewer chips ultimately results in unprecedented chip complexity.

The evolving standards, increasing chip complexity and price erosion are challenging the semiconductor industry. However, WLAN has a bright future if these hurdles can be overcome. ◆

Standard	Frequency	Data Rates	Volume Ship
IEEE 802.11b	2.4 GHz	1, 2, 3,5, 11 Mbps	1999
IEEE 802.11g	2.4 GHz	22 Mbps	Pending FCC decision
HomeRF 1.0	2.4 GHz	1 or 2 Mbps	2000
HomeRF 2.0	2.4 GHz	10 Mbps	2002
IEEE 802.11a	5 GHz	6, 9, 12, 18, 24, 36, 48, 54 Mbps	2003
ETSI HiperLAN 2	5 GHz	6, 9, 12, 18, 27, 36,54 Mbps	2003



DID YOU ? KNOW



Who built the first paved road?

To build their monuments and temples, the ancient Egyptians needed huge blocks of black basalt, which they floated to Giza (just outside Cairo) using wooden barges on the Nile River. But how did they get the blocks of stone from the quarry to the water, which was about seven miles away (11 km)?

They solved the problem by building what may have been the world's first paved road. The six-foot wide (1.8 meter) road was paved mostly with flat slabs of sandstone and limestone. Because there are no grooves on the ancient stones, it is thought that the blocks of basalt were moved on rollers.

STATS acquires majority interest in Taiwan test house

Takes 51 percent stake in Winstek to capture growing outsourcing opportunities in Taiwan semiconductor market

A leading independent semiconductor test and advanced packaging service provider, ST Assembly Test Services Ltd (STATS), has acquired a 51 percent interest in Winstek Semiconductor Corporation, Taiwan, a specialist test house located in Hsin-Chu Hsien, Taiwan.

STATS subscribed to new shares issued by Winstek for a total of approximately U.S. $28 million.

Winstek, a private company incorporated in April 2000, has capabilities to test optical, mixed-signal, digital and radio frequency (RF) devices. It provides an integrated range of services including wafer probe, final test, turnkey and drop shipment services.

The company has a plant at Hsin-Chu Hsien, Taiwan and a technical support office in San Jose, California. Winstek will continue to be led by Richard Weng , its chairman and president.

"Winstek is very excited to have STATS as our partner and majority owner," Weng said. "STATS has a leading position in the outsourced test and assembly semiconductor industry with a particularly strong reputation in mixed signal testing. With STATS' technological expertise and financial strength behind us, we are confident we can grow to become one of the leading test houses in Taiwan."

Tan Bock Seng, STATS chairman and CEO, said, "Our investment in Winstek provides STATS with a strategic foothold to capture the growing outsourcing opportunities in semiconductor test and assembly services in Taiwan. STATS and Winstek will be able to serve our existing customers better and develop new businesses with companies that take wafers from fabs in Taiwan."

Taiwan is the home of the world's two largest foundries. It is also the second largest fabless semiconductor ICs design base in the world.

"Our investment in Winstek is our first strategic step and we will continue to explore investment opportunities in Taiwan," said Tan. ◆

Chip design firms are trying to raise industry's profile

Several Singapore chip design companies, supported by the Economic Development Board (EDB), will meet monthly to raise the industry's profile, ignite students' interest in the field and sharpen the Singapore semiconductor industry's competitive edge.

Senior executives from 15 integrated circuit (IC) design companies voiced their major concerns at a recent meeting, and common to all is the difficulty they have finding and keeping IC design engineers. The root cause, they say, is the lack of community spirit and less-than-glamorous perception of chip designers.

eMicro president and CEO Michael Holt said: "There is no connectedness here. In San Jose, people get together often, formally or informally. And you can really feel the excitement, the buzz there."

Holt reckons the buzz is lacking because Singapore IC designers are

Continued on page 7

Intel to set up two design centers for processors in Malaysia

The world's largest chipmaker, Intel Corp., recently announced the setting up of two design centers in Malaysia which will see local engineers and designers from Intel Malaysia create and design future microprocessors for next generation personal computers (PCs) and networks.

Intel Corp. President and CEO Craig Barrett said one of the centers will be used to develop future generation processors while another is a network processor design center, which is the first such center in Asia as well as the first outside the U.S. and Israel.

"The facility here already has the experience in various Intel technologies, so it is just moving into the next complex microprocessor capability," Barrett said. "Engineers from Intel Penang have been working closely with engineers in the U.S., so, it is logical to give independent control for Penang engineers to design and develop microprocessors."

Barrett said initially 100 local engineers will be employed at the design centers and the number will be increased "significantly" later. "Products from these design centers are expected to hit the market in 2003," he said.

The design centers witness Intel moving onto a higher technology ladder as it is adding value to its existing manufacturing-based to engineering-based activities.

"We intend to make Malaysia a significant cornerstone in manufacturing technology as we are moving from testing the technology, assembly and packaging, and now we use the facility for engineering capability."

Barrett said Intel Malaysia has also been selected to assemble, test and package the Intel Pentium 4 processor, the company's highest performance microprocessor for desktop computers.

Intel Malaysia has a combined workforce of 8,000 people, with cumulative investment since 1972 amounting to nearly U.S. $2 billion. Analysts believe that Intel's bold move in the wake of the U.S. economic slowdown and downward cycle in the global electronics sector will enhance business confidence in Malaysia, especially the multinationals which have been affected by the slowdown. ◆

Source: Business Times (Malaysia)

Industry profile

Continued from page 6

used to getting assignments from their head offices, say, in the U.S. They were not driving the solutions.

A large number of IC designers are foreigners who can pack up and go any time. Future Techno Designs CEO P. Bala said: "Because there is no cluster ambiance, the ambitions of these foreigners are not met. That's why they leave."

Last year the semiconductor industry made up 30 percent of the electronics sector, which, in turn, contributed 52 percent of Singapore's gross domestic product. In 2000, the sector's output was U.S. $24.8 billion, up 73 percent. It employs some 30,000 people. Besides 31 IC design companies, there are 14 wafer fabs and 18 assembly and test companies here. ◆

Source: The Business Times

DID YOU ? KNOW

Where are the fastest steady winds in Earth's atmosphere?

The fastest winds are the jet streams, high altitude rivers of air that circle the planet in the northern and southern hemispheres. These long, thin air flows can reach speeds of more than 300 miles per hour.

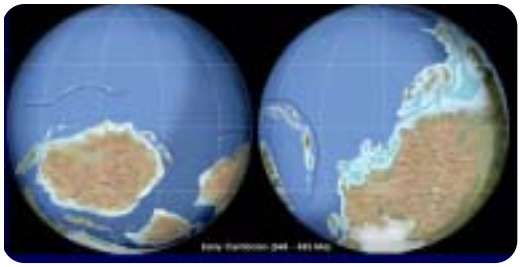
There are two jet streams on each side of the equator (sometimes three in the northern hemisphere). They flow from west to east at the edges of major air masses, where storms are formed.

The jet streams were first discovered by airmen during World War II. They are the main cause of "clear air turbulence," which sometimes shakes up passengers in high-flying planes.

This photograph taken from about 320 kilometers (200 miles) above the Earth shows a band of cirrus clouds produced by a westerly jet stream that stretches across the Red Sea from Sudan to Saudi Arabia. The contained uniformity of the cloud formation reflects the narrow track of the jet stream moving from left to right across the frame.



DID YOU ? KNOW



A paleogeographic view of the Earth from both the northern hemisphere (left) and from Asia. This is the early Cambrian period, 545—535 Ma.

When was there only one giant continent?

Throughout Earth's history the continents have been moving around, pushed by deep currents of semi-liquid rock. About 400 million years ago all the land masses came together to form one single continent. In those days plants had just started coming onto land, along with primitive scorpion-like creatures.

The huge land mass called Pangea formed when the two smaller continents Gondwana and Laurasia slowly merged, a process which took millions of years. After more millions of years, Pangea began to break apart and some of the continents we have today were formed.

About 95 million years ago, today's continents of Africa and South America split apart, forming the Atlantic Ocean. About 55 million years ago, the subcontinent of India pushed up against southern Asia, forming the magnificent Himalaya mountains.

Tamarack Microelectronics selects Agilent's SOC test system

Will test QoS Ethernet switch controller with embedded memory

High-performance data communication solutions provider Tamarack Microelectronics Inc. (TMI) has selected Agilent 93000 SOC C200e model test system as its test standard. This model will offer wide-spread application coverage to TMI in next generation network IC test platform. TMI is the first C200e model customer in the Greater China Region.

TMI designs, researches and manufacturers analog and digital mixed-signal ICs for the data communication communities. TMI solutions are incorporated into many products of major networking manufacturers around the world. In view of the promising outlook of LAN demand, TMI is expanding its Giga Ethernet Switch Controller production.

The newly released 16 ports 10/100Mbps QoS Switch controller with embedded memory, TC6216M, outperforms the unmanaged switch controller by providing features usually associated with managed switches at very high performance levels. It provides leading edge QoS with three levels of priority. TC6216M significantly improves the availability and bandwidth for a store and forward switching method used in nonblocking architecture.

TMI selected Agilent testers for its proven SCAN and embedded memory testing. It provides a cost-effective solution and the single scalability to meet current and future upgrade requirement. Agilent's 93000 SOC series is the sole tester in the market to test the broad range of applications. With the multi-site testing capability and compatible software/fixture throughout all platforms, Agilent provides the most economic and technical solutions that support TMI's commitment to provide the most cost-effective Ethernet solutions at a variety of performance points.

TMI soon will volume ship the next generation network ICs to serve Greater China Region customers in communications industries. "TMI is in good shape to introduce the leading-edge high speed networking communication solution. Agilent's 93000 testers help TMI to improve productivity and reduce fault coverage. We expect NT $250M revenue will come from 100 Mbps QoS Switch controller with embedded memory this year," said Frank Chuang, TMI Marketing Director.

Agilent's 93000 SOC series will assist TMI with cost-effective SCAN and embedded memory test capabilities, said Chuang. ◆

Samsung begins mass production of third-generation 256Mb Rambus DRAM

Samsung Electronics, the world's largest memory chip maker, has started mass production of third-generation 256Mb Rambus DRAM chips, signaling its move away from 128Mb chips. Samsung's latest technology utilizes a 0.15micron procedure, empowering its 256Mb Rambus DRAM with 1GHz processing speed.

The 0.15micron-based production is the latest in a series of developments in the technology. The first-generation DRAM used a 0.19 micron procedure and the second-generation opted for 0.17 micron.

The chipmaker said it expects 256Mb Rambus DRAM will take center stage in the chip market from late this year.

The 0.15micron technology applied to 256Mb Rambus DRAM production improves the chip output per wafer by 30 percent compared with 0.17 micron, while the internal signal processing speed has been also upgraded from 800MHz to 1GHz or faster.

Samsung said it has also reduced the size of the new 256Mb Rambus DRAM chips, ensuring their price competitiveness in comparison to SDRAM.

Samsung expects that its Rambus DRAM chips will take a central role in the market for memory chips for mobile, entertainment and interactive communications digital media, the demand for which is expected to jump in coming years, despite falling PC sales.

Samsung controls about 60 percent of the global Rambus DRAM market.

The company plans to mass produce the fourth-generation Rambus DRAM based on 0.13 micron technology at the end of this year. It also plans to produce 4Bank Rambus DRAM chips in the first half of next year.

The 4Bank Rambus chips are 3 percent smaller than SDRAM chips, making them 10 percent cheaper than their DDR counterparts when mass produced, suggesting a faster penetration in the market, Samsung said. ◆

Source: Korea Herald

Hynix to sell flat-panel unit

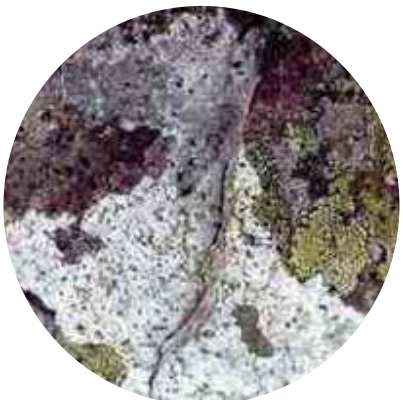
South Korea's Hynix Semiconductor Inc. has agreed to sell an 80.1 percent stake in its wholly owned flat-panel display unit for $570 million to a consortium led by Taiwan's Cando Corp.

Hynix company will receive $400 million in cash by November, the company said. After the deal, Hynix will hold 19.9 percent of the flat-panel display unit.

Cando and Hynix will set up a joint venture company to run the unit, which produces thin film transistor liquid crystal displays, or TFT-LCDs. The flat-panel displays are commonly used in notebook computers and television sets designed to be hung on a wall. Cando specializes in producing color filters for TFT-LCDs.

Hynix's was formerly known as Hyundai Electronics Industries Co. ◆

Source: Associated Press



Crustose lichens: A patchwork of lichens on a rock surface, including several colonies of the green-colored Rhizocarpon geographicum and the white Lecidia species.

DID YOU ? KNOW

What kind of organism is made of a fungus and an algae?

The crusty lichens that grow on rocks are actually two different organisms in close partnership. By cooperating and sharing, they can grow together in places where no other life forms can take hold.

The main body is made out of fungus threads (hyphae), which anchor the lichen to the rock and grow into various leafy or crusty shapes, depending on the species. Embedded in the mass of fungus threads are algae cells, protected and supplied with nutrients by the fungus.

The lichens are actually dissolving the rock they're on. Little by little, the acids and other substances they secrete seep in between cracks, gently widening them.

TSMC verifies its 0.13 micron intellectual property process on Agilent's 93000 platform

Broad application coverage with embedded memory testing capabilities allows for TSMC's development, manufacturing of embedded memory components

TSMC has successfully verified its advanced technology 0.13 micron process on the Agilent 93000 SOC Series.

The Agilent 93000 SOC single scalable platform provides customers the flexibility to perform speed and memory upgrades as test needs evolve. More importantly, the software programs and hardware are compatible as the test development moves from characterization into volume production.

"The memory redundancy repair analysis capability on the Agilent 93000 SOC series allows us to significantly improve our manufacturing yield and provides fast time to market at high throughput," said Daniel Yang, department manager of TSMC's Fab 6 Testing Service Department.

The TSMC redundancy repair analysis for IP verification and production on the 93K is one of the most critical parts in the test process. The production device incorporates TSMC's most advanced technology wafer process.

"The APG-per-pin provides us with the greatest flexibility for embedded memory testing at full tester speed. Agilent's application support team worked very closely with TSMC engineers, transferring their knowledge and experience on programming, debugging and analyzing. We are extremely pleased with the collaborative results that continue to move our industry forward," Yang said.

The TSMC redundancy repair analysis for IP verification and production on the 93K is one of the most critical parts in the test process.

"TSMC is on the leading edge of advanced wafer process technology," said Tom Newsom, vice-president and general manager of Agilent's SOC Business Unit. "We are pleased that they have chosen the Agilent 93000 platform for the development and production testing of their 0.13 micron process."

TSMC created the semiconductor dedicated foundry industry in 1987. TSMC posted annual sales of U.S. $5.3 billion in 2000 and currently employs more than 14,500 people worldwide. It maintains account service offices in Taiwan, North America, Europe and Japan. ◆

DID YOU ? KNOW

Fiber's new wave

The late '90s boom for builders of undersea fiber-optic trunks produced miles and miles of underseas cable lines. Newer cables can use dense wavelength division multiplexing and optical switching to squeeze more data channels onto existing bandwidth—modes of expansion far cheaper than laying more lines. In Asia, cable capacity is expected to rocket from practically nil in 2000 to nearly a third of the world's total by 2003, when Singapore's throughput will rival that of the U.S.

Submarine cable capacity by region (Gbps)

North America-Europe		
2000	2003	Maximum capacity
547	5,648	12,322
Americas		
2000	2003	Maximum capacity
291	3,696	8,7562
Asia-North America		
2000	2003	Maximum capacity
244	5,117	16,904
Intra-Asia		
2000	2003	Maximum capacity
15	8,438	20,220
Europe-Africa-Asia		
2000	2003	Maximum capacity
51	75	131
Total		
2000	2003	Maximum capacity
1,148	22,975	58,333

Source: Wired *magazine*



Agilent 93000 SOC Series' broad application coverage

- High-speed digital
- Analog
- Serial communications
- Scan
- Embedded memory
- RF

The standards are changing in an emerging Bluetooth market

In today's wireless market, many new applications are emerging. Bluetooth™, a high-volume market expected to grow to more than 1.15 billion units in 2005 (source: *Micrologic Research*), is showing up in the consumer market today. But the standards for Bluetooth continue to change—adding the functionality and interoperability demanded by the consumer market.

The first standard released was Bluetooth 1.0 in December 1999. The current standard is Bluetooth 1.1, released in February 2001. Bluetooth 2.0—which will enable data rates of 2 Mbps and 10 Mbps—is in discussion, though it will not replace Bluetooth 1.1.

In order to be widely accepted by the consumer market, Bluetooth will need to be low cost. Industry analysts estimate that a $5 bill of material for Bluetooth modules will be required. In order to reach this goal, test times for radio modem integrated circuits (ICs) will have to be about 1.5 to 2 seconds.

In addition to changing standards and continuing price erosion, integration levels continue to increase. More and more functionality is being placed on smaller chips.

Bluetooth module

There are mainly two chip implementations of the Bluetooth module—radio modem IC and baseband controller IC. There are also single chip or single package solutions available. As integration levels continue to increase, single chip or single package solutions will be standard. However, demand for radio modem ICs will continue for applications where the Bluetooth baseband controller is built into the host appliance's control logic.

The Bluetooth block diagram shown below gives a general idea of how the Bluetooth module operates. In receive mode, a 2.4 GHz frequency hopping signal is received through the antenna and amplified. The data is downconverted by setting the modulated LO to the correct frequency to match the frequency hopping signal. The receiver then demodulates the signal and recovers the data, which is sent to the host appliance.

In transmit mode, the Bluetooth module receives digital data from the host appliance. The data is converted to analog, modulated onto a carrier signal and upconverted to the correct frequency. The signal is then amplified and transmitted through the antenna.

Radio modem IC test

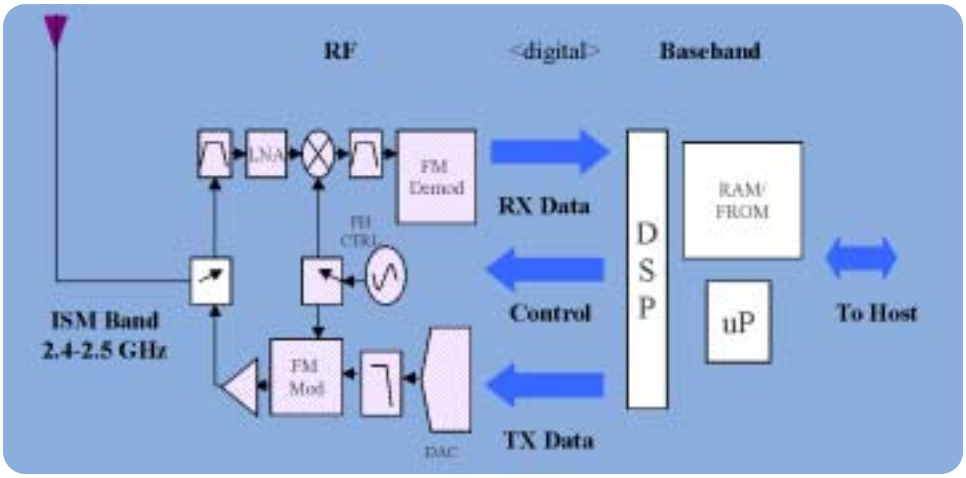
There are a number of transmitter and receiver tests required for the Bluetooth radio modem IC. The following list on the right gives a brief explanation of each.

Transmitter Tests:

- Maximum Output Power Over Frequency – Measure the maximum output power from the device under test (DUT) at several different frequencies.
- Output Power Control – Adjust the output power of the DUT and measure output power control.
- Spurious Emissions:
  - *In-band* – Measure the signal leakage from desired channel into adjacent channels.
  - *Out-of-Band* – Measure signal leakage into frequency bands above and below the ISM band (2.400 to 2.4835 GHz). For example, from 30 MHz to 1 GHz, the emissions must be < -36 dBm in operation mode and < -57 dBm in idle mode; from 5.15 to 5.3 GHz, the emissions must be < -47dBm in operation and idle mode.
- Modulation Characteristics:
  - *Initial Frequency Tolerance* – Verify the accuracy of the transmitter's carrier frequency.
  - *Drift over DH1, DH3, DH5 packets* – Measure drift of the carrier frequency over several different packet lengths.
  - *Maximum/Minimum Deviation* – Measure frequency deviation across different bits in a packet.
- Synthesizer lock time – Measure how long it takes the synthesizer to lock to a new frequency.
- 20 dB bandwidth – Verify that the 20 dB bandwidth of a modulated signal is less than 1 MHz.

Continued on page 12

Bluetooth Block Diagram



The Bluetooth trademarks are owned by their proprietor and used by Agilent Technologies under license.

Continued from page 11

Receiver Tests:

- Receiver Dynamic Range:
  - * *Minimum Sensitivity* – Stimulate the DUT with a low-level signal and measure bit error rate (BER).
  - * *Maximum Input Power* – Stimulate the DUT with a strong signal and measure BER.
- Interference Performance:
  - * *Co-channel* – A weak interference signal is placed in the same channel as the desired signal to check the ability of the DUT to recover data in the presence of a co-channel interferer.
  - * *Adjacent Channel 1, 2, 3 MHz* – Measure BER with interference signals in channels adjacent to the desired channel.
- Out-of-Band Blocking – Measure BER with an interferer signal outside of the ISM band in addition to the desired signal. For an interfering signal between 2.0 – 2.399 GHz, the interfering signal level must be -27 dBm and for an interfering signal between 2.498 and 3.0 GHz, the interfering signal level must be -27 dBm.
- Intermodulation Characteristics – The DUT is stimulated with a three-tone signal – the desired modulated signal, a CW interferer signal and a modulated interferer signal. The interferer signals are spaced so the intermodulation product of the CW signal and the modulated signal will fall in the desired channel. The BER of the DUT will depend on how high the intermodulation product is of the two interfering signals. Intermodulation should be tested for n = 3,4 and 5.
- Frequency Hopping – A number of the receiver tests are performed under frequency hopping conditions.

Essentially, the transmitter tests are power measurements over frequency and frequency measurements over time. The receiver tests are basically several BER measurements performed under different stimulus conditions. Thus, reducing BER measurement test times will significantly reduce receiver test times and utilizing fast switching sources can reduce transmitter test times.

Reducing test times

With the Agilent 93000's RF Measurement Suite, four digital channels are specifically designed for BER measurements. Thus, real-time BER measurements can be made in parallel on up to four devices under test (DUTs)—minimizing BER test times. For example, when measuring BER with 40,880 bits, a test time—for four devices in parallel—of 66 ms is achieved. As the data rate is 1 Mbps, it takes about 41 ms just to get the data. Using 102,200 bits, it takes 102 ms of the 127 ms test time to get the data. Resulting in an overhead of only about 25 ms.

Test time reductions in the transmitter tests are realized with the fast switching sources used as the RF Measurement Suite's primary RF source and system LO source. The fast power level and frequency switching allows significant test time reduction in power, gain, harmonic, and intermodulation measurements. The fast switching source also enables the frequency hopping capability of the RF Measurement Suite.

In addition to real-time BER measurements and fast switching sources, the Agilent 93000 with RF Measurement Suite is capable of real-time RF data processing. The unique, real-time RF data processing architecture of the RF Measurement Suite allows data manipulation and comparison in the DSP of the RF receiver, avoiding time consuming downloads of data into the host computer.

The RF Measurement Suite supports up to quad-site test—ensuring the highest throughput. Using Agilent's time-proven RF technology, accurate and repeatable measurements are assured from site-to-site.

Reducing test times and increasing throughput are critical in reducing cost of test. However, it is important to look at more than just test costs. In today's fast-paced market, time-to-market is also critical. Things such as DUT board complexity and correlation of characterization data to production data should also be considered.

The RF Measurement Suite design allows for simple DUT boards. All RF components—such as splitters, switches, combiners, amplifiers and attenuators—are built into the test system, not on the DUT board, reducing both cost and development time for new DUT boards. Simple DUT boards increase repeatability of the test system, ensuring better tester-to-tester and tester-to-bench correlation, while also increasing system reliability to minimize downtime.

The Agilent 93000 with RF Measurement Suite uses the same measurement algorithms and hardware as Agilent's benchtop equipment. This provides quick correlation from the Agilent 93000 to benchtop equipment—reducing the time it takes to correlate characterization data to production data—ultimately reducing time to market.

The leading provider

Agilent is the number one provider of wireless test solutions with more than 10,000 employees focused on technology for the wireless communications market. When Agilent's wireless test expertise is combined with the Agilent 93000 SOC Series, the result is an ultimate test solution for Bluetooth radio modem ICs—a test solution with all the benefits of the lowest cost, single-scalable platform, plus the ability to meet challenging test requirements today, and in the future. ◆

Design-for-test software available for the Agilent 93000

Test smarter and you deliver ICs faster. That's the central premise behind SmarTest Program Generator (PG) software, a new design tool built on the Agilent 93000 SmarTest system software. SmarTest PG brings true meaning to the term "Intelligent Test," creating the perfect design-for-test environment for the Agilent 93000 SOC Series test system.

SmarTest PG accelerates the way IC designs are tested and debugged by extending Agilent 93000 capabilities into the design department. Now IC designers and test engineers can work as part of the same team, even if they're in different time zones. SmarTest PG opens the design-to-test pipeline, so ICs move from design to test to fab to shipping—down the line and out the door—with minimum delay.

SmarTest PG is a link that translates EDA (electronic design automation) system data into test pattern and program files for the Agilent 93000 running the SmarTest operating system.

- Agilent 93000-ready vector, formatting and timing files include tester pin and channels, levels, timing edges and variables, pattern vector data, and test flow.

- Industry-leading capabilities for "cyclization"—traditionally the most difficult aspect of automatic program generation—include graphical timing capture, equation-based timing throughput, mid-cycle I/O, sequential cycle matching and more. SmarTest PG makes sure that design timing cycles have a tight match in test.

- Tests engineers can customize their views of design data. They can view design and test domains at the same time, compose descriptive specs and timing edge labels using a variety of controls, view timing track properties, control data display radix, view relationships and expression representation, and much more.

The benefits of SmarTest PG go directly to the bottom line. Automatic program generation is fast and accurate, so ICs are tested and debugged with fewer engineering hours. Design and test engineers work with one development tool rather than multiple custom or commercial applications, reducing maintenance and IT support costs. And productivity is enhanced in a standardized environment, with the gains multiplying over time as a greater knowledge-base is built and shared across design and test.

Perhaps the most important benefit of SmarTest PG is the simplest: The design-for-test process is more efficient, so ICs ship sooner, which is the real bottom line in IC manufacturing.

SmarTest PG is being introduced at the International Test Conference (ITC) in Baltimore, Maryland, on October 30, 2001. Visit Booth #1321 for a demo, or go online (after ITC) to learn more: **agilent.com/see/smartestpg.** ◆

DID YOU ? KNOW

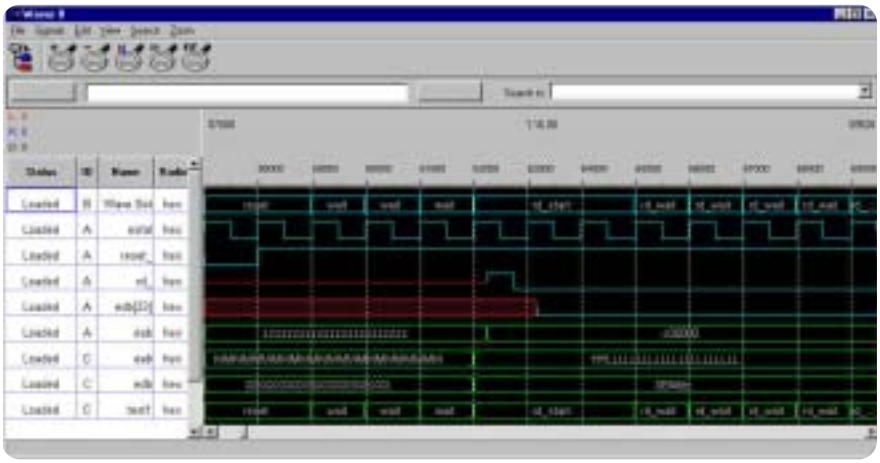


Who made the first rubber balls?

The ancient Mayans of Central America made rubber out of natural latex 3500 years before the modern process of vulcanization was invented. They played games with rubber balls and used rubber bands to attach axe heads to their handles.

The Mayans made latex, which is the sap of rubber trees, into flexible, durable rubber by mixing it with the juice of morning glory vines. The mixture developed molecular cross-links that made the latex elastic, and removed substances that caused the rubber to turn brittle. The resulting rubber was black and bouncy, with a texture like a pencil eraser. The Mayans used balls to play Ulama, something like a cross between tennis, basketball, and soccer. The game had deep religious significance. Shown above is an ancient Mayan ball court in Honduras.

Only SmarTest PG allows design and test domains to be viewed at the same time on the same screen. Engineers get a clear view of how the Agilent 93000 test timing will match the device timing



Choosing the right parameter analyzer



Figure 1



Figure 2

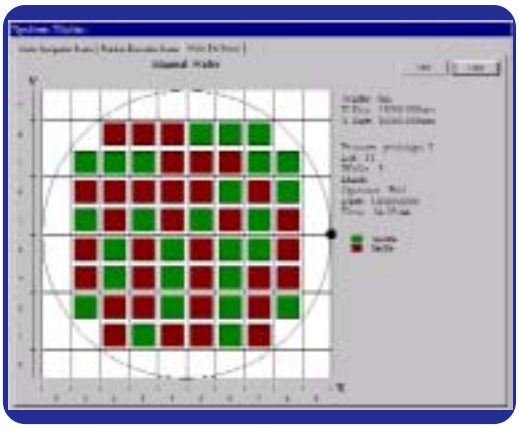


Figure 3

EDITOR'S NOTE: This is the third in a series of articles meant to help in choosing the semiconductor parameter analyzer that best fits parametric measurement needs. The previous article discussed automation test speed and instrument longevity. This article discusses the I/CV test automation software in greater detail. I/CV is available from both Metrics Technology (an Agilent partner) and is also sold by Agilent Technologies as an OEM product.

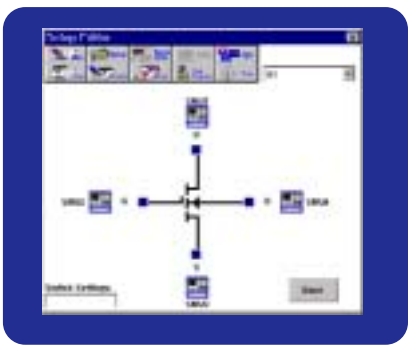
For most parameter analyzer users, the inevitable day comes when there is a need to automate instrument parametric measurements. Creating one's own test software to automate these measurements may seem appealing at first; however, using a standard software package such as I/CV offers many advantages. Among them:

- Efficiency—I/CV allows one to create algorithms and wafer test plans quickly without having to program. It also supports the most popular 200mm and 300mm semi-automated wafer probers.
- Ease of Use—I/CV's intuitive GUI interface is easy to master, and the on-line help menu reduces the learning cycle.
- Flexibility—I/CV can control a wide variety of instruments and wafer probers and allows one to customize the operator interface and test flow.
- Speed—I/CV runs on a PC external to the instruments (which can be the same PC as the wafer prober), ensuring that the instruments' controllers are not slowed down by software overhead.
- Supportability—I/CV is professionally supported.

I/CV runs on Windows 98, Windows NT, and Windows 2000. It provides a complete automated test solution by combining ICS (Interactive Characterization Software) with wafer prober control and other tools necessary for an automated test environment. (See figure 1.)

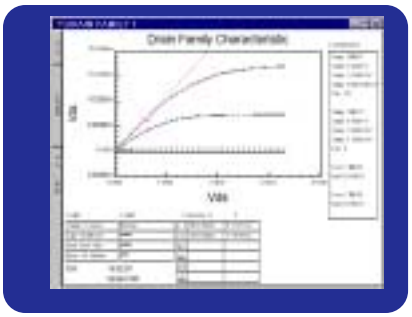
I/CV uses ICS as its measurement "engine." ICS is available as a separate product from either Agilent or Metrics, although it is included within the I/CV product. The large worldwide installed base of ICS (more than 2,000 copies) ensures that I/CV rests on a well-proven and reliable foundation. Moreover, current ICS users can upgrade to I/CV at a reduced cost.

One can easily create ICS measurement algorithms using a series of intuitive GUI windows. The Setup Editor window provides a visual representation of the DUT, and allows one to assign measurement resources to device terminals. The individual resource setup windows then allows the user to specify the distinct resource settings. Finally, the graphical display interface allows one to plot measurement results, and the built-in math functions enable one to automatically generate and display derived parameters such as tangent lines, derivatives, etc. Of course, the user can also export the graphical results in tabular format to Excel spreadsheets and other similar software packages.



Continued on page 15

Continued from page 14





Graphical measurement using ICS

I/CV provides great flexibility in wafer prober control, by using either the wafer prober software provided with the wafer prober, or using Metrics Probe software. In either case, both the measurement software (ICS) and the wafer prober software are running on the same PC. This eliminates the problems that inevitably occurs when trying to synchronize an external PC controlling the wafer prober with a second PC controlling the measurement instrument(s). (See figure 2.)

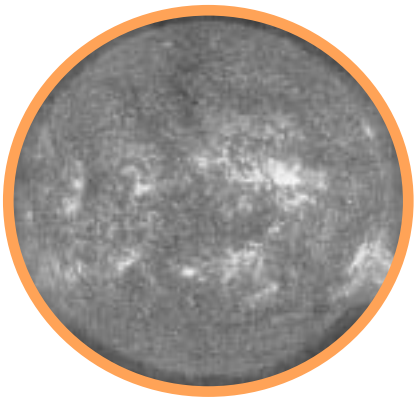
Moreover, I/CV contains numerous software "wizards" that greatly ease many tasks, such as creating a wafer test plan. I/CV also supports important wafer testing constructs, such as named sub-die locations. I/CV can display wafer-mapping results in real time, as well as aid in post-measurement analysis of measurement results across a wafer. (See figure 3.)

I/CV provides the essential capability of a built-in test sequencer. Besides providing the ability to specify die and sub-die moves across the wafer and sequence ICS measurement algorithms, the I/CV test sequencer also enables one to make conditional branching decisions and to execute test code from a variety of sources. Supported tools include Visual Basic Script, Agilent VEE, and National Instruments' LabView. The I/CV test sequencer is fast and efficient, and coupled with the new ICS capability to use the 4155C/4156C Agilent FLEX command set, the test sequencer provides the performance needed to measure 300 mm wafers and sub-quarter micron CMOS processes. (See figure below.)



It is important to consider all current and potential measurement automation needs when purchasing a parameter analyzer. The user interface of the instrument is meaningless once one moves to external PC control with a wafer prober. The important considerations then become how fast the instrument operates under remote control, and how easily one can create automated test plans using both instrument and wafer prober. Agilent Technologies believes that the 4155C/4156C used in conjunction with I/CV provides the fastest, most efficient and cost-effective means to automate testing on a semi-auto wafer prober. ◆

DID YOU? KNOW



Storms on the Sun

At the peak of an 11-year cycle, spectacular storms are raging across the surface of the Sun, throwing off huge flares—the white areas in the photo above, as well as the one on the lower right. While the flares can send radiation toward earth, disrupting communications satellites, electrical power and the weather, this one—recorded Oct. 1, 2001—had no significant reported effects. The image was made by the extreme ultraviolet imaging telescope of the Solar and Heliospheric Observatory, known as SOHO, which has been photographing the Sun since 1995 from a vantage point almost a million miles from earth. The satellite is designed to study the internal structure of the sun, its outer atmosphere, and the origin of the solar wind, the steam of highly ionized gas that blows continuously outward through the solar system.

Source: The New York Times

Concurrent Test allows parallel testing of IP blocks within each device

DID YOU ? KNOW



How large can a polyphemus moth grow?

The egg of a polyphemus moth (*Antheraea polyphemus*) is the size of a sesame seed, and the caterpillar that emerges from it is even smaller. But it is a very hungry caterpillar, and it immediately sets to work.

Over the next 56 days, the tiny eater consumes its own weight in leaves over and over again, growing to 86,000 times its initial weight. If a seven-pound human baby were to grow that much, it would weigh about 300 tons.

After spending the winter in a cocoon, the adult insect emerges: a huge, brown and white moth with two striking eyespots. It is one of the world's largest moths, with wings spanning almost six inches (15 cm).

"Multi-site testing" enables parallel testing of several identical devices at the same time. Concurrent Test is an analogous technology that enables parallel testing of multiple intellectual property (IP) blocks within each device. The combination of multi-site and concurrent test capabilities accelerate IC test execution time by an order of magnitude, slashing true test costs.

Agilent's 93000 SOC Series test system allows concurrent test of any number of on-chip functions. For example, the Agilent 93000 can test multiple logic, embedded memory and analog IP blocks in parallel rather than sequentially. The only fundamental requirement, addressed in the design phase, is that IP blocks on the SOC (system-on-a-chip) device be isolated so they are independently accessible, observable, and controllable.

Key features of the Agilent 93000 for Concurrent Test:

- Support for multi-site testing as well as concurrent test of IP functional blocks accelerates test execution time for complex SOC devices.
- Per-pin architecture allows unrestricted port configuration with single-pin granularity to match the DUT's pin-out—in test mode and mission mode.
- Per-port architecture supports independent period, timing, levels, pattern and sequencing. Unique port flexibility allows high- and low-end pin technologies to be mixed on the same tester for the lowest possible ATE cost.
- Each tester pin can operate in different modes (SCAN, BIST-Control, APG, digital capture, functional) for each test.
- Port synchronization allows asynchronous operation for independent ports, phase-synchronous operation for interdependent ports, and uncompromised OTA specification between ports.

Implementing Concurrent Test requires specific Design For Concurrent Test (DFCCT) guidelines. Designers must increase their awareness of power dissipation, signal integrity, and design-for-test area impacts throughout the design process. Test engineers must work with designers throughout the design process to generate a Concurrent Test and multi-port test strategy, and ensure that proper steps are taken to enable the success of the Concurrent Test implementation.

With DFCCT guidelines in place, improvements ripple through the production environment:

- Concurrent Test more accurately simulates system-level behavior (multiple IP blocks operating in parallel vs. sequentially).
- Capital expenditures are minimized due to the reduced number of test systems needed to handle the same volume .
- Maintenance costs are minimized due to the reduction in number of systems required.

Concurrent Test reduces the cost of verifying that SOC devices are correctly manufactured. Though it does take a joint effort among design engineers, test engineers and EDA tool vendors, the tangible benefits are hard to ignore. With Concurrent Test on the Agilent 93000, SOC devices can be tested faster, shipped sooner, and delivered at lower cost. ◆

Agilent expands flash memory test system

Fully scalable Agilent V4400 test platform allows choice of performance

Agilent has introduced two scalable performance options to its Agilent Versatest Series Model V4400 memory test system. The new models, V4400/F40 and V4400/F70, offer manufacturers of flash memory devices, used in MP3 players, digital cameras and PDAs, a choice of performance on a single scalable flash memory test platform that can grow with their needs.

As consumer demand for these flash memory devices increases, so does the need for low-cost, complex flash memory test systems. The Agilent V4400's scalable performance gives customers a cost-of-test advantage by providing three performance grades that address the range of test requirements from standard flash to burst mode to embedded memory. The top of the line model V4400/F100 runs at 100 MHz with the V4400/F70 at 70 MHz and the V4400/F40 at 40 MHz. This gives manufacturers the choice of 40, 70, or 100 MHz for today's applications, with the flexibility to expand performance on the same test system for future needs. The number of pins per site, total number of test sites, buffer memory and vector memory also can be configured to provide the optimal test system for a customer's needs.

"The new test models re-affirm Agilent's long-standing philosophy of providing customers with the right test for their current applications and room to grow to meet changing market trends," said Gayn Erickson, marketing manager of Agilent's memory test division. ◆

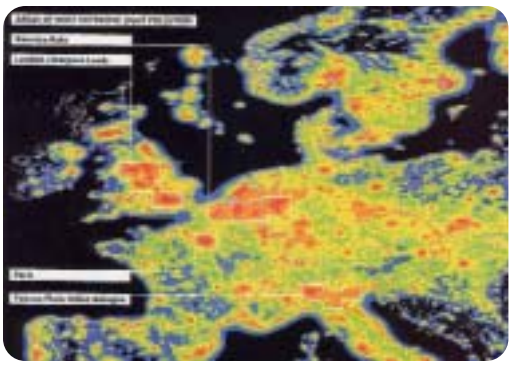
FormFactor and Agilent deliver breakthrough testing technology

In an industry first, FormFactor Inc. and Agilent have jointly developed a quarter-wafer flash memory test solution enabling global flash device manufacturers to increase throughput as much as 50 percent, significantly reducing cost of test. This solution, which tests flash memory chips typically used in high volume storage applications within wireless and other consumer products, substantially increases the throughput and yield of each test cell by accurately testing an entire 200mm wafer in just four wafer probe touchdowns.

The joint test solution, initially produced for top flash memory device manufacturer FlashVision LLC, a joint venture between Toshiba Corp. and SanDisk Corp., features FormFactor's WaferProbeTM PH100 probe card with MicroSpringTM contact technology and the Agilent Versatest Series Model V4400 Memory Test System.

Agilent's Model V4400 wafer sort solution features a rigid direct-dock interface to reduce system deflection, solving high force, high parallelism and large-active area probing challenges. Coupled with the FormFactor WaferProbe PH100, the solution produces uniform, accurate and highly repeatable contact across the entire wafer.
With more than 2,304 I/O channels and a total of more than 7,300 contacts in FormFactor's 14" probe card, the test solution has the world's highest density wafer sort interface. It is designed to maximize parallelism and probing accuracy. ◆

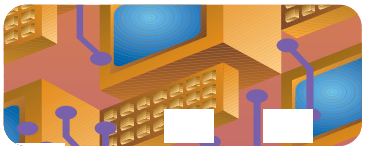
DID YOU ? KNOW



City lights vs. star lights

Paris is not Europe's only city of light: Across the European continent, the effect of city lights on the night sky can now be measured by looking down rather than up. Scientists at the University of Padova in Italy and the National Geophysical Data Center in Boulder, Colorado, are building a digital atlas of the glow from urban areas. They are creating it by merging data from multiple Air Force satellites, which is fed through new software that simulates atmospheric diffusion effects. The resulting map of Europe shows artificial night-sky brightness in the V-band—the range of light visible to the human eye. The finished product—pictured above and to be published by the International Astronomical Union, along with a map of the U.S.—will be used to identify problem areas as well as track changes. A few regions in Italy already have introduced laws limiting the amount of skyward emissions permissible at night.

Source: Wired *magazine*



For more information, please contact your Agilent sales engineer. Or visit our Website at:

http://www.agilent.com/go/semiconductor

Agilent helps with productivity, efficiency and optimum test utilization

DID YOU ? KNOW



The original Diamond Sutra at the British Library Exhibition

What's the oldest printed book with a date?

The oldest known printed book that can be clearly dated is a copy of the Sanskrit Vajracchedika-prajnaparamitasutra (Buddha's Diamond Sutra), dated by its maker on May 11, 868 AD in China. It is one of Buddhism's greatest treasures.

To make the book, seven rolls of paper were printed with wooden blocks, then cut and glued together. It is written in Chinese, with elaborately detailed illustrations of the Buddha and his disciples.

Although the Diamond Sutra is the oldest dated book, it is not the oldest printed work. Wood block printing was known for more than 100 years prior to the Diamond Sutra's printing.

The original Diamond Sutra is at the British Library Exhibition Galleries:

In today's volatile business climate, semiconductor manufacturers are faced with the formidable challenge of making and maximizing profits. The clock is ticking: Competition is driving down prices and product life cycles are continuously shortening.

Agilent Semiconductor Test Services and Support can work with manufacturers side-by-side every step of the way to help focus manufacturing operations on efficiency, productivity and optimum test system utilization. Whether the need is for production support, application support and consulting, or training, Agilent's team of experts add value throughout the semiconductor product life cycle.

New services

New services for production support include:

- Automated Test Equipment System Relocation Service
- Software Update Installation Assistance, and
- Workstation Upgrades.

The Agilent ATE Relocation Service provides the knowledge and the tools required to move highly sensitive test equipment from one location to another—worldwide—resulting in minimum downtime.

For continuous optimal test performance, Agilent Software Update Installation Assistance and test system workstation upgrades keep test systems current with the latest technological improvements. Semiconductor manufacturers can team up with expert partners to get systems up quickly and keep them running, testing parts.

Agilent's global team of consultants are an integral part of a successful test strategy. Experts are available to help throughout the product life-cycle—from quick ramp-up of new devices and technologies to optimizing the manufacturing process for fastest time-to-profit. Specific services include test program conversions, test program development and test program optimization, as well a system start-up assistance.

For example, for a large Southern California customer, Agilent's Application Development Center (ADC) recently completed a test program development "turnkey" program that provided a solution for the customer's need of having experts get a product into production in the shortest time possible. In this case, the production program went to Taiwan, which was setup and supported by local Agilent engineers.

The ADC is a project and knowledge expertise center which specializes and focuses on these types of solutions. They also work hand-in-hand with other Agilent entities for seamless support.

For system startup assistance, Agilent scales the solution around what the customer needs are. For example, one repeat Bay Area California test house simply needed a system installation and Agilent product training as their start-up assistance, because they had knowledgeable staff to meet their other needs. A large Sacramento-based customer needed a more elaborate solution—providing a customized engineering and production hardware and software interface, developing turnkey applications, providing specialized tools to optimize the customer's processes, and even having Agilent resident professional engineers that work full time at the customer site.

Continued on page 19

Innovation wave

Continued from page 2

Chartered Semiconductor Manufacturing and Silicon Manufacturing Co. Pte. Ltd. (SSMC) are trying to emulate the successes of their Taiwan counterparts.

Malaysia is successfully reinventing itself from being purely in the back-end assembly and test manufacturing business for several decades, into an emerging foundry service provider. 1st Silicon and Silterra Malaysia Sdn. Bhd. are two dedicated foundries that have been successful in attracting customers.

Korea and Japan IDMs are starting to re-examine their business models that had worked well for them in the past. However, they cannot afford to ignore the cost savings and reduced financial risk that the dedicated foundries offer. First, with new foundries costing $2 billion or more, outsourcing overflow manufacturing capacity to foundries reduces capital spending dramatically. Second, foundries are increasing investment in leading-edge technologies. IDMs can channel their investment in new chip design that requires larger capital investment to make the necessary advances. Korea also wants a piece of the expanding foundry business, resulting in start-ups like Dongbu joining Anam Semiconductor.

Agilent Technologies helps complete the circle of innovation by offering the semiconductor value chain a single "scalable" test platform. The ability to support a broad range of applications using the same hardware and software supports the innovation occurring in Asia. I believe that Asia will play a critical role in shaping the semiconductor landscape of the next decade and is well positioned to enjoy the fastest rate of growth of any world region. ◆

Continued from page 18

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DID YOU ? KNOW

Are there people with mirror-image bodies?

About one person in 8,500 has a condition called *situs inversus* in which all the internal organs are located in mirror-image to the usual arrangement. People with *situs inversus* have their heart on the right and their liver on the left. The condition does not usually result in any medical problems.

No one knows why some people are internally flip-flopped, but recently scientists have discovered some clues.

In the earliest days of embryo development there is a critical period during which cilia (tiny beating hairs) cause a current to flow across the embryo. This current carries certain substances to one side more than the other, creating a left-right difference that becomes amplified into the left-right positions of the organs.

People with situs inversus may have a genetic quirk that reverses or removes that current.

More than 60,000 visitors representing 59 countries registered to attend SEMICON/West, held in July at San Jose, California. There were 1,457 booths. Below is Agilent's booth, with the theme, "The last test platform you'll ever need to buy,"—the Agilent 93000.



global calendar

OCTOBER

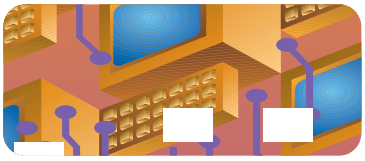
ITC
October 30—31
Baltimore, Maryland

NOVEMBER

Productronica
November 6—8
Munich, Germany

DECEMBER

SEMICON/Japan
December 5—7
Chiba, Japan



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