

Supersedes:

None

MODEL 5001C MICROPROCESSOR EXERCISER**All Serials****THE EFFECT OF THE READY LINE FROM A
UNIT UNDER TEST TO THE 5001C**

The READY line from a Unit Under Test (UUT) is connected to the 8085A Microprocessor inserted in the 5001C through a buffer (5001C Control Buffer). This buffer is enabled by setting the ENB bit to one in the 5001C Control Register. The ENB bit is set to one while executing the Internal Test programs 01-55 (ENB=0 during Test 00).

If the READY line is set low while executing Test 01-55, the 8085A and the 5001C will stop until the READY line is set high again. Any user with the UUT that uses the READY line should be aware of the potential problem when executing the Internal Test programs 01-55.

WN/I/IM

SO-7/81-02

**HEWLETT
PACKARD**

For more information contact a local Hewlett-Packard Office. (Hewlett-Packard has 200 Sales and Service Offices in 75 countries).
Or write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304, U.S.A.

Printed in U.S.A.