

M8062A-01

Modification Recommended Service Note

Supersedes:
NONE

M8062A - 32 Gb/s Front-End for J-BERT M8020A High-Performance BERT

Serial Numbers: MY55120014, MY55120016, MY55120051, MY55120054, MY55120056, MY55120057, MY55120058, MY55120064, MY55120066, MY55120068, MY55120069, MY55120070, MY55120071, MY55120072, MY55400301, MY55400302, MY55400304, MY55400305, MY55400306, MY55400307, MY55400311, MY55400312, MY55400315, MY55400317, MY55400318

The Problem: Some systems may not run error-free at data rates above 32 Gbps with System Clock selected as the M8062A Analyzer Clock Source.

Parts Required: NONE

ADMINISTRATIVE INFORMATION

ACTION	<input type="checkbox"/> ON SPECIFIED FAILURE	STANDARDS			
CATEGORY:	X AGREEABLE TIME	LABOR:	1.0 Hours		
LOCATION	<input type="checkbox"/> CUSTOMER INSTALLABLE	SERVICE:	X RETURN	USED	X RETURN
CATEGORY:	<input type="checkbox"/> ON-SITE (active On-site contract required)	INVENTORY:	<input type="checkbox"/> SCRAP	PARTS:	<input type="checkbox"/> SCRAP
	X FACTORY		<input type="checkbox"/> SEE TEXT		<input type="checkbox"/> SEE TEXT
	<input type="checkbox"/> CHANNEL PARTNERS				
AVAILABILITY:	PRODUCT'S SUPPORT LIFE	NO CHARGE AVAILABLE UNTIL:	PRODUCT'S SUPPORT LIFE		
	X Calibration Required	PRODUCT LINE:	PL24		
	<input type="checkbox"/> Calibration NOT Required	AUTHOR:	MM		

ADDITIONAL INFORMATION:
Hardware modification can be performed at the Factory only.

Situation:

When the system clock (“SYS CLK”) is selected as the M8062A analyzer clock source (Data In > Clock > Source), the clock signal for the M8062A analyzer is supplied to the M8062A from the M8041A via the 4-wire sync cable. On affected units, clock sensitivity at the M8062A Sync In port may be poor when operating at the highest data rates (32.0 – 32.4 Gbps). This can result in failure of the system to run error-free when connected in loop back (data outputs connected to data inputs).

There is no expected impact to performance when:

- Operating at data rates below 32 Gbps.
- “CDR” or “CLK IN” is selected as the analyzer clock source.

Solution/Action:

A board level hardware modification (M8062-66802 Mod 13) exists which fixes this problem. This modification is to be performed at the Factory only.

This modification is to be performed on all listed units sent to the Factory for calibration or repair, even if the failure symptom is not observable. Implementation of this modification is to be performed at the expense of the Factory. The customer may be charged for failures found on incoming test which are not related to this modification.

It is necessary to run full performance verification after this modification has been performed.

Revision History:

Date	Service Note Revision	Author	Reason for Change
12 April 2016	01	MM	As Published